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### OBIC analysis of different edge terminations of planar 1.6 kV 4H-SiC diodes

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**Abstract.** High voltage SiC semiconductor devices have been successfully fabricated and some of them are commercially available [1]. To achieve experimental breakdown voltage values as close as possible to the theoretical value, i.e. value of the theoretical semi-infinite diode, it is necessary to protect the periphery of the devices against premature breakdown due to locally high electric fields. Mesa structures and junction termination extension (JTE) as well as guard rings, and combinations of these techniques, have been successfully employed. Each of them has particular drawbacks. Especially, JTE are difficult to optimize in terms of impurity dose to implant, as well as in terms of geometric dimensions. This paper is a study of the spreading of the electric field at the edge of bipolar diodes protected by JTE and field rings, by optical beam induced current.

#### Introduction

Due to its good properties, SiC has potential for high voltage applications. Bipolar or Schottky devices have been fabricated and are commercially available. To block high voltage with low leakage currents, the periphery of the diodes must be optimized, so that to avoid premature breakdown at the surface of the component. The efficiency is therefore defined as the ratio between experimental breakdown voltage and the theoretical one. Several kinds of periphery have been studied and JTE (Junction Termination Extension) is a good technological solution. But other technological solutions exists, such as guard ring, field plates, mesa-isolated devices. Diodes protected by JTE, guard rings, or by combination of both JTE and rings have been realized and tested. This paper reports results obtained by OBIC (Optical Beam Induced Current).

#### **Experimental details**

Several kinds of JTE-protected planar diodes have been realised by CNM, using 4H-SiC n-type Cree epilayers of 10  $\mu$ m doped at 9.5×10<sup>15</sup> cm<sup>-3</sup>. Current voltage measurements have been performed on bipolar diodes, Schottky diodes and JBS protected by a single JTE or by a double zone JTE, or by field guard ring, in order to measure their breakdown voltages.

JTE have been realised by Al implantation. Several kinds of JTE have been compared. Single JTE contains a dose of  $1.1 \times 10^{13}$  cm<sup>-2</sup>, and have a length of 30, 60 or 120 µm. Double JTE consists in a first JTE realised with a dose of  $10^{14}$  cm<sup>-2</sup>, and a second, with the same dose as single JTE. The two JTE are placed side by side or are embedded. Also diodes protected by 5 floating guard rings of 8 µm length, spaced by 3 µm, have been realised. All these structures are schematised in Figure 1.

As a general rule, all protected devices of the wafers are able to block  $\sim 1.6$  kV, except those protected by only floating guard rings ( $\sim 1.3$  kV). It is important to note that all these devices are passivated. The few non passivated diodes have very high leakage currents.

Optical Beam Induced Current (OBIC) analyses have also been performed on these diodes in order to check the distribution of the electric field at the edge of the devices.



Figure 1 : Schematic cross sections of diodes with different periphery protections. Thicknesses of the layer are not proportional to the reality. 1a) single JTE; 1b) five floating guard rings; 1c) two side-by-side JTE; 1d) two embedded JTE.

Experimental OBIC set-up consists in an Ar<sup>++</sup> laser with a wavelength of 333.6 nm for this study, which corresponds to a penetration depth of ~11  $\mu$ m. The laser beam is focused to a diameter of 3-4  $\mu$ m at the surface of the sample by several lenses and modulated at 70 Hz by a mechanical chopper. The current modulation is detected by a lock-in amplifier (SR830). The sample is reverse biased by a Keithley 237 Source Measurement Unit (SMU). Sample is carried by motorized micro-translation stages. The UV beam generates free carriers in the semiconductor. If these carriers are generated in a space charge region, they are separated by the electric field and current is measured by the lock-in amplifier. So that it is possible to study the lateral extension of the space charge region.

#### **Results and discussion**

Figure 2 and Figure 3 shows OBIC characteristics obtained at different reverse biases. For easier lecture, JTE region and anode have been drawn at the bottom of the graphs. Figure 2 shows that the JTE perfectly plays its role, i.e. it is depleted on its whole length, so that there is no peak near the emitter or at the edge of the JTE. It indicates that the dose of the JTE is close to the optimized value, see also [2]. In Figure 3, it is possible to distinguish the two different JTE zones. Indeed the OBIC signal is higher in the lower doped JTE (namely JTE2), i.e. more carriers are generated in the space charge region that extends deeper in JTE 2 than in JTE1. In other words, it is due to the lower doping level of JTE2.

Figure 4 shows similar measurements on a diode protected by two JTE placed side by side (with an overlap of  $5\mu m$  between the two zones). There is no noticeable difference between the signals measured in Figure 3 and 4. This is in agreement with simulations and measurements of the

breakdown voltage  $V_{br}$  [3]. In both case,  $V_{br}$  increases with the JTE length, and is equal for embedded or side-by-side JTE structures. Measurements at higher voltages could sometimes show the appearance of a peak nears the emitter or at the edge of the JTE [2], depending on the doping level of the JTE, but leakage currents becomes too high on these diodes to allow OBIC measurements. Highest applied voltage is 700 V on a diode similar to that of Fig. 4. There is no noticeable difference in the shape of the peak between 500 and 700 V.

2.5

-500 V

= -400 V





V = -300 \ = -200 V 2.0 = -100 \ OBIC signal (nA) 1.5 1.0 0.5 0.0 JTE2 200 ò 400 600 800 1000 X (µm)

Figure 3 : OBIC measurements obtained on a bipolar diode protected by two embedded JTE (JTE1 : 65  $\mu$ m length, doped at ~2×10<sup>18</sup> cm<sup>-3</sup>, 0.5  $\mu$ m depth and JTE2 : 125  $\mu$ m doped at ~10<sup>17</sup> cm<sup>-3</sup>, 0.8  $\mu$ m depth). Reverse voltage varies from 0 to 500 V. Locations of JTE and anode metallisation are indicated. Efficiency = 87%.





Figure 4 : OBIC measurements obtained on a bipolar diode protected by two side by side JTE (JTE1 : 65  $\mu$ m length, doped at ~2×10<sup>18</sup> cm<sup>-3</sup>, 0.5  $\mu$ m depth and JTE2 : 65  $\mu$ m doped at ~10<sup>17</sup> cm<sup>-3</sup>, 0.8  $\mu$ m depth). Reverse voltage varies from 0 to 500 V. Locations of JTE and anode metallisation are indicated. Efficiency = 87%.

Figure 5 : OBIC measurements obtained on a bipolar diode protected by FGR doped at  $\sim 2 \times 10^{17}$  cm<sup>-3</sup>. Reverse voltage varies from 0 to 500 V. Locations of anode metallisation and EGR are indicated. Efficiency = 60%.

Bipolar diodes protected by floating guard rings (FGR) have also been studied. Figure 4 shows OBIC measurements obtained from a diode with FGR doped at  $2 \times 10^{17}$  cm<sup>-3</sup>. Similar analyses have

also been performed on EGR doped at  $2 \times 10^{18}$  and  $2 \times 10^{19}$  cm<sup>-3</sup>. No difference between OBIC signals have been detected up to 500 V, although the V<sub>br</sub> varies from 1100 V to 800 V with increasing FGR's doping level [3]. This can be due to the relatively low applied bias in regard to V<sub>br</sub>. However, applying higher voltages under UV beam often results in higher currents that are not supported by the lock in amplifier. Considering V<sub>br</sub>, the efficiency of FGR has been showed lower than JTE [3] : ~1100 V (efficiency of ~60%) for FGR protected diodes, and ~1500 V (efficiency of ~80%) for JTE protected diodes (with JTE length of 55 µm). It has been assumed that it can be due to an inaccurate optimization of the distance between rings. However, it is not possible to distinguish OBIC peak between the rings, as it can be expected if equipotential lines tighten between rings. This can be explained by the diameter of the UV beam which has a diameter in the same range as the distance between the rings, but also by the fact that equipotential lines do not tighten between rings, which proves that FGRs' geometry is rather correct.

As shown by previous figures, OBIC measurements allow the study of the distribution of electric field in the periphery of diodes. Differences in doping level and/or depth of implanted zones can be detected. However to obtain quantitative estimation of doping, comparison with simulation results are needed.

Another noticeable fact in all these figures is the presence of a spreading out of the OBIC signal farther from the JTE or FGR. These "shoulders" are probably due to the presence of the silica film which is used to passivate the surface structure. The presence of traps in this oxide or at the interface with SiC, may lead to the spreading out. In fact, this spreading-out is extremely dependent of the diode under test, and is also dependent on the measurement historic (for example, the order in which reverse biases are applied, or if the diode is in stand-by several days before measuring again). The negative bias of the anode creates a high electric field in the oxide. As a consequence, a part of the holes that are generated by the UV beam are probably captured in interface states or in oxide traps. Once they are trapped, it creates a positive charge in the oxide which can deplete the semiconductor under the oxide interface. Far from the diode, the electric field in the oxide is weak and therefore, there is no hole traps, so that the OBIC signal is low. This hole trapping phenomenon is the same as that observed in MOS capacitors [4,5].

Unfortunately all diodes without passivation layers have excess leakage currents and OBIC measurements are not possible.

#### Conclusion

OBIC analyses allow the study of the space charge region extension in the periphery of diodes. Measurements on diodes with different protections show clearly the presence of one or two JTE. Presence of FGR is also detected. It also proves that OBIC analysis is possible in spite of the presence of an oxide layer. However the presence of the oxide passivation layer, due to the trapping of generated holes in the oxide or at the SiO<sub>2</sub>/SiC interface contributes to the spreading out of the equipotential lines at the edge of the diode.

#### References

[1] SiCED Electronics Development GmbH, http://www.siced.de.

[2] C. Raynaud, S.R. Wang, D. Planson, M. Lazar, J.P. Chante. Diamond and Related Materials, Vol. 13/9 (2004), p. 1697-1703.

[3] R. Perez Rodriguez. "Planar edge terminations and related manufacturing process technology for high power 4H-SiC diodes". Ph.D. thesis. Universitat Autonoma de Barcelona, 2005. 223p.

[4] V. V. Afanasev et al. Microelectronic Engin. Vol. 28 (1995), p.197-200.

[5] C. Raynaud. J. Non-Crystalline Solids Vol. 280 (2001), p.1-31.