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Process Optimization for High Temperature SiC Lateral Devices

M. Soueidan^{1,a}, M. Lazar^{1,b}, D. M. Nguyen^{1,c}, D. Tournier^{1,d},
C. Raynaud^{1,e}, and D. Planson^{1,f}

¹ AMPERE, UMR CNRS 5005, INSA-Lyon, F-69621, France

^amaher.soueidan@insa-lyon.fr, ^bmihai.lazar@insa-lyon.fr, ^cduy-minh.nguyen@insa-lyon.fr, ^ddominique.tournier@insa-lyon.fr, ^echristophe.raynaud@insa-lyon.fr, ^fdominique.planson@insa-lyon.fr

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Abstract. Complementary lateral structures, N-JFETs, P-JFETS and bipolar diodes, have been implemented in p and n-type 4H-SiC wafers with epilayers. The device were optimized using finite element code MEDICITM simulations, based on ion implanted and etched Reduced-Surface-Field structures. Two Ti/Ni alloy composition are found to form ohmic contacts compatibles with high temperature device operation. 900°C and respectively 1000°C post-metallisation annealing during 2min are necessary. The presence of a graphite layer is determined by XPS (X-ray photon spectroscopy) analyses at the metal-semiconductor interface. On the fabricated p and n-type lateral JFETs, in blocking state, breakdown voltage as high as 600V are obtained.

Introduction

The principal qualities necessary in power devices developing and integration are good static and dynamic characteristics at high temperatures, a high breakdown voltage and a size that must be as smallest as possible. The device miniaturization allows to increase considerably the performances of the integrated systems, such as the reduction of switching time and losses related to the distance of signal propagation. The use of silicon carbide (SiC) makes it possible and answers these various criteria.

The high electric field that may be developed in SiC allows to consider the integration of diodes and switching devices. A lateral integration is preferable due to the high impurities concentration on the substrates. Lateral technology improves the power integration degree, i.e. the density of the devices that could be implemented in SiC wafers.

In this paper technological process optimisation for SiC lateral device realization are presented, in particular for bipolar diodes and JFETs (Junction Field Effect Transistors), able to work at high temperature and high voltage up to 300°C and 600V respectively.

Experimental

Complementary structures, N-JFETs, P-JFETS and bipolar diodes, have been implemented in p and n-type commercial 4H-SiC wafers with epilayers P⁻ and N⁻ respectively. In figure 1 is a schematical cross sectional view of an optimized lateral N-JFET together with the predicted I_{ds} - V_{ds} associated characteristic obtained by MEDICITM simulations. The RESURF (Reduced Surface Field) technique [1] is applied here for the design of SiC lateral diodes and JFETs in order to reduce the on-resistance R_{on} and to increase the blocking voltage by decreasing the lateral device sizes. The RESURF technology consists in introducing layers that are defined by their geometric dimensions (thickness and length), doping type and concentration. By dimensioning these parameters, the presence of these layers will generate a more homogenous distribution of the electric field in the device structures. The device structures were optimized using finite element code MEDICITM simulations.

To realize these structures two runs have been performed. For the first one, the n- and p-type channels have been obtained by ion implantations of nitrogen (N⁺-N²⁺) and aluminium (Al²⁺) in

order to reach a 1 to $2 \times 10^{17} \text{ cm}^{-3}$ box profile doping. For the second run these layers have been fabricated by epitaxial growth using CVD technique. Structures of the first run are planar, whereas mesa structures are occurred by Reactive Ion Etching (RIE) process during the second run. Sources, drains (for JFETs) and anodes, cathodes (for bipolar diodes) have been realized by ion implantation doping of Al^{2+} for the p-type zones and $\text{N}^+ \text{-N}^{2+}$ for the n-type zones. Relative high doses (3 to $5 \times 10^{14} \text{ cm}^{-2}$) were implanted through a sacrificial oxide to obtain superficial zones with a doping ranging from 3 to $4 \times 10^{19} \text{ cm}^{-3}$. A last thin layer was ion implanted in surface with a doping value in the same order with the channel but in opposite type (double RESURF structure [2]). In blocking state the role of this top layer is to avoid the lateral depletion of the channel before the vertically expansion of the SCR (Space Charge Region).

Eight levels of masks have been used for the device fabrication. During the technological process several steps had to be optimized: deep ion implantation [3], post-implantation annealing [4], deep RIE [5], multi-layer isolation and ohmic contact formation, compatibles with high temperature device operation. This paper is focused on this last technological step.

Ni/Ti alloys were studied for the realisation of ohmic contacts, especially on p-type 4H-SiC layers with a doping obtained by ion implantation (3 to $4 \times 10^{19} \text{ cm}^{-3}$). The ohmic contact was achieved on etching and non etching surface, such as on the mesa lateral JFETs structures.

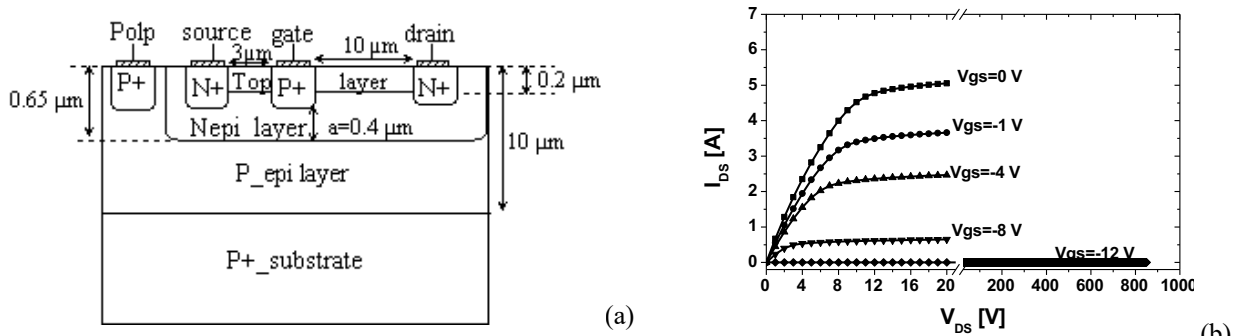


Fig.1: N-type lateral JFET structure(a) and its electrical characteristics (b) obtained by MEDICITM simulations.

TLM (Transmission Line Method) structures were achieved with a special attention on the electrical isolation of this structures and avoiding bi-dimensional effects. Three alloy compositions were studied. For the ohmic contact formation, after the successive metal layers evaporation a rapid thermal annealing (RTA) was performed in two steps, in the second step the temperature being varied from 800 to 1200°C during 2 min.

Results and discussion

The effects of Ti (1 to 48 nm) layer thickness on the properties of bilayer nickel/titanium contacts to p-type 4H-SiC with a constant top Ni layer thickness of 100 nm were investigated. We can deduce that no ohmic contact formation was obtained (not shown) in the case of 1 nm Ti layer thickness. In contrast, when the Ti amount increases from 1 to 25 nm , the ohmic contact was obtained at 1000°C (see fig.2a). Moreover, for this alloy composition, the current-voltage characteristics before and after annealing at 1200°C are identical. For annealing at 800 and 900°C , we can see that I-V characteristics are similar and the contact is almost ohmic. It was found that the annealing at high temperature (1200°C) destroyed the contact. We can also see that the formation of ohmic contact was obtained at 900°C when the Ti amount is equal to 48 nm . This is presented in fig. 2b.

The specific contact resistance is in the range of 10^{-4} to $10^{-3} \Omega \cdot \text{cm}^2$, measured at room temperature. This specific contact resistance is relatively high and this could be related to the presence of a graphite layer (C-C) as determined by XPS (X-ray photon spectroscopy) analyses at the interface between the Ni/Ti alloy and the SiC surface after post-metallisation annealing [6].

According to the XPS measurement, we can deduce the metal-semiconductor interface formation (Ni_2Si and TiC). The XPS spectra for the 48 nm Ti sample are shown in Fig. 3.

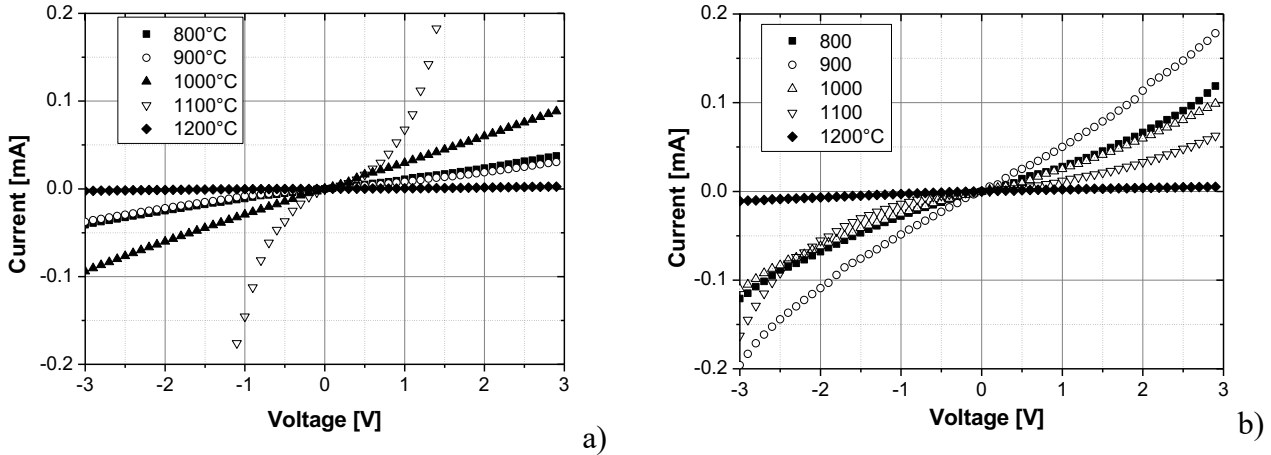


Fig.2: Ohmic contact formation occurs at 1000°C for 25 nm of Ti (a) and at 900°C for 48 nm of Ti (b). Note that the Ni content was fixed at 100 nm.

Up to 650 K, these contacts were validated on bipolar diodes, polarized in direct bias at 5V during one hour. No significant variation on the device characteristics was observed (Fig4). Similar values and behaviour are obtained for the contacts realized on 4H-SiC etched surface up to 2 μm depth.

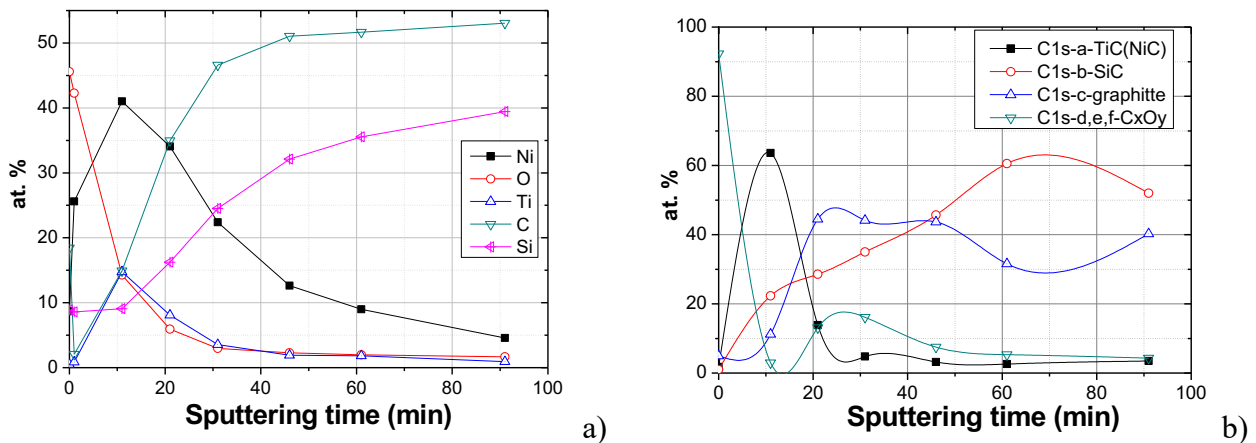


Fig.3: Element profile (a) with deconvolution of the C_{1s} pic (b) obtained from XPS analyses on ohmic contacts formed with 48nm of Ti / 100nm of Ni.

We have chosen the 48 nm of Ti and 100 nm of Ni for the fabrication of lateral JFETs. The lateral JFETs run where the n-type and p-type channels are realized by ion implantation is achieved. The first results show that in blocking state, the breakdown voltage (V_{BR}) was validated for both n-type and p-type lateral JFETs. V_{BR} values as high as 600V (Fig.5) were obtained which is in conformity to the required specifications for these devices.

In the on-state regime, p-type lateral JFETs are normally-off. For the realization of the p-type channel Al^{++} ions have been used. Compared to the N^{++} ions used in the n-type channel formation, their implantation is not deep enough to form a sufficiently wide channel under the n-type gate. Moreover the n-type gate realized also by ion implantation may present a channelling tail deviation responsible for a compensation of the p-type channel doping. This phenomenon is difficult to control on SiC hexagonal [7].

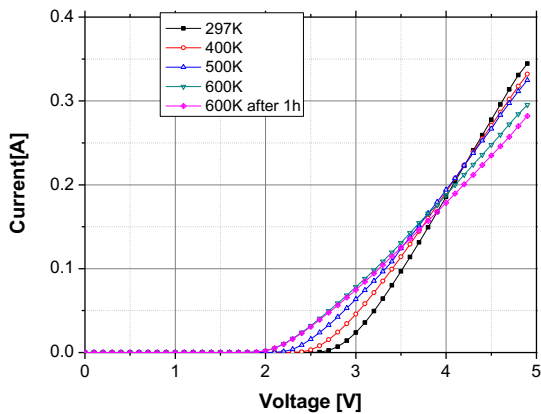


Fig.4: Forward biased current-voltage characteristics dependence in temperature of bipolar diodes with Ti/Ni ohmic contacts

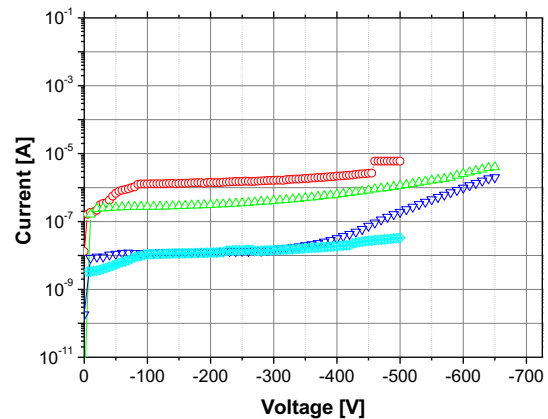


Fig.5: Typical voltage sustain of p and n-type JFETs in blocking state

Although etched lateral JFET structures of the second run asked a more elaborated and longer technological process, they are normally free from these problems.

Conclusion

In order to fabricate p and n-type lateral JFETs, technological steps have been developed with a particular accent on the realisation of ohmic contacts compatibles with high temperature device operation. Ohmic contacts are obtained for two Ti/Ni allows on p-type SiC, the specific contact resistance presenting relatively high values due the presence of a graphite layer at the metal-semiconductor interface. No significant changes for these ohmic contacts are observed up to 650K. For the realized p and n-type JFETs the voltage sustain was validated in the blocking state, in contrast on the on-state, normally-off behaviour is obtained for the p-type JFETs.

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