Impact of RIE Etching on the Breakdown Voltage of 4H-SiC Mesa Diode

Heu Vang, Sigo Scharnholz, Christophe Raynaud, Mihai Lazar, Gontran Pâques, Dominique Planson

Impact of RIE etching on the breakdown voltage of 4H-SiC mesa diodes

H. Vang[1,2,a], S. Scharnholz[1,b], C. Raynaud[2,c], M. Lazar[2,d] and G. Pâques[1,e] D. Planson[2,f],

[1]French-German Research Institute of Saint Louis (ISL), BP 70034, 68301 Saint Louis, France

[2] AMPERE INSA Lyon, 21 Av. Jean-Capelle ; 69621 Villeurbanne, France

[a]heu.vang@fr.schneider-electric.com, [b]sigo.scharnholz@isl.eu, [c]christophe.raynaud@insa-lyon.fr, [d]mihai.lazar@insa-lyon.fr, [e]paques@isl.tm.fr, [f]dominique.planson@insa-lyon.fr,

Keywords: RIE, mesa, PiN diode, breakdown voltage

Abstract. This paper presents a comparison of the reverse characteristics of mesa terminated PiN diodes fabricated on n- and p-type 4H-SiC substrates. For n-type the attained breakdown voltages are higher and for p-type lower than expected. This is likely to be explained by the presence of negative charges at the interface between passivation oxide and SiC. Supported by XPS data we come to the conclusion that the RIE process creates surface charges which have an impact on the breakdown voltage of the fabricated diodes.

Introduction

Silicon carbide is well known to have physical and electrical properties superior to those of silicon for power, high temperature and RF applications [1]. Its critical electric field and its bandgap are ten and three times higher, respectively. However, the fabrication of SiC devices still suffers from technological difficulties. Almost all SiC demonstrators with a high breakdown voltage (10 kV) realized to date have a mesa/JTE edge termination [2-3]. This kind of structure requires an etching process. Chemical etching on SiC is hardly possible due to its high chemical inertness. Generally, only dry methods with plasma reactors are used to etch SiC. Although ICP (inductively coupled plasma) reactors demonstrate higher performance than the standard RIE (reactive ion etching) reactor [4], the latter is usually used to perform the mesa etch process.

This paper deals with the influence of reactive ion etching (RIE) on the breakdown voltage of 4H-SiC diodes with a simple mesa edge termination. Two kinds of diode were fabricated: $n^+p^-p^+$ and $p^+n^-n^+$. The former was based on a p^+ substrate with a p^- epilayer. The latter was fabricated on an n^+ wafer with an n^- epilayer. In both cases, the electrode on the top was realized by ion implantation and the mesa edge termination structure was realized by RIE. The influence of the RIE process is displayed by the reverse characteristics of the realized diodes.

Experimental

4H-SiC substrates with epilayers purchased from CREE (p^+p^-) and SiCrystal (n^+n^-) have been used. The epilayers of the p^+p^- and n^+n^- epiwafers are 10 and 11 µm, with a doping concentration of 1.53×10^{15} cm^{-3} and 5×10^{15} cm^{-3} respectively. The breakdown voltage of the structures was simulated with MEDICI™. The maximum breakdown voltages with these epiwafers are 1.6 kV and 1.4 kV for the p^+p^- and n^+n^- epiwafers respectively. The difference of these values is due to the epilayers parameters and to a higher ionization coefficient for the holes [5]. In order to analyze the impact of RIE etching on the breakdown voltage because of surface degradations, the diodes mesa depth was fixed to 5 µm. The expected breakdown voltages of theses structures (fig.1) are 1.3 kV and 1.2 kV respectively.

The samples were first cleaned in chemical solutions. On the p^+p^- epiwafer the cathodes were realized by nitrogen implantation. The anode on the n^+n^- epiwafer was formed by aluminium implantation. In order to activate the dopants, post-implantation annealing was performed in a JIPELEC inductive furnace at 1650 °C during 45 min under Ar atmosphere. The cathode of the $n^+p^-p^+$ diodes and respectively the anode of the $p^+n^-n^+$ diodes were patterned with a bilayer Ti/Ni as etching mask. The etching process was performed at 60 mTorr in an RIE reactor (250W and 350 V bias) with an SF_6/O_2 plasma [6]. An etching depth of approximately 5 µm has been obtained. After an RCA cleaning, dry oxidation was performed to realize a thin passivation layer at 1150°C during 2 hours and a post-annealing at 1150°C under nitrogen during 1 hour is performed. Just before introducing the samples in the metal evaporation chamber, the oxide was removed by Buffered Oxide Etchant in the contact areas of cathode and anode. Ti/Ni and a Ni/Al contacts are formed on the cathode and anode, respectively. Ohmic contacts are formed after annealing in RTA at 1000°C during 2 minutes [7]. The electrical characterization was performed with a probe station and a Keithley 2410 SourceMeter supplying a maximum source voltage of 1.1 kV. Having no thick passivation layer, the devices were immersed in Galden™ for the reverse characteristics.

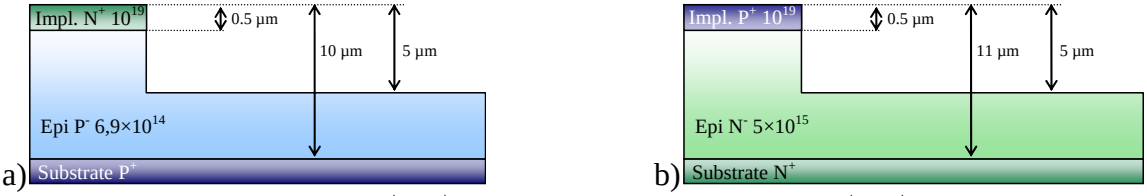

Fig. 1: a) Structure of the $n^+p^-p^+$ diode and b) structure of the $p^+n^-n^+$ diode.

Results and discussion

Electrical characterization. The two kinds of diodes were characterized in the same condition. Anode is negatively biased with respect to the cathode. Fig 2. depicts typical on state and blocking characteristics of the fabricated PiN diodes. The difference in on-state current can be attributed to the diode diameter. The statistical distribution of the breakdown voltage of $n^+p^-p^+$ diodes is presented on the left hand side of Fig. 3. The average breakdown voltage is about 550 V. This value is lower than the expected value (1.3 kV). Half of the 150 tested diodes have a breakdown voltage in the range 500 to 600 V. And only eight diodes show a breakdown voltage in excess of 1100 V, the limit of the voltage source used. On the other hand, an important number of $p^+n^-n^+$ diodes exhibit a maximum breakdown voltage greater than 1100 V, (Fig. 3, right) whereas the theoretical value was calculated to only 1000 V.

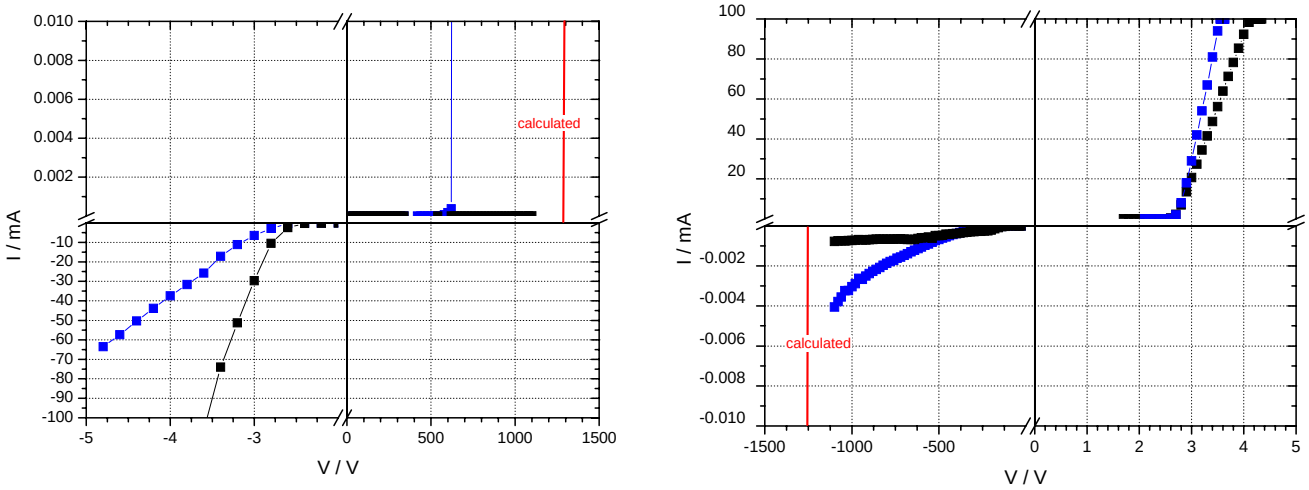

Fig. 2: Typical on-state and reverse characteristics of PiN diodes on p-type (left) and n-type substrate (right).

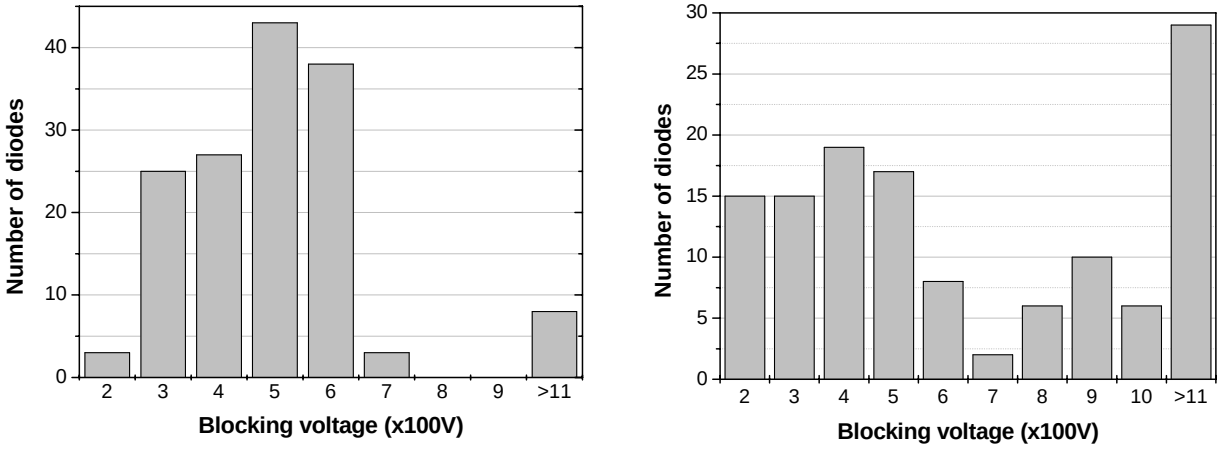

Fig. 3: Statistical distribution of the breakdown voltage of mesa terminated PiN diodes on p-type (left) and n-type epiwafers (right).

The behavior of the diodes in reverse states is likely to be explained by the presence of negative charges at the near-interface between passivation oxide and SiC. Indeed, for $n^+p^-p^+$ diodes, a negative interface charge would cause a concentration of positive counter charges at the surface of the p^- epilayer. This phenomenon prevents the spreading of the space charge region in the drift layer (Fig. 4, left). The consequence is the reduction of the mesa protection efficiency so the breakdown voltage is lower than the expected value. In opposite, for $p^+n^-n^+$ diodes, the presence of negative charges creates a high concentration of positive charges at the SiC surface. This effect enhances the spreading of the space charge region along the surface of the epilayer (Fig. 4, right). Thus, as it is the case for our results, the breakdown voltage is superior to the expected value.

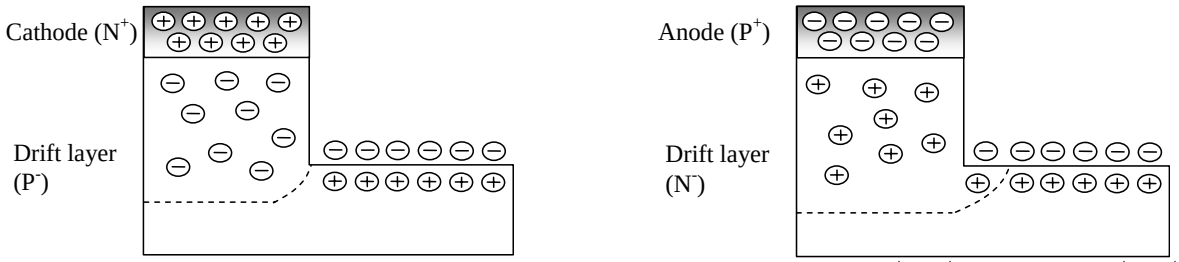

Fig. 4: Influence of negative charges at the near-surface of the $n^+p^-p^+$ (left) and $p^+n^-n^+$ diodes (right).

X-Ray Photoelectron Spectroscopy. XPS analysis was performed on etched surfaces. As can be seen in Fig. 4, a high concentration of oxygen and fluorine atoms was detected at the near-interface (up to 20 nm). Thus, it can be assumed that RIE etching process causes implantation of oxygen and fluorine ions in the SiC because of the high kinetic energy in the plasma. The presence of the F^- ions coupled with the oxygen ions creates a high concentration of negative charges at the near-interface of the SiC as we observed on our diodes reverse characteristics.

The total dose of the of the F atoms calculated from these XPS spectra is estimated to $1.3\times10^{15}cm^{-2}$. A constant density of the SiC has been utilized. The analyzing time was converted in the depth considering that 16 min of XPS analyses correspond to ~20nm in SiC (based on the etching rate of Ar ion beam during the XPS analyses). The dose is high enough to have an impact on the device electrical behavior under reverse bias. Nevertheless these analyses have been performed just after RIE process, before post-implantation annealing and oxide growth. Only a part of these atoms will become electrically actives by diffusion at SiC/SiO_2 interface.

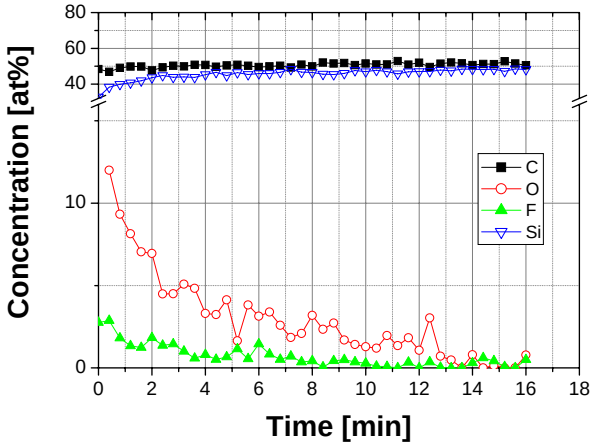

Fig. 5 : XPS analysis performed on SiC surface after RIE etching.

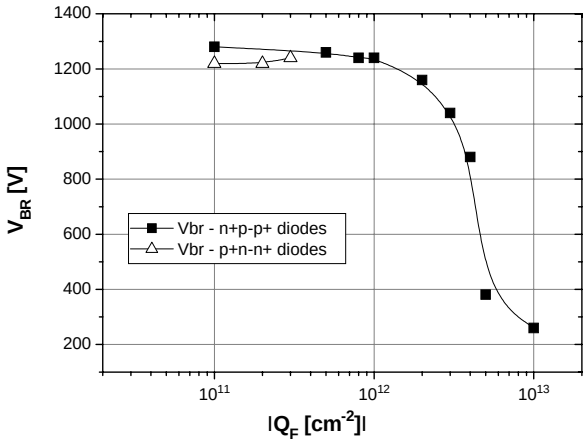

Fig.6 : Breakdown voltage of the $n^+p^-p^+$ and $p^+n^-n^+$ diodes for different concentration of negative charges at the near-interface of the SiC.

Finite-element simulations have been performed in order to investigate the influence of the negative charges at the near-interface of the SiC. The structures of the two $n^+p^-p^+$ and $p^+n^-n^+$ diodes were introduced in MEDICI^{TM} simulator with the negative charges at the oxide-SiC interface. Fig. 6 shows the influence of this charge on the diode breakdown voltages. The experimental results are confirmed especially for the $n^+p^-p^+$ diodes. For the $p^+n^-n^+$ diodes we are limited by convergence problems for the highest charge densities.

Conclusion

In both cases, the RIE process causes damage at the SiC surface that could be disclosed by negative charges whatever is the type of the epilayer. In order to support this assumption, XPS analysis was performed on a sample after etching. The results show a significant concentration of oxygen and fluorine atoms close to the exposed SiC surface. Residues are visible up to a depth of 20 nm. Thus, during the etching in the RIE reactor, species from the plasma with high energy were probably accelerated and implanted into the SiC. This induces lattice damage at the SiC near-surface. This phenomenon impacts directly on the breakdown voltage for the mesa diodes.

References

[1] R. Singh, Microelectronics Reliability 46 (2006), p. 713

[2] Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour and T. Hayashi, Proc. of the 13th Int. Symp. on Power Semiconductor Devices & ICs (2001), p. 27

[3] J.H. Zhao, P. Alexandrov, J. Zhang and X. Li, Electron Device Letters 25 (2004), p. 474

[4] D.W. Kim, H.Y. Lee, B.J. Park, H.S. Kim, Y.J. Sung, S.H. Chae, Y.W. Ko and G.Y. Yeom, Thin Solid Films 100 (2004), p. 447

[5] A.O. Konstantinov, Q. Wahah, N. Nordell, U. Lindefelt, “Ionization Rates and Critical Fields in 4H-SiC”, Applied Physics Letters 71, (1997), p.90

[6] M. Lazar, H. Vang, P. Brosselard, C. Raynaud, P. Cremillieu, J.-L. Leclercq, A. Descamps, S. Scharnholz, D. Planson, Superlattices and Microstructures 40 (2006), p. 388

[7] H. Vang, M. Lazar, P. Brosselard, C. Raynaud, P. Cremillieu, J.-L. Leclercq, J.-M. Bluet, S. Scharnholz, D. Planson, Superlattices and Microstructures 40 (2006), p. 626