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Electrical characterization of PiN diodes fabricated on a p layer selectively grown by VLS transport

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Abstract. This paper deals with electrical characterization of PiN diodes fabricated on an 8° off-axis 4H-SiC with a P⁺⁺ layer selectively grown by vapour-liquid-solid (VLS) transport. It gives evidence for the first time that a high quality P-N junction can be achieved by using this technique. This paper also discusses the role of a high temperature annealing after the VLS growth on the P-N junction properties.

Introduction

Day after day, the quality of 4H-SiC bulk and epilayer material is improving and several unipolar devices such as Schottky and JBS rectifiers, JFET and MOSFET are commercially available.

Nevertheless, some technological barriers still exist like the local and in depth p-type doping into the SiC top epilayer. Indeed, Al ion implantation is the simplest and most widely used way to currently obtain a localized doped area. However this technique has significant drawbacks. First, ion implantation process damages the crystalline quality and a high temperature annealing (typically around 1700 °C) is required to both partially activate the doping element and restore the crystalline quality [1]. In practice, a defect-free area with high p-type doping level is very difficult to obtain by ion implantation. Finally, the depth of the implanted area is limited to several hundred of nanometers when using ion implanters with a standard energy level.

SiC Selective Epitaxial Growth (SEG) by Vapour-Liquid-Solid (VLS) transport on a bowl-shaped geometry (see Fig. 1) appears to be a promising solution to perform deep, highly doped and high quality doped area either “n” or “p” type. Such SEG-VLS growth of highly p-doped (> 5x10¹⁹ cm⁻³ and 1 μm thick) SiC layer was successfully demonstrated recently on large area circular-shaped structure using Reactive Ion Etching (RIE) [2]. Such growth results need to be completed by electrical characterization of PiN diode structures. This is the purpose of the work presented in this paper.

Experiments

Fig. 1 displays the structure of the fabricated and characterized PiN diodes. The N⁻ layer was grown

in a hot-wall CVD reactor on 8°-off 4H-SiC substrate. The thickness and the doping level of this layer is respectively 15 μm and $N_d=5 \times 10^{15} \text{ cm}^{-3}$. The 1 μm depth bowl-shape structure was obtained by conventional photolithography technique and RIE under SF_6/O_2 .

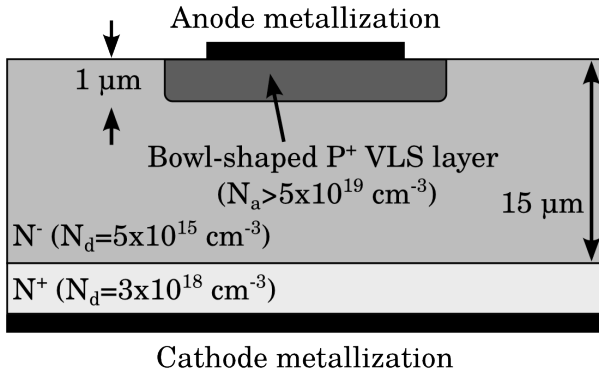


Figure 1: Structure of the fabricated and characterized PiN diodes

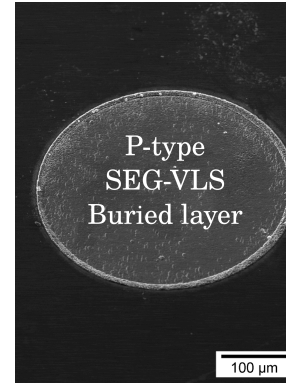


Figure 2: SEM picture of a 300 μm diameter circular PiN diode after the VLS growth

The fabricated and characterized diode is a circular diode with a diameter of 300 μm (Fig. 2). Details of the SEG-VLS technique are reported elsewhere [2]. In this study, samples grown using different conditions were electrically investigated. Among them, one was cut in two pieces and one piece was annealed at 1700°C under Ar during 30 min in order to characterize the influence of this annealing on the PiN diode forward static J-V behavior. Prior to this annealing, the surface of this sample has been passivated by a carbonized AZ5214 E photoresist.

Cathode and anode metallization stacks are Ti(5nm)Ni(170 nm) and Ni(10nm)Ti(40 nm)Al(240 nm)Ni(10 nm) respectively. Then these contacts have been annealed in a Rapid Thermal Annealing (RTA) furnace during 90 s under Ar at 900 °C and 800 °C respectively. The diodes were finally electrically characterized by using a K2410 System Measure Unit and probe station with a minimum of 10 diodes per sample at room temperature. Some of these diodes have been selected in order to perform Current-Voltage measurement at temperature (I-V-T) from 25 °C to 350 °C.

Results and discussions

Fig. 3 reports J-V behaviors of several diodes come from three different samples with different SEG-VLS growth conditions. For a better readability, only a few representative J-V characteristics have been plotted.

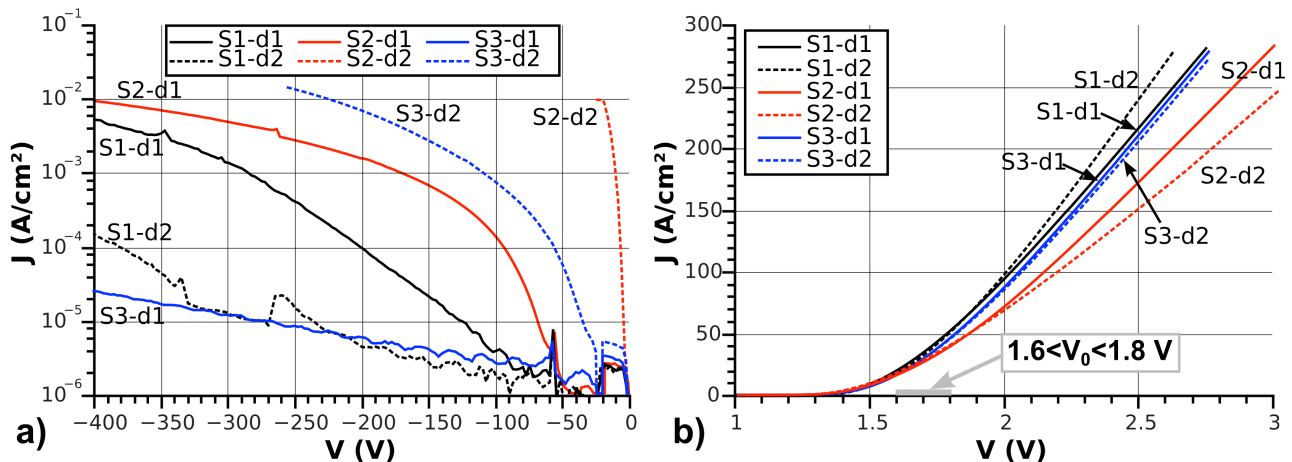


Figure 3: J-V behaviors of several diodes come from 3 different samples after the SEG-VLS growth and metallization process: a) reverse characteristics - b) forward characteristics. In the figure, “S” is for “sample” and “d” is for “diode”.

First, we did not evidence any influence of growth condition on the forward and reverse J-V characteristics. Indeed, for all samples, some diodes have a low leakage current $J < 10^{-4} \text{ A.cm}^{-2}$ at

$V = -400$ V, some have a high leakage current $J = 10^{-2} \text{ A.cm}^{-2}$ at $V = -400$ V and some have a low breakdown voltage $V_{BR} < 50$ V. Moreover, one can see on Fig. 3-b that the threshold voltage (V_0) varies from 1.6 to 1.8 V. For a 4H-SiC P-N junction, the threshold voltage is usually found at $V_0 \sim 3$ V. As a consequence, the current conduction model of our diodes had to be clarified. That is why I-V-T measurements were performed on several diodes from Sample2. Fig. 4 exhibits the result obtained for a typical diode (Fig. 4-a) and the evolution of its differential resistance (R_D) and V_0 as a function of the measurement temperature extracted from I-V-T characteristics (Fig. 4-b) extracted from the linear part of I-V-T behaviors.

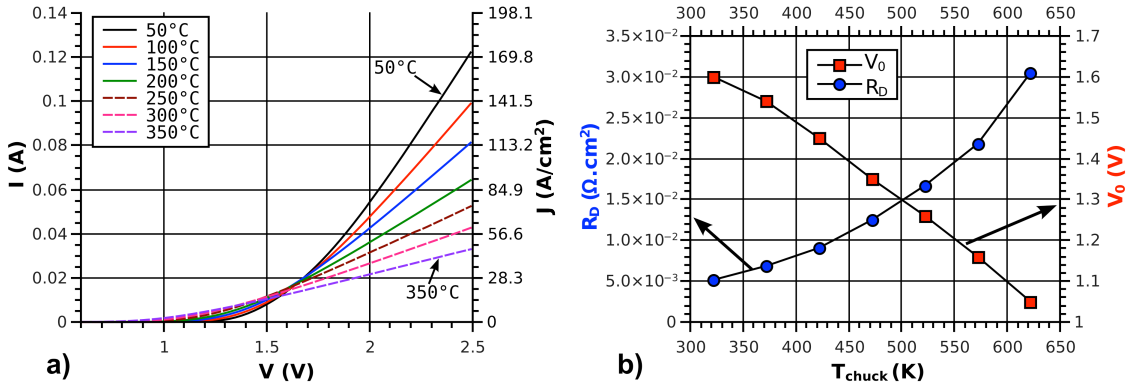


Figure 4: a) Current voltage measurement in temperature (I-V-T) of a typical diode – b) Evolution of the threshold voltage (V_0) and the differential resistance (R_D) extracted from I-V-T behaviors as a function of the measurement temperature.

Surprisingly, both of these figures clearly exhibit the intersection of I-V-T characteristics with an increase of R_D and a decrease of V_0 when the measurement temperature is increased. Such behaviors are typical of a thermionic current conduction where R_C mainly depends on the $N^-(\text{epi}) + N^+(\text{substrate})$ material resistivity and V_0 depends on the Schottky barrier height. Moreover, fitting the forward I-V characteristics by following the thermionic emission theory at room temperature of diodes from all as-grown samples generates Schottky Barrier Height (Φ_b) and ideality factor (n) values in the range $1.16 < \Phi_b < 1.35$ eV and $1.54 < n < 1.8$ respectively.

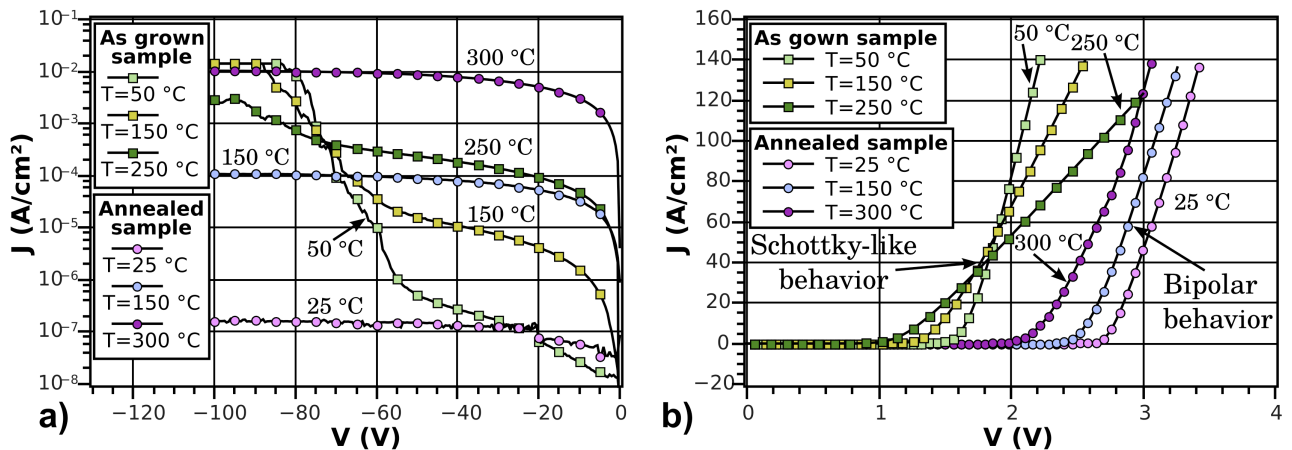


Figure 5: Effect of the high temperature annealing on the J-V-T behaviors of the VLS diodes. a) reverse polarization - b) forward polarization.

Different hypotheses can be held to explain these results. First, the grown material could be not a 4H-SiC layer. However, our previous studies clearly demonstrated the formation of a step bunched epitaxial 4H-SiC P^{++} layer with these growth conditions [2]. Another hypothesis could be that the phase in contact with the N^- layer is not 4H-SiC (for instance Al_4C_3) but in this case, it is difficult to understand how epitaxial SiC could grow on top of any foreign material. Finally the last hypothesis could be that the epi-VLS / epi-CVD interface contain a lot of crystalline defects which render the

P-N junction “non-abrupt”. It was already shown that such kind of defects was already observed after standard (non SEG) VLS growth of a P⁺⁺ layer on an N⁺ 4H-SiC substrate [3].

Assuming that last hypothesis is correct, a high temperature annealing could improve the crystalline quality of the interface. Fig. 5 shows the J-V-T characteristics on forward and reverse polarization of typical diodes before and after high temperature annealing. As expected, forward J-V-T characteristics of as grown diodes have the same Schottky-like behavior as previously seen with comparable V₀ values and the rapid increase of the leakage current for V > 50 V. In the contrary, after a high temperature annealing, the J-V-T characteristics are definitely different. Indeed, the forward ones are parallel one to each other. These results tend to confirm a bipolar conduction with a decrease of V₀ and a stagnation of R_D with the increase of the measurement temperature. Moreover, in this case the V₀ value found at room temperature increases to a more classical one, V₀ = 2.85 V, which is in agreement with a 4H-SiC P-N junction.

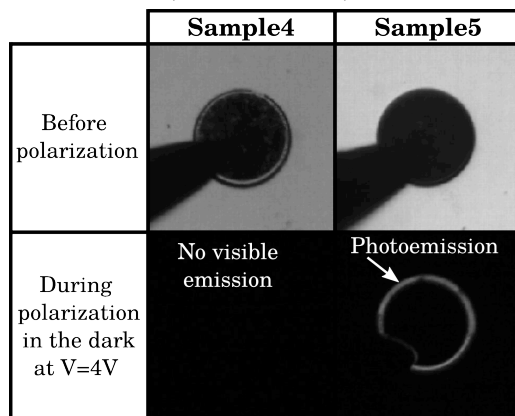


Figure 6: Observation of the electro-luminescence on forward bias at 4 V of two typical diodes from as grown sample and annealed sample.

In order to confirm the bipolar conduction of these annealed diodes, we compared their photoemission with the one of as-grown diodes at a forward voltage of 4 V. Fig. 6 shows clearly that there is photoemission for the annealed diodes whereas there is no visible emission without the annealing. These observations tend to demonstrate the carriers injection for the annealed sample and confirm the bipolar conduction mode.

Conclusion

In conclusion, our studies demonstrate for the first time that SEG by VLS transport of P⁺⁺ epilayer can provide a high quality P-N junction on 4H-SiC. An annealing at a high temperature is required to get the best quality and properties. This work also demonstrates that the SEG by VLS transport of P⁺⁺ epilayer technique opens new perspectives of technological design of devices such as guard rings peripheral protection, JBS rectifier or others structures with buried layers.

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