



**HAL**  
open science

## Power Cycling Test of PCB-Embedded Power Packaging

Mounira Bouarroudj, Said Bensebaa, Mickael Petit, Stéphane Lefebvre

### ► To cite this version:

Mounira Bouarroudj, Said Bensebaa, Mickael Petit, Stéphane Lefebvre. Power Cycling Test of PCB-Embedded Power Packaging. PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, May 2023, Nuremberg, Germany. <10.30420/566091124>. <hal-04364495>

**HAL Id: hal-04364495**

**<https://hal.science/hal-04364495v1>**

Submitted on 11 Mar 2025

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire HAL, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

# Power Cycling Test of PCB-Embedded Power Packaging

Mounira Bouarroudj<sup>1,2</sup>, Said Bensebaa<sup>2</sup>, Mickaël Petit<sup>2</sup>, Stéphane Lefebvre<sup>2</sup>

<sup>1</sup> Université Paris Est Créteil UPEC, France.

<sup>2</sup> SATIE, École normale supérieure Paris-Saclay, CNRS, UCP, CNAM, France

Corresponding author: Mounira Bouarroudj, mounira.bouarroudj@universite-paris-saclay.fr

Speaker: Mickael Petit

## Abstract

Power cycling test is the major reliability test method of conventional power modules due to temperature stress. In recent years new packaging technologies based on embedding active dies on the Printed Circuit Boards (PCB) are proposed. However, the reliability of these new technologies must be assessed. In this paper, experimental investigations on the already proposed solderless packaging in which connections are made using a pressed metal foam are presented. To assess the later packaging reliability, the devices have been subjected to power cycling conditions. Failure analysis have been made revealing degradations in the PCB interfaces.

## 1 Introduction

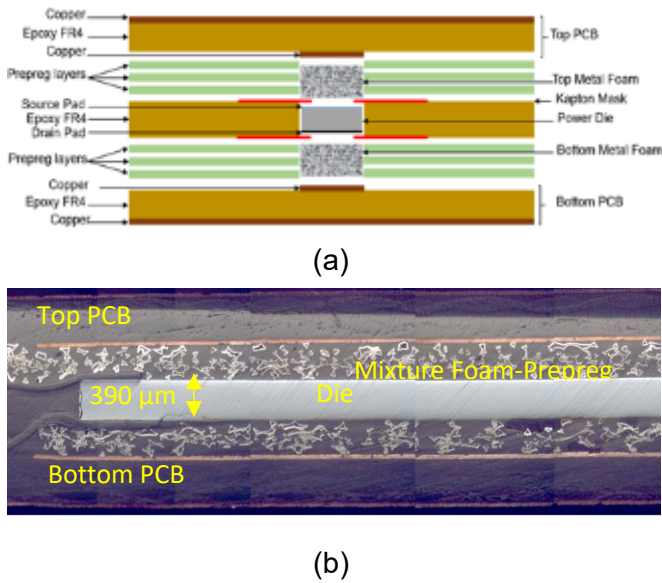
Printed Circuit Board (PCB) embedded technology is very attractive for power electronic converters especially those based on wide gap components. This technology allows high density integration and miniaturization of the devices with a drastic reduction of parasitic inductances [1][2]. Several contact process adapted to PCB-embedded technology have been developed [3]. The most conventional one is based on the use of micro-vias to ensure the electrical contact at the top of the active die when the bottom is soldered on the substrate or by microvia at double side. The manufacturing process of this technology requires advanced/industrial equipment as microvias are formed by laser processing. Some innovative solutions have been proposed mainly by academic laboratories such as that using double side sintering technology [4] or the use of laminated foam metal for ensure the electrical contact of the active die. The reliability of the proposed devices is investigated by applying thermal stresses under passive or active cycling. The obtained results revealed delamination at the solder joints for assemblies where the chip is soldered to the substrate and cracks in the micro-vias. In some studies, the tests are stopped without any failure being observed. Power cycling test is one of the major methods used to study the reliability performance and evaluate lifetime of power converters with respect to the temperature

stresses. In this paper we propose accelerated ageing tests to determine the failures due to thermomechanical stresses caused by power dissipation in the chip.

## 2 Samples preparation

The test devices are proposed PCB-Embedded diodes with solderless packaging [5]. In line with characterization studies, power diodes connection have been provided by metal nickel foam at the top side and copper foam for the back side [6]. Devices under test have been manufactured according to dedicated manufacturing process where the different material layers (bottom PCB, Prepreg, bottom foam, die, top foam, prepreg, top PCB) were stacked and laminated under specified pressure along the z-axis and temperature conditions (LPKF MultiPress S). Obtained packaging is depicted in Fig. 1.

In this study four devices have been tested under the same conditions.

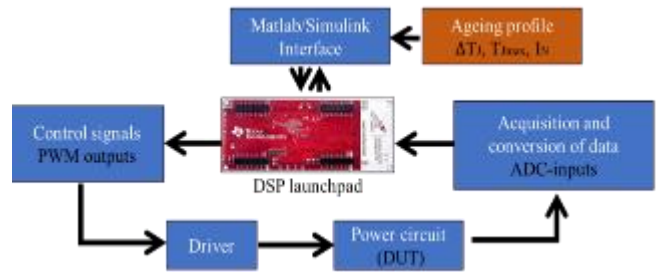


**Fig. 1** (a) Sample stacking before pressing (b) Microscopic section view of an embedded die.

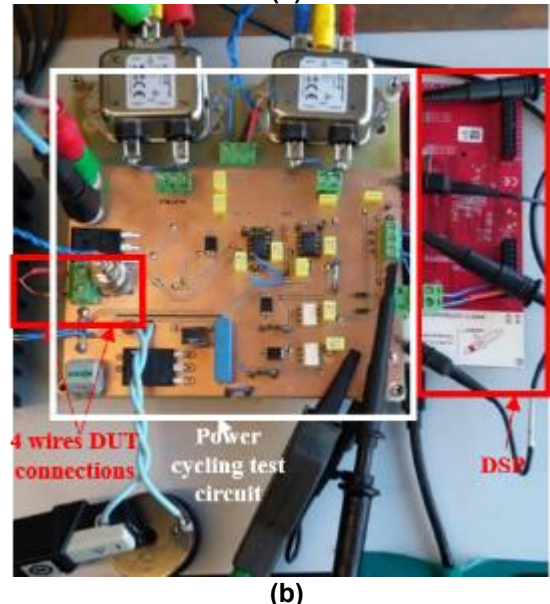
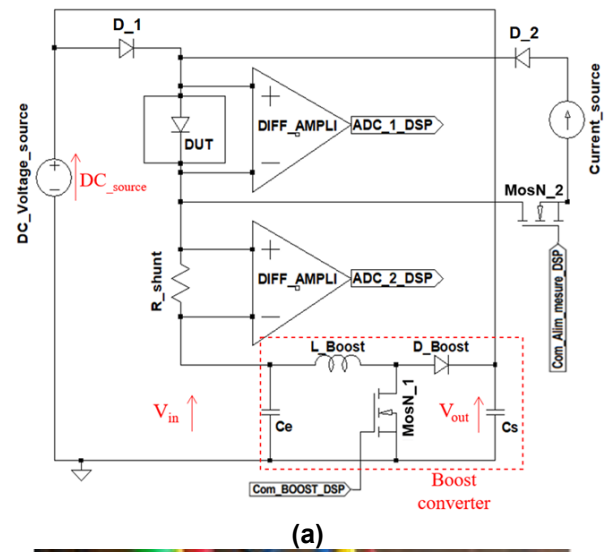
### 3 Power cycling test bench

#### 3.1 Test bench description

Dedicated PWM power cycling test bench has been developed to perform accelerated ageing under thermal constraints. As shown in Fig. 2 it is composed of a digital signal processor DSP (LAUNCHXL-F28379D) which allows both generating the control signals through the driver and acquiring the various measurements during ageing tests (current and voltage) by its internal ADC (Analog-to-Digital Converter). The communication with the DSP is done through Matlab/Simulink® software. Two modes of communication and data transmission between MATLAB/Simulink and the DSP microcontroller coexist. The first mode (Internal mode) allows to implement a program in the microcontroller which will be executed autonomously. The second mode (called: External mode) allows to modify in real time the program under execution. The DSP compares the setpoints and measurements and generates the control signals that are used to control the drivers, which in turn control the power circuit. The power circuit is shown in Fig. 3.



**Fig. 2** Synoptic scheme of the developed power cycling test bench



**Fig. 3** Proposed PWM power cycling test

A Boost converter is used to control the average DC current thanks to the duty cycle (from 0.11 to 99.9%) and control the amplitude of current ripples through its inductance and switching frequency until 5 kHz. In order to minimize losses, the Boost output voltage  $V_{out}$  is connected to the DC voltage source. This bench can be used to measure the junction temperature by two methods. The first by using the on-state voltage at low current injected just after the power current injection (up to 100mA) provided here by a precision current source. The second method is based on the use of current ripples and allows the on-line temperature to be measured during the warm-up phase. This latter method requires a high precise and accurate instrument with a very low acquisition time [7].

Two differential amplifiers are inserted, the first one allows to measure the voltage at the DUT terminals and the second one allows measuring the image of the forward current through a shunt resistor. The outputs of these two amplifiers are directly connected to the ADC inputs.

### 3.2 Test conditions

The test conditions target are as follows:  $\Delta T_j = 50^\circ\text{C}$ ,  $t_{on} = 1\text{ s}$ ,  $t_{off} = 2\text{ s}$ . These conditions were reached with a DC current value of 18A. The DC-bus voltage was 12 V. The DUT is fixed to an air cooler via a TIM thermal interface and then placed in a thermal chamber with controlled ambient temperature  $T_{amb} = 25^\circ\text{C}$ .

#### 3.2.1 Thermosensitive parameter (TSEP)

As mentioned above, the junction temperature ( $T_j$ ) was measured by an indirect method based on the the threshold voltage as a thermo-sensitive parameter (TSEP). As illustrated on Fig. 4, during the measurement phase, the current through the DUT is taken only from the precision supply ( $I_m$ ) and the power current  $I_F$  is reset to zero.

In Fig. 5 is depicted the dependence of the  $V_F$  with temperature between  $8^\circ\text{C}$  and  $65^\circ\text{C}$  and measurement current  $I_m$  until 100mA.

#### 3.2.2 Aging indicators

In the studied assembly, the areas subject to degradation with ageing are the electrical connections. So, the electrical on-state resistance  $R_s$  was used as an indicator of ageing.  $R_s$  was measured after 1k, 2k, 5k, 10k cycles. Then every 10k cycles until failure.

If a failure appears, an analysis by microsection is realized in order to understand its origins.

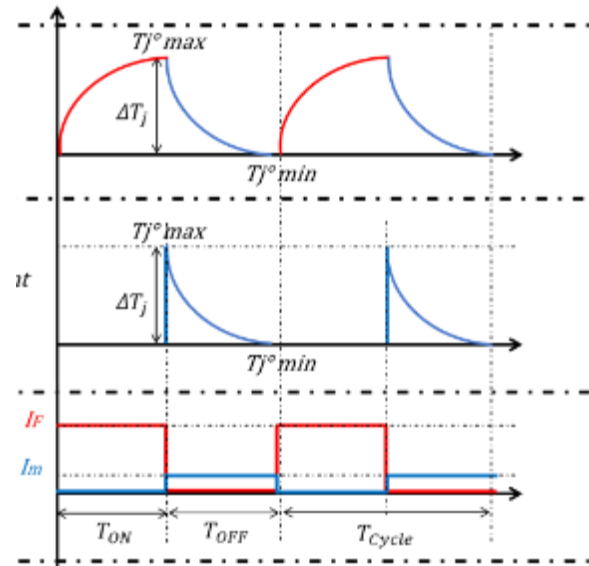
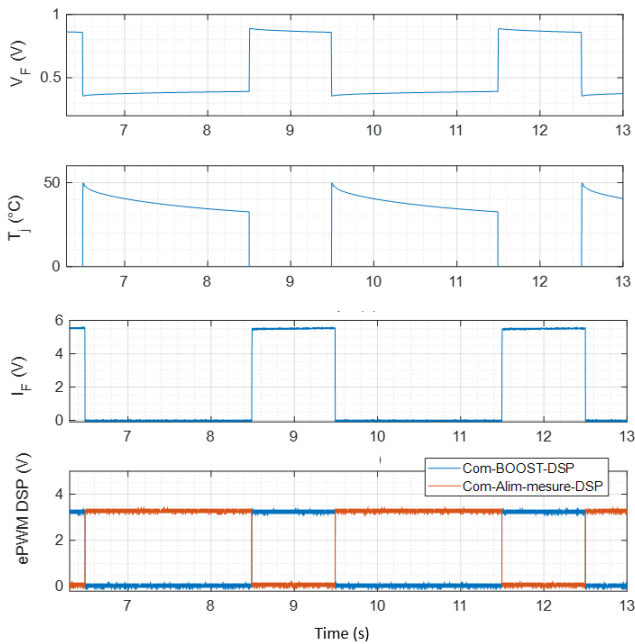


Fig. 4: Theoretical curves showing the currents ( $I_F$  and  $I_m$ ) injected into the DUT, and the range where the temperature is estimated.

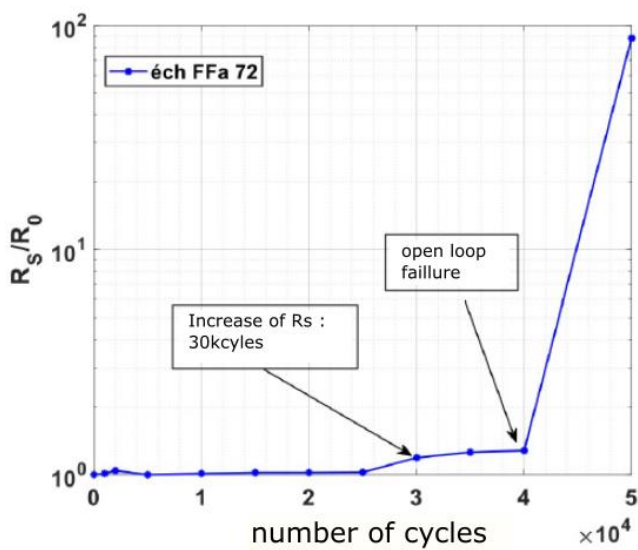
## 4 Power cycling test results

As described in paragraph 3.2, the obtained junction temperature varied between  $\Delta T_j = 50^\circ\text{C}$  and  $55^\circ\text{C}$  with a heating phase ( $t_{ON}$ ) of 1 s and cooling phase ( $t_{OFF}$ ) of 2 s. The duty cycle value was fixed to (35%) and switching frequency to 5 Hz leading the temperature reaching its minimum value during the cooling phase. The estimated dissipated power losses during this period was approximately 4.7 W. These losses are required to reach the targeted  $\Delta T_j$ . The power cycling strategy used here is constant load current. This type of strategy is considered as the most severe because it is expected that degradations in the device will result in an increase of  $\Delta T_j$  with no compensation in the control. Only one device has failed after 44k cycles by open-circuit. For this last, the evolution of the normalized electrical resistance and maximal temperature are shown as a function of the number of thermal cycles in Fig.2. Indeed, during the 25 first kcycles the resistance does not increase. Between 25k and 40k the resistance increases by 20 %, and continues to increase until the failure occurs at 44k. The evolution of the electrical resistance is consistent with the increase of the junction temperature, Fig 7. The maximum junction temperature increased also during ageing, due to the increase of the electrical resistance of the packaging. It reaches  $160^\circ\text{C}$  in the last 1000 cycles before failure and exceeds the glass transition temperature of the epoxy ( $T_g = 140^\circ\text{C}$  [5]).



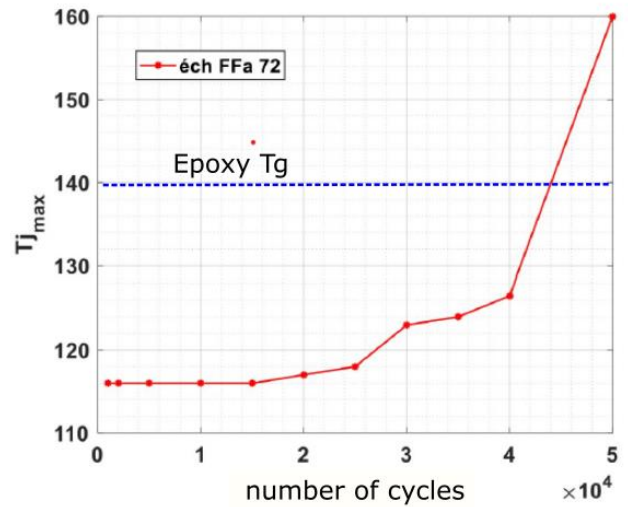
**Fig. 5:** Measurements of the direct voltage  $V_F$ , the current  $I_F$ , the junction temperature  $T_j$ , and the control signals from the DSP during power thermal cycling

As the temperature increases, the epoxy resin expands. As a result, the number of electrical contact points between the copper of the PCB and the metal foam, as well as between the metal foam and the chip, decreases, causing thermal runaway. As soon as the temperature of the PCB exceeds the glass transition temperature, the expansion of the epoxy resin is sufficient to lose all the contact points. The stack then becomes an open circuit. The stresses became crucial at the interconnections, inducing the failure of the device.



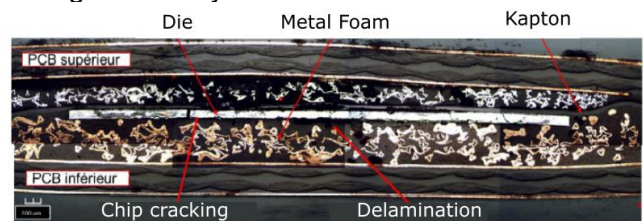
**Fig. 6:** Evolution of the normalized resistance of

package with thermal cycles. Only the failed sample is shown



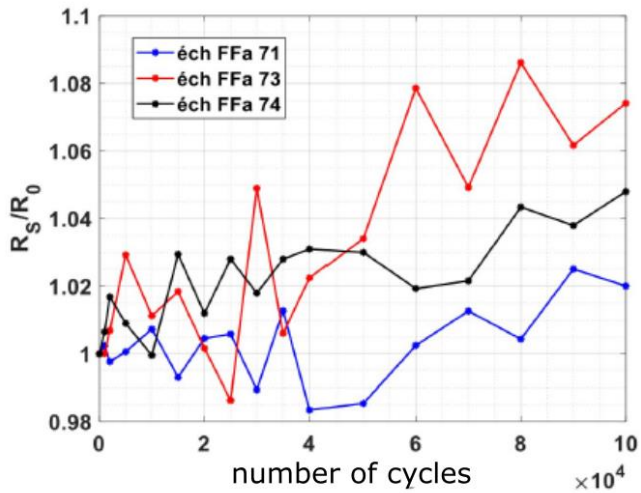
**Fig 7:** Evolution of  $T_{jmax}$  of the failed package with thermal cycle.

Figure 8, shows a metallographic section observed with an optical microscope of the sample that has failed. The failure manifests itself as both a disbonding of the interfaces between the chip and the metal foam and a fracture of the chip. The latter proves the presence of a significant stress during the last cycles.



**Fig 8:** Metallographic section of the failed sample

The other three samples remain operational after 100kcycles. Figure 9 shows that the on-state resistance of the stacking does not exceed 8% after 100kcycles



**Fig. 9:** Evolution of the normalized resistance of still functional samples

## 5 Conclusion and Outlook

A test bench adapted to printed circuit boards integrating active components has been developed. The active components chosen are diodes whose electrical connection is ensured by a Nickel metal foam.

The active cycling protocol is based on a heating and cooling cycle of the assembly by periodic current injection. The intensity and time of heating and cooling are kept constant.

Of the four samples tested, only one shows an open circuit failure before 50kcycles. This failure is due to an increase in package resistance causing an increase in temperature. The failure occurs when the temperature exceeds the glass transition temperature of the substrate.

A metallographic analysis shows the appearance of foam delamination and cracking of the chip. The use of a higher Tg substrate (e.g. polyimide) would delay the failure.

On the three still healthy samples, their resistance increases with cycling but does not exceed 8% at 100kcycles. This is comparable to the modules integrating solder and bonding classically used in power electronics.

A passive aging campaign has already been carried out showing results close to the literature. The next step of our work will be to simultaneously combine active and passive cycling on these assemblies

## 6 Reference

- [1] A. P. and B. M. J. . -P. Sommer, T. Hofmann, A. Neumann, "Highly Integrated Advanced Power Electronic Systems for Automotive Applications," 2010.
- [2] G. Regnat, P. O. Jeannin, D. Frey, J. Ewanchuk, S. V. Mollov, and J. P. Ferrieux, "Optimized Power Modules for Silicon Carbide mosfet," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1634–1644, 2018, doi: 10.1109/TIA.2017.2784802.
- [3] T. Huesgen, "Printed circuit board embedded power semiconductors: A technology review," *Power Electron. Devices Components*, vol. 3, no. July, p. 100017, 2022, doi: 10.1016/j.pedc.2022.100017.
- [4] G. Feix, E. Hoene, O. Zeiter, and K. Pedersen, "Embedded very fast switching module for SiC Power MOSFETs," *PCIM Eur. 2015; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag. Proc.*, no. May, pp. 19–21, 2015.
- [5] S. Bensebaa, M. Berkani, S. Lefebvre, M. Petit, N. Schmitt, and S. Zhang, "Reliability study of PCB-embedded power dies using solderless pressed metal foam," *Microelectron. Reliab.*, vol. 114, no. May, p. 113904, 2020, doi: 10.1016/j.microrel.2020.113904.
- [6] S. Bensebaa, M. Berkani, S. Lefebvre, M. Petit, and N. Schmitt, "Experimental and Numerical Characterization of PCB-Embedded Power Dies Using Solderless Pressed Metal Foam," *2020 22nd Eur. Conf. Power Electron. Appl. EPE 2020 ECCE Eur.*, pp. 1–10, 2020, doi: 10.23919/EPE20ECCEurope43536.2020.9215758.
- [7] S. Bensebaa, M. Berkani, M. Petit, and S. Lefebvre, "On-line temperature measurement during power cycle of PCB-embedded diode," *Microelectron. Reliab.*, vol. 126, no. July, p. 114313, 2021, doi: 10.1016/j.microrel.2021.114313.