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# P-type SiC layers formed by VLS induced selective epitaxial growth

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**Abstract.** Al-Si patterns were formed on n-type 4H-SiC substrate by a photolithographic process including wet Al etching and Si/SiC RIE process. RF 1000°C annealing under C<sub>3</sub>H<sub>8</sub> flow was performed to form p<sup>+</sup> SiC layers by VLS process. This method enables to grow layers with different size (up to 800 μm) and various shapes of pattern. Nevertheless the remaining Al-based droplets on the largest patterns are indicators of cracks defects formation, going through the p<sup>+</sup> layer down to the substrate. SIMS analyses have shown Al profile with high doping concentration in surface, high N compensation and Si/C stoichiometry variation between the substrate and the VLS layer. The hydrogen profile shape follows the one of Al in the VLS layer with an overshoot at the VLS/substrate interface. I-V measurements performed directly on the semiconductor layers have confirmed the formed p-n junction and have allowed to measure a sheet resistance of 5.5 kΩ/□.

## Introduction

Unipolar SiC devices like Schottky diodes, MESFET and JFET are already or will be soon commercialized. Different universities or industrial research teams have published a non-negligible number of bipolar device demonstrators in SiC. And thus large efforts were mainly targeted in increasing the breakdown voltage. Results on 19.5kV bipolar diodes were published [1].

In spite of that, the development of SiC bipolar devices is slowed down due to the low currents that are obtained in forward polarization. This is due firstly to the material quality which limits the device area and secondly to the high resistances of the p-type SiC layers and the ohmic contacts on these layers. Diminishing the p-type SiC layers resistance is difficult by classical process due to the solubility limit of dopants during the CVD epitaxy [2] and/or the material degradation by ion implantation at high doses. Partial material recovery and dopant activation are obtained after high temperature post-implantation annealing (1700 – 1800°C) [3].

In this paper we present SiC p-type material selectively grown at relatively low temperature process by Vapour-Liquid-Solid (VLS) process.

## Experiment

The unique configuration of the VLS process, where only carbon is brought by the gas phase, allows to grow SiC only where the seed is covered by the Al-Si melt. Using the same procedure as in reference [4], a n-type 8° off-axis 4H-SiC substrate is covered by controlled thickness Al-Si bilayer stacking, 1 μm of Si by CVD at 1000°C under silane followed by 2 μm of Al deposited by sputtering. Photoresist was deposited on the sample and Al patterns were defined by photolithography and subsequent Al wet etching. Using the formed Al mask, RIE (Reactive Ion Etching) was performed to locally remove the Si and SiC up to 4 μm in the substrate by using a SF<sub>6</sub>-O<sub>2</sub> plasma with 250W power and 60mTorr pressure.

The sample as prepared is heated up to 1000°C in a cold wall RF reactor on a graphite susceptor under 5 slm Ar. Propane is then flowed in the reactor and reacts with the local Al-Si melt formed by

the Al/Si patterns. Al-doped SiC layers are thus grown selectively at the places where the liquid is present. Note that the initial Al/Si thickness ratio corresponds to a molar ratio of 70/30.

Secondary Ion Mass Spectroscopy (SIMS) measurements were performed on this samples with a CAMECA IMS4F using an  $O^{2+}$  primary ion beam with an energy of 10 or 12 keV and a current around 500 nA. These measurements were carried out in order to determine the  $^{27}Al$  doping profile.

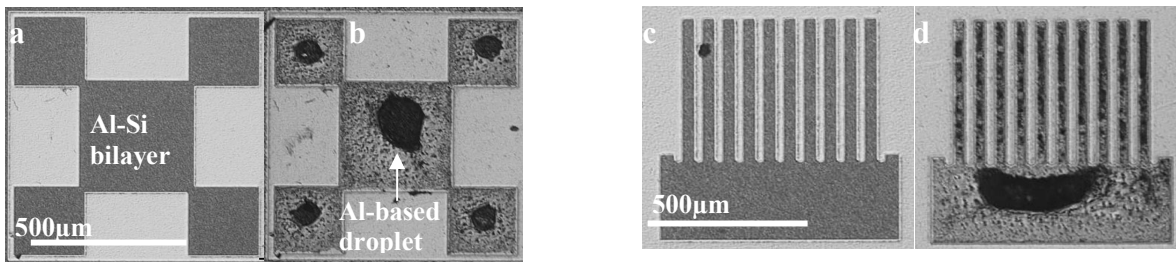
The intensity of the secondary ion beam was converted into dopant concentration, by comparing with SIMS analyses of a reference sample with a known Al dopant profile, in the same concentration range. Depth of the craters is measured with a profilometer.

To take into account the possible variations in the ion collecting between two analyses, it was measured in each sample a reference ion signal beam corresponding to one element of the target. The target ion reference is chosen according to the Al level to detect. When the Al concentration is high, the aperture of the SIMS set-up is closed to the maximum because the ionization yield is very high. The ion of reference is selected between  $^{30}Si$  or  $^{12}C$ .

In order to detect the interface - junction formation, to understand the stoichiometric evolution, precipitation, contamination or diffusion phenomena besides the target ions spectra, qualitatively (only calibrated in the depth) SIMS profiles were also obtained for  $^{14}N$ ,  $^{11}B$  or  $^1H$ .

Electrical I-V measurements were performed on these layers formed by VLS with a Keithley 2410 SMU, in vertical configuration to check the insulation of the epitaxial layer from the n-type substrate, and in horizontal configuration to estimate the sheet resistance of these layers.

## Results and discussions

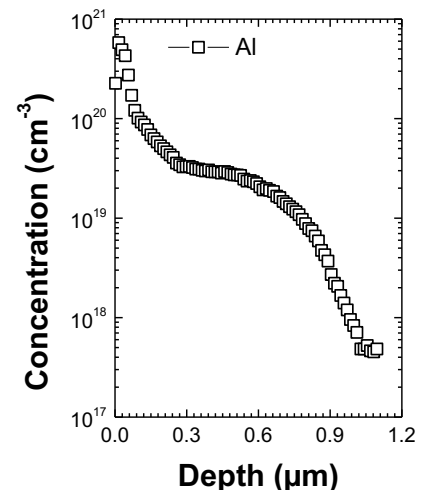


*Figure 1 : Illustration of the selective growth using VLS process for two different patterns: a) and c) before the growth, b) and d) after the growth. The white scale corresponds to 500 μm.*

Results of selective growth by VLS are presented in the figure 1. Micrographie pictures in figure 1a and 1c show the stacking layer structures Al/Si/SiC before the VLS growth and fabricated by the Al and Si/SiC wet and dry RIE etching respectively.

In figure 1b and 1d the same structures are presented after the VLS growth. It is clear that this method enables to grow layers with different size (up to 800 μm) and various shapes of pattern. For larger patterns, it would be necessary to increase the Al/Si bilayer thickness in order to avoid dewetting upon melting. There is however a risk to decrease the patterns definition resolution limits. VLS devices have to be designed taking into account this aspect.

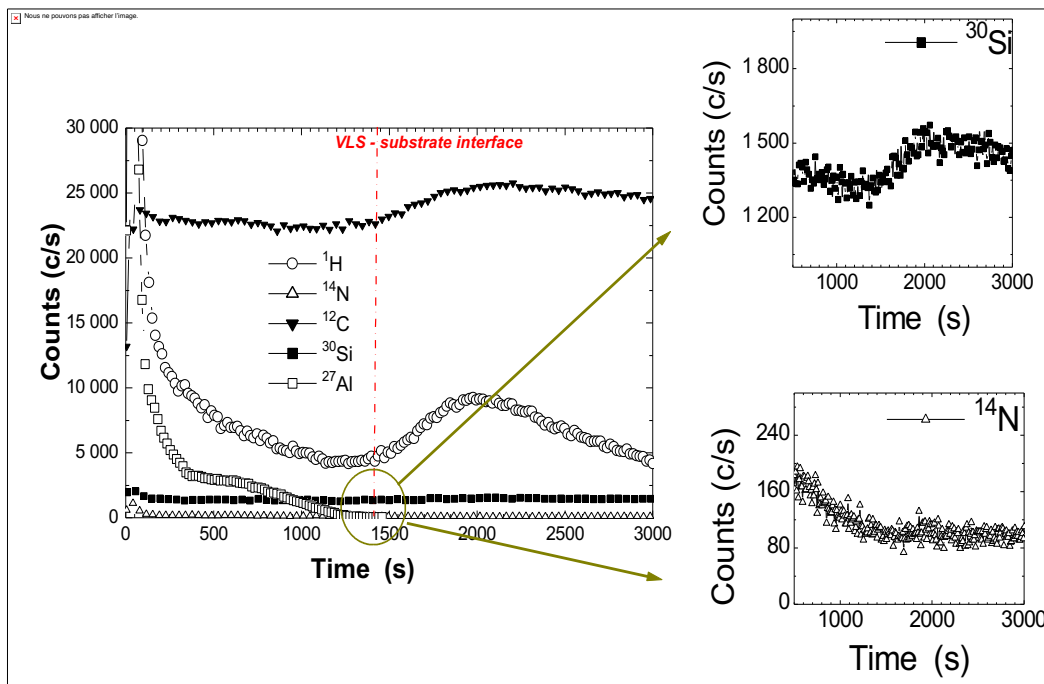
Nevertheless we have to note the remaining Al-based droplets on the largest patterns. After the removing of the remaining Al and Si (by wet etching in HF/HNO<sub>3</sub>/HCl solution), some cracks were sometimes found, going through the p-doped layer down to the substrate. We believe that these cracks come from thermal mismatch stress with the solidified remaining melt. This could



*Figure 2 : Al doping profile in semi-logarithmic scale*

be avoided by performing an annealing at the end of the growth to evaporate the Al excess before cooling.

Figure 2 and 3 set SIMS spectra obtained in the VLS grown layers. The Al profile calibrated in depth and concentration (figure 2) presents a very high concentration in surface ( $4$  to  $5 \times 10^{20} \text{ cm}^{-3}$ ) in the first  $40 \text{ nm}$ , decreases to a plateau of  $3 \times 10^{19} \text{ cm}^{-3}$  and finally falls at the interface between the VLS layer and the substrate. This decrease of the Al concentration could be related to the Si content impoverishment during VLS growth as the initial amount of Si is limited.



*Figure 3: SIMS spectra in linear scale with the evolution of  $^{12}\text{C}$ ,  $^{30}\text{Si}$ ,  $^{14}\text{N}$ ,  $^1\text{H}$  and  $^{27}\text{Al}$  profiles. The inserts show the  $^{30}\text{Si}$  and  $^{14}\text{N}$  profiles at the epilayer/substrate interface.*

The interface between the VLS layer and the substrate is also clearly showed by the evolution of  $^{12}\text{C}$ ,  $^{30}\text{Si}$ ,  $^{14}\text{N}$  or  $^1\text{H}$  profiles. The two firsts increase simultaneously before to reach a constant plateau revealing a difference between the epitaxial VLS layer and the substrate stoichiometry.

The  $^{14}\text{N}$  decreases indicating a higher N concentration in the epitaxial VLS layer, about 2 times compared to the substrate one. This concentration remains low compared to the Al doping in surface, but it generates a high compensation level in the VLS formed layers. We have to remark that the SIMS analyses performed with an  $\text{O}^{2+}$  primary ion beam do not allow us to accurately obtain the concentration of nitrogen, our estimation remaining qualitative.

The hydrogen profile shape follows the one of Al in the VLS layer with an overshoot at the interface. The hydrogen incorporation seems to be related to the Al one, maybe the formation of Al-H bonds. The interface overshoot on the hydrogen profile shows the probable presence of H-related complexes formed at the interface (correlated with the stoichiometric Si/C yield evolution between the VLS layer and the substrate) which may influence the electrical characteristics of the different layers and the formed junction injection.

I-V measurements are shown in Figure 4. These were performed directly on the VLS grown layers, without additional metallization to form ohmic contacts. In fact this technological step was difficult due to the cracks formed in the VLS layers. Short-circuit between the VLS layers and the substrate may not be avoided.

In vertical mode (tips are put on the VLS layer and on the support chuck – see figure 4a) a rectifier behavior is found with a threshold voltage of  $\sim 2\text{V}$  in forward bias. The p-n junction is so confirmed and thus the p-type layer may be electrically analyzed.

In lateral mode (the two tips are put on the VLS layer – see figure 4b) the almost linear current versus voltage variation shows ohmic contact behavior between the tips (tungsten carbide) and the p-type SiC. We remark the low level of the current, which is typical for semiconductor behavior of the p-type SiC layers. To estimate the sheet resistance of the p-type SiC layers, four – points I-V measurements were performed on Van-der-Paw structures. The sheet resistance found was  $5.5 \text{ k}\Omega/\square$  which represents a promising result compared to those obtained on ion implantation layers [5]. The square resistance is still high due to the Al concentration decrease from the surface to the interface (Figure2). The calculated sheet resistance with this Al profile is about  $3.5 \text{ k}\Omega/\square$ , the difference between these two values being furthermore due to the nitrogen compensation that was not taken into account. These results show that well activated p-type layers (high Si substitutional yield for the Al dopants) were obtained in spite of the low temperature process ( $1000^\circ\text{C}$ ). On the other hand, thanks to the higher Al level at the surface, no difficulty was encountered to take the contact.

Typical p-type SiC layers have been so obtained by a selective VLS growth, with a particular high doped region in surface that may be an important issue in bipolar devices development. Thus the ohmic contacts may be improved besides the utilization of relatively low Al doped p-type SiC layers.

Nevertheless the still incompatibility found between the VLS growth and the classical bipolar power devices fabrication shows that the VLS technique have to be improved to avoid the crack formation in the large p-type formed layers or the device geometry has to be adapted to this VLS technology.

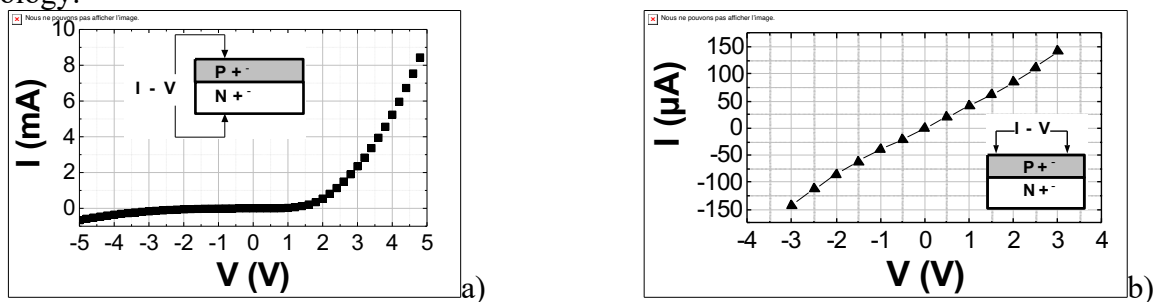


Figure 4 : I – V measurements performed on the VLS formed layers in vertical (a) and lateral configuration (b), tips are applied directly on the semiconductor layers.

## Summary

P<sup>+</sup>-type SiC layers with different size and various shapes of pattern, have been obtained by VLS selective process growth on a n-type substrate. Al profile, the N compensation and Si/C stoichiometry variation between the substrate and the VLS layer, have been analyzed by SIMS.  $5.5 \text{ k}\Omega/\square$  sheet resistance were measured by I-V with tips directly on the semiconductors thanks to the high Al concentration in surface. Well activated Al doped layers are so obtained in spite of a relative low temperature process. These layers are very promising to obtain bipolar devices with low p-type sheet and contact resistances, but the VLS technique should be improved to avoid the short-circuit by the defect cracks formation or to adapt the device structures to the VLS method.

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