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Graded Etched Junction Termination for SiC Thyristors

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Abstract. In this paper, we propose a graded etched junction termination extension which has the functionality of a multiple implanted junction termination extension, but is realized by purely etched means. This termination is demonstrated up to 4 kV on a sample with a drift layer of 35 μm . On another sample with a thinner drift layer, a low resistive contact could be realized, resulting in an on-state voltage drop of 3.2 V at 40 A/cm².

Introduction

Silicon carbide (SiC) thyristors are of specific interest for high power and especially for pulsed power applications [1, 2]. One of the critical design and fabrication aspects is the termination. To reach high blocking voltages, nowadays, an implanted junction termination extension (JTE) is commonly used [2, 3]. The ion implantation and following high temperature annealing process can cause crystal damage and surface roughness, respectively, which affect the performance of the fabricated devices. Etched terminations are therefore an attractive alternative. Moreover, etched terminations are less laborious, less cost-intensive and are a proven type of termination in silicon technology. One possible termination is a simple etched JTE, which was shown for SiC BJT's in [4]. Such a single step termination suffers from a high sensitivity to the optimum etching depth. Using a graded etched (GE) JTE, which we proposed and simulated in [5], this sensitivity is significantly reduced. A two step etched JTE was shown in [6] for SiC diodes. In this paper we present SiC GTO thyristors terminated by a three step GEJTE for the first time. By way of introduction, some design aspects and the fabrication steps will be detailed. Then, the electric behaviour is presented and discussed. To our knowledge, this is the first time that an etched JTE is demonstrated for SiC thyristors.

Design and fabrication

For economic reasons, 1 x 1 cm² samples are used. In this paper, results of three thyristor samples with two different epitaxial structures are presented (see Tab. 1). Sample one and three have a GEJTE and annealed contacts, sample two has a mesa termination and non annealed contacts. As shown in Fig. 1, up to 36 thyristors with a size of 9.9 x 10⁻³ cm² (with termination) are realized on a 1 x 1 cm² sample.

Table 1: Overview of the three samples under investigation.

sample	W_{drift}	termination	h_1	h_2	h_3	h_{mesa}	$V_{\text{br max.}}$
01	35 μm	GEJTE	1.2 μm	0.5 μm	0.5 μm	4.9 μm	5.5 kV
02	35 μm	mesa	1.3 μm			4.8 μm	1.2 kV
03	10 μm	GEJTE	3.1 μm	0.55 μm	0.55 μm	2.8 μm	80 V

Termination. The graded etched JTE is based on the idea that a remaining thin layer of the upper n-type gate layer (see Fig. 2) can replace an ion implanted JTE. The dose is given by the height and the doping of such a thin layer. In case of the graded etched JTE this remaining layer is etched stepwise, slightly increasing the dose from the outside to the inside. The advantage is that the height of each step is not critical, the mean value is important. The optimal dose can be approached even with a relatively high uncertainty concerning the step height, the n layer thickness or its doping concentration.

Simulation results of the GEJTE are shown in Fig. 3. The first step is set constant to $h_1=1.5 \mu\text{m}$. The step heights h_2 and h_3 are varied between 0.25 (0.3) and 0.7 μm . For this range, the efficiency of the GEJTE is over 90%, as long as the two varied steps are at least 0.3 μm high. In case of a single step JTE, a variation of 400 nm from the optimal height results in a breakdown voltage drop of at least 30% [5]. The limitation of the GEJTE is given by the relation that the step high needs to be thinner with increasing doping concentration. For a doping concentration of 10^{18}cm^{-3} the remaining n layer thickness needs to be around 100 nm, this is hardly feasibly with our etching means since we observed an etching deep variation of up to 6%.

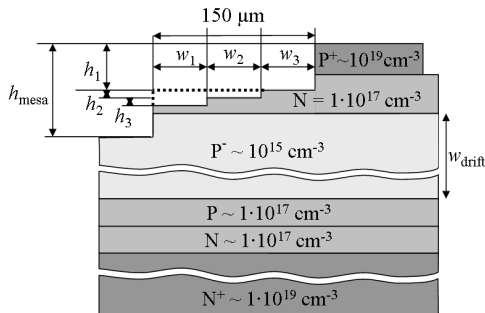
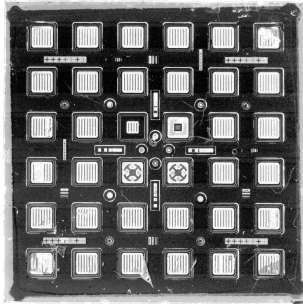


Figure 2: Schematic cross-section of the thyristors with graded etched JTE and mesa termination (dashed-line).

Figure 1: Micrograph of a $1 \times 1 \text{cm}^2$ SiC sample with 36 thyristors terminated by a graded etched JTE.

Epitaxial Structure. Fig. 2 shows the schematic cross-section of the thyristors on sample one and two. The common asymmetric blocking n^+ (substrate) $\text{p}^- \text{p}^- \text{n} \text{p}^+$ epitaxial structure was used. The forward breakdown voltage, simulated with the T-CAD program Sentaurus, is 5.74 kV. The highly doped anode layer ($\text{p}^+ \sim 10^{19} \text{cm}^{-3}$) is 1 μm and the gate layer ($\text{n} \sim 10^{17} \text{cm}^{-3}$) 2 μm thick. The epitaxial structure of sample three is symmetrically blocking with a breakdown voltage of about 80 V. The anode and gate layers have the same doping concentration as those of the two other samples, but are 2 and 3 μm thick, respectively.

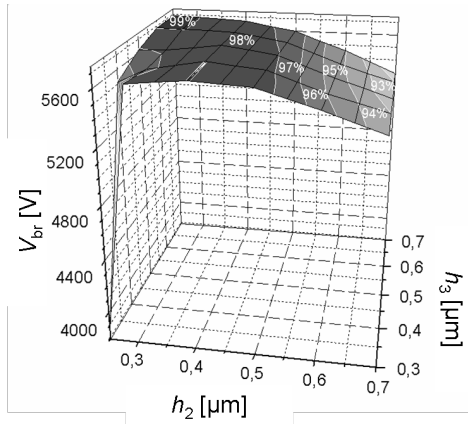


Figure 3: Simulation of the breakdown voltage for $h_1 = 1.5 \mu\text{m}$ (const.).

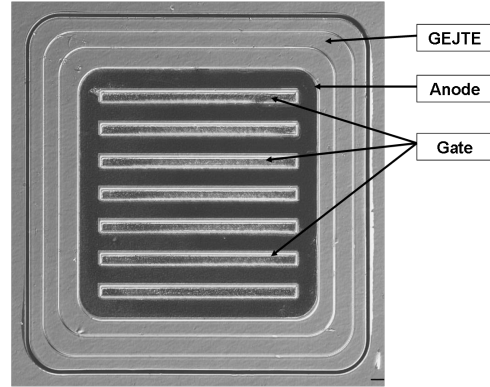


Figure 4: Micrograph of a 1 mm^2 SiC thyristor with a three step graded etched JTE.

Fabrication process. First, the anode was etched using a Ni mask. All etching processes were done by reactive ion etching (RIE). The interdigitated anode-gate structure that can be seen in Fig. 4 shall allow GTO behaviour. The three step GEJTE can be seen very well. The RIE of the steps was done with photo resist masks. Sample two, with mesa termination (compare Fig. 2), was etched together with the other two samples to attain the same total height h_{mesa} . The determined heights ($h_1 \dots h_3$) and the calculated maximal breakdown voltages are given in Tab 1. For sample one and three, the metallization of the contacts was deposited and annealed in two steps. For the contacts on n-type a Ni based and for the contacts on p-type an Al/Ti/Ni tri-layer was used. The main differences between these two samples are the metal order on the anode (p-type) and the over-metallization that was not done for sample one due to technological problems. For sample three, a second over-metallization layer is planned to interconnect the gate fingers on the one hand and allows large contact areas on the other hand.

Electric Characterization

For the evaluation of the termination, the blocking characteristic is shown first. Then, the on-state characteristic is presented to give an idea of the contact resistivity and the functionality of the realized thyristors.

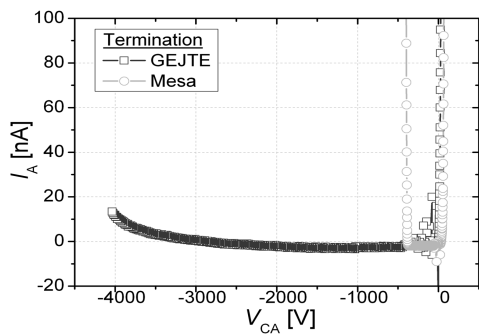


Figure 5: Forward and reverse blocking characteristic of asymmetrical SiC thyristors with GEJTE and mesa termination.

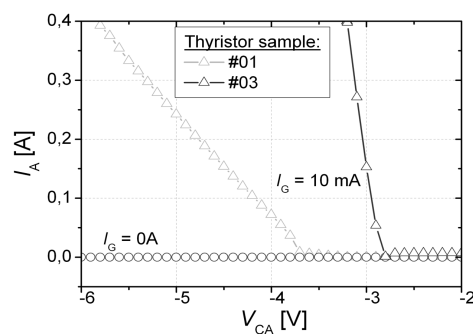


Figure 6: Typical on-state characteristics of SiC thyristors on two samples ($A = 0.01 \text{ cm}^2$).

Blocking Characteristics. High voltage characterization of the thyristors was performed in a vacuum probing chamber. This chamber allows measuring semiconductor devices on chip level up to 20 kV with a current resolution of less than 1 nA [7]. The forward and reverse blocking characteristics of the thyristor with the highest blocking capability on sample one and two are shown in Fig. 5. As expected, the highest blocking voltage of 4 kV was attained by a device with GEJTE. The characterization in forward blocking direction was not conducted to higher currents (20 nA) to avoid the destruction of the device. In the case of thyristors with mesa termination, the

highest measured breakdown voltage is 560 V. This value is clearly lower than the simulated one, because the bevel angle of the realized mesa was not taken into account. In accord with the expectations, several devices with GEJTE attained a significantly higher breakdown voltage compared to the ones with mesa termination. In reverse direction the breakdown voltage is below 80 V.

On-State Characteristics. Typical on-state characterizations for sample one and three are shown in Fig. 6. To switch the device on, in both cases, a gate current of 10 mA is applied. The high voltage drop of the thyristor on sample one, 5.8 V at 40 A/cm², can be explained by a missing over-metallization and a high resistive contact metallization. In contrast, the voltage drop on sample three is low, 3.2 V at 40 A/cm².

Conclusion

In conclusion, a graded etched JTE could be applied to silicon carbide thyristors for the first time. This termination has the advantage that it can be realized by simple technological means and that it is insensitive to process variations. Compared to an implanted JTE, this termination is less damaging, less expensive and should be at least as efficient. Compared to a simple mesa termination of the same height, a significantly higher breakdown voltage can be reached.

On one sample with a drift layer thickness of 35 μm, the realized devices showed a blocking capability of up to 4 kV, which corresponds to 73 % of the simulated breakdown voltage for the realized geometry. Since we used a sample from the border of the wafer, we assume that the blocking capability is not limited by the termination but by the actual drift layer thickness and doping concentration. A drift layer thickness of 26 μm was determined on another border sample of the same wafer using a scanning electron microscope (SEM). With this thickness, the breakdown voltage is calculated to 4.6 kV, which corresponds better to the attained breakdown values.

On another sample with a thin drift layer, the contact metallization could be tested and a low resistive contact could be realized. This contact metallization combined with the GEJTE termination will be applied on low defect material with a drift layer thickness of 100 μm in further works.

Acknowledgments

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