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A 3.5 kV thyristor in 4H-SiC with a JTE periphery

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Abstract :

Introduction :

Today, at ISL, there are pulsed power applications under investigation which handle electric energies up to 10 MJ using spark gaps or silicon based high power semiconductors as switching elements [1]. Since silicon based technology is reaching its physical limits concerning blocking and power handling capability, GTO thyristors based on SiC are under investigated for compact future pulsed power systems we are investigating [2]. Reaching breakdown voltages of 19 kV [3], the potential of SiC based devices appears very interesting. According to preparatory device simulations using the finite element code MEDICITM, the developed GTO-thyristors should be able to block voltages up to 6 kV. The models and parameters used by the simulator are described by Brosselard and al. in [4]. After a short introduction about structure and the operating mode of the thyristor in 4H-SiC, simulations will be presented on the peripheral protection of mesa/JTE type of the component. The stress will be laid on the parameters of the JTE (length and implanted dose). The passivation of the component is ensured by a deposition of SiO₂. This layer was taken into account in simulation and the results will be presented. Technological unfolding will be presented in order to show the various technological stages necessary for the manufacture of the thyristor. The electric characterization of the component will be to divide into two parts. First of all, the forward state of the thyristor will be presented and followed better results of the breakover voltage. This paper will end in a cartography of the behaviour in tension of the components before passing to the conclusion and the prospects for the various components.

Structure and operating mode of the 4H-SiC thyristor :

The n-type 4H-SiC wafer material was purchased from Cree ResearchTM, including a PP-NP⁺ (from the wafer up to the top) epitaxial layer structure (figure 1). Three junctions determine the thyristor. If an anode cathode voltage is applied, the junctions J₁ and J₃ are into direct and J₂ in reverse. To put in conduction the thyristor, it is necessary to polarize the J₂ junction on line by injecting electrons in the gate zone. To block the thyristor, the voltage V_{AK} should be cancelled. So the holding current is determined at the switch-off of the thyristor by I_H. The thyristor can be put in conduction starting from the state blocked by the mechanism of impact ionization. Thus, the latch-up current is determined by the symbol I_L.

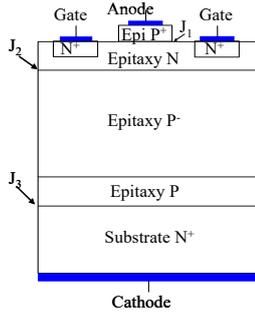


Fig. 1 : Cross sectional view of the 4H-SiC GTO-thyristor

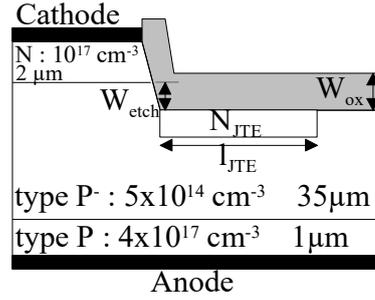


Fig. 2 : Cross sectional view of the 4H-SiC diode simulated

The reverse mode is characterized by a negative voltage V_{AK} . This mode is very often destroying for the component. In this paper, no simulation and electric characterization will be presented for this case. This part showed the various modes of the thyristor, the phase of design of the thyristor will be to approach.

Simulation results :

The first stage of this work rests on the design of the component using simulation with finite elements code. In this part, a detailed attention will be given on the behaviour in tension of the component and in particular on peripheral protection and passivation. The characteristics of the various layers were given during a preceding work. [5]. It is only the J_2 junction which is responsible for the behaviour in voltage. To this end, only the diode NP-P was simulated. Figure 2 illustrates the structure simulated with the various parameters to optimize for protection (depth of engraving, length and amount of the JTE). An angle of 10° was retained but actually a perfectly perpendicular engraving is very difficult to obtain. The characteristics of the various layers from SiC are those of the plate which will be processed.

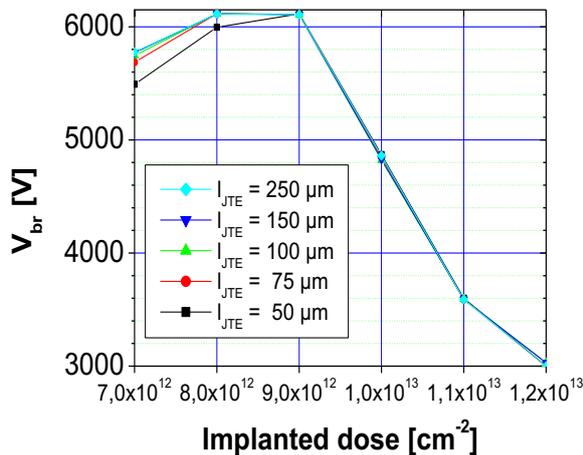


Fig. 3 : Breakdown voltage of the device versus implanted dose (N_{JTE}) for different length of the JTE (l_{JTE}),

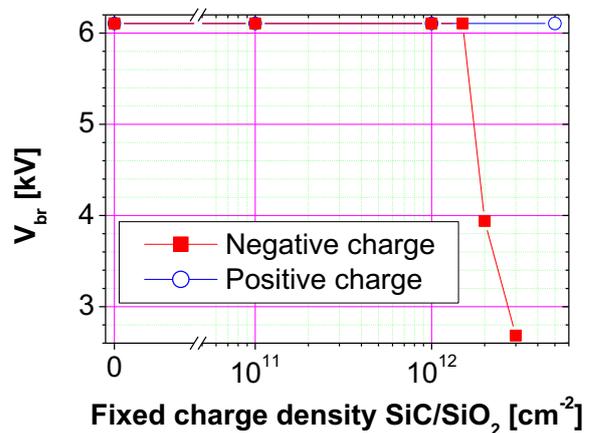


Fig. 4 : Breakdown voltage versus the effective charge density for thyristor protected by mesa/JTE combination

A first group of simulations was carried out for an etching depth W_{etch} of $1 \mu\text{m}$ and a profile of doping of the JTE obtained by a software of ion implantation in SiC [6]. Figure 3 represents the breakdown voltage of the diode according to the implanted dose of the JTE (N_{JTE}) for various lengths of JTE. An optimal dose (d_{op}) can be retained for the various lengths of JTE (l_{JTE}) and it equals at $9 \times 10^{12} \text{ cm}^{-2}$. If the dose is lower than d_{op} , the voltage varies little and the

electric field is maximum in the JTE on the left of the JTE. On the contrary, if the dose is higher than d_{op} , the voltage varies brutally. The electric field peak is in end of JTE. Thus, the JTE plays the role of the anode and the problem of periphery is deferred. The parameters retained for the JTE periphery are a length higher or equal to $150 \mu\text{m}$ (l_{JTE}) and an optimal dose of $9 \times 10^{12} \text{ cm}^{-2}$.

With these optimized parameters, simulations were carried out by holding account a thickness of SiO_2 (W_{ox}) equalizes with $1,5 \mu\text{m}$. The density of fixed charge to the SiC/SiO_2 interface was defined. According to, the conditions of growth of oxide and the nature of the equipment used, the sign and the value of this density vary. Figure 4 illustrates the results of simulation. Charge of the positive type do not have an influence on the behaviour voltage. On the other hand for the negative charges of which the density of loads is higher than 10^{12} cm^{-2} , the behaviour in voltage decreases. If the charge are negative in oxide, they are positive in SiC (neutrality). The spreading out of the space charge is thus disadvantaged even in the presence of the JTE what leads to the fall of the behaviour in voltage. In conclusion, the state of SiC/SiO_2 interface can be responsible for a bad behaviour in voltage of the component. These various results will be confronted with the experimental characteristics.

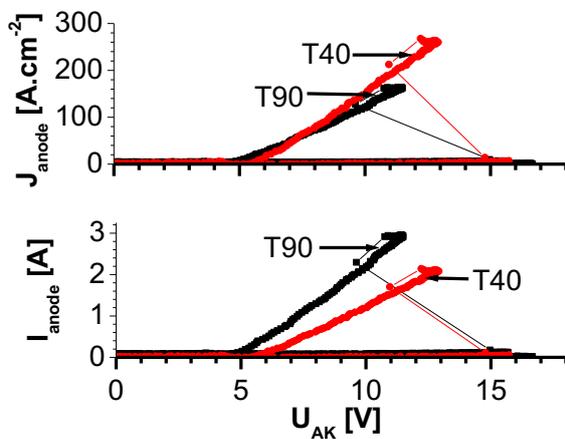


Fig. 5 : Electrical characterisations in forward state.
T40 and T90 is two different devices

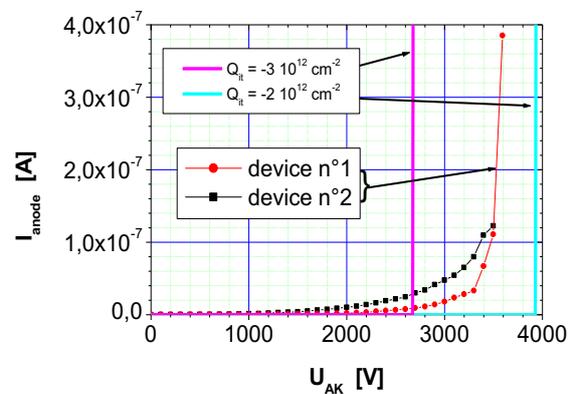


Fig. 6 : Experimental and simulated electrical characteristics

Technology process :

The process sequence has been divided in five photolithographic levels. The realization began with two different dry etchings, the first allowing to make the gate contact. The etch depth equals to $1.4 \mu\text{m}$. The second one necessary for the mesa protection. Within sight of the results of simulation, a etching depth of $1 \mu\text{m}$ was requested from the technology center and it was reached. A nitrogen implantation followed by $1700^\circ\text{C}/30\text{mn}$ annealing were needed to realize the JTE. This establishment required 4 different energies and 4 amounts since the mechanism of diffusion in SiC is non-existent. After a $1.5 \mu\text{m}$ oxide deposition by LTO (Low Temperature Oxidation) process to passivate the thyristor structure, a nickel metallization has been realized. With a thickness of 500 nm only, the realization of bonding is not possible. It will be to consider after one on-metallization and the first metallization show some good ohmic contact.

Electrical characterizations :

First of all, an electric characterization of setting in conduction of the thyristors was carried out. The voltage source used is one curve tracer Tektronix 370 whose control signal was

formatted. Figure 5 represents the results in the form of current density and current. The threshold voltage lies between 5 and 6 V. These values are higher than those obtained by simulation (3 V). This is due to non-ohmicity of the anode contacts. This voltage can decrease by improving to a significant degree metallization of anode.

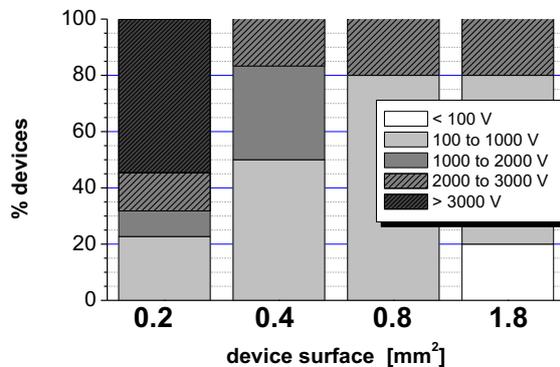


Fig. 7 : Statistic of the breakover voltage as a function of the device surface (in percents) *i*

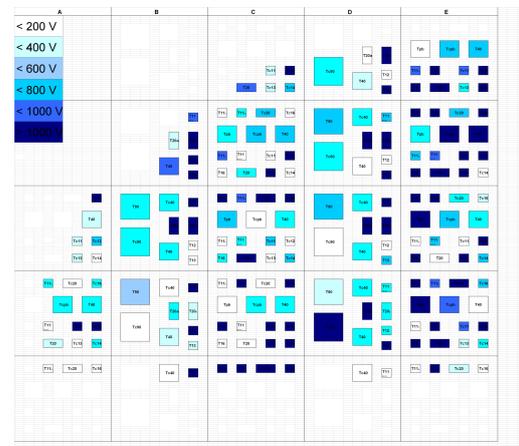


Fig. 8 : Repartition of the breakover voltage of thyristors as a function of the device place on the quarter wafer surface

The blocking forward state was characterized first once on 46 components. The best held in tension is equal to 3500 V. A comparison is carried out between the experiment and simulation and it represents by figure 6. Thus, charge are of the negative type to the SiC/SiO₂ interface and the density lies between 2 and 3 10¹² cm⁻². Moreover, statistics were carried out and they are represented by figure 7. This reveals that in fact the components of low size have the best held in voltage. This is due to the various defects in material. All devices on the sample have been electrically characterised with a 1100 V Keithley K2410. Figure 8 shows the location of the breakover voltage on the wafer surface. The dark ones hold a voltage of up to 1kV. This figure clearly shows that the repartition of the better ones, is not uniform. We can see that most of them are placed in the upper left side of the sample, whereas nearly no thyristor, able to hold a higher voltage, are placed in the left border region. That illustrates the non uniform distribution of wafer defects.

Conclusion :

We conclude, that the results are encouraging for the use of SiC-thyristors in power applications. The turn-on characterisations are in progress and will be described in the final paper. The setting in conduction of the components show limits from a point of view of threshold voltage. Confrontation experiment and simulation for the blocked state made it possible to highlight which the stage of passivation was to be optimized in particular in term of preparation of surface.

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