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# Switching losses calculation method for modular multi-level converters using half-bridge submodules

Benhur Zolett, Juan David Páez, Joan Sau-Bassols, Daniel Gomez A. and Florent Morel, *Senior Member, IEEE*

**Abstract**— Several converters based on series-connected submodules have been reported in the literature for high voltage direct current (HVDC) applications. For these converters, the calculation of switching losses in the semiconductors is challenging since it is difficult to predict the instants of the switching actions. Analytical methods with low accuracy and methods based on detailed simulations with long computation time have been proposed in the literature for modular multilevel converters (MMC). In this context, this paper proposes a simulation-based method for calculation of losses on any converter topology based on stacks of half-bridge submodules balancing accuracy and computing time. The method is based on the time-domain simulation of a submodule stack model in Matlab/Simulink. Then, the converter key operation values obtained from the simulation, such as stack current and submodule control actions, are used to calculate the switching losses in a post-processing treatment. To validate the method, the submodule stack switching losses of a MMC and a DC-MMC are assessed. The method is compared against a detailed model simulation using PLECS platform as a reference and against analytical methods. Furthermore, a statistical analysis of the losses distribution among the submodules and a sensitivity analysis are performed. As result, the proposed method gives a good trade-off between accuracy and computing time. The contribution of this paper is the proposed method to assess switching losses in converters based on stacks of submodules, not only the MMC, with acceptable accuracy and low computing time, compared with other state-of-the-art methods.

**Index Terms**—modular multilevel converters, switching losses, simulations, HVDC, balancing control algorithm, voltage balancing control.

## I. INTRODUCTION

The development of voltage-source converters (VSC) for high voltage direct current (HVDC) applications have turned to modular multi-cells converters. These technologies, which were mainly dedicated to static synchronous compensators (STATCOM) [1], are nowadays used for AC-DC conversion in HVDC links, with the modular multi-level converter (MMC) as the widespread solution [2]. The main advantages of MMCs over other technologies are the modularity, the low harmonic content and the scalability [3]. Another important characteristic of MMCs is the low level of losses compared to two or three-level VSCs, which is mainly linked to lower switching frequency operation [4]. For HVDC projects, losses directly affect investment cost (cooling system

sizing) and operational costs, being an important key performance indicator, thus, losses need to be assessed early in the design stage. The MMC is a well established solution for HV AC/DC conversion, but other AC/DC topologies are under study [5]. Future HVDC systems may also require DC/DC conversion to connect systems with different voltage levels, HVDC technology or grounding schemes [6]. In the literature, several DC/DC based on series connection of submodules have been proposed (front-to-front MMC, DC-MMC, DC-autotransformer, etc.) [7]. For those converters, losses are also an important key performance indicator to assess their interest.

The main source of power losses in a MMC are the semiconductor devices [8]. Conduction losses can be reasonably estimated using analytical expressions. However, the estimation of switching losses brings more challenges, especially if a balancing control algorithm or voltage balancing algorithm is used to balance the voltage levels in the submodules. The reason is that the switching events may no longer be uniformly distributed, as it happens with pulse-width modulation strategies (PWM), thus, being difficult to predict [9]. Two main strategies can be considered to evaluate the switching losses: using analytical expressions or time-domain simulations.

Analytical expressions provide a fast way to evaluate the losses, at the expense of lower accuracy. Regarding the analytical expressions, a solution is proposed in [10], [11], where an average switching frequency is used, assuming that the switching events are uniformly distributed during the AC period. Nonetheless, the previous method still requires knowing the average frequency of the converter, which must be obtained from simulations anyway. In [9], the switching losses are divided in two components, the essential (dependent on the variation of the inserted voltage by the submodule stack) and the additional (non-predictable component from the balancing control algorithm). In [12] a distribution of probability of switching events is also used, which is composed of two terms: one proportional to the derivative of the modulation index of an average submodule and another due to the capacitor voltage boundaries, which is assumed to be equally distributed within the period. In [13], the switching actions are divided between the ones due to the modulation, common to all balancing control algorithms, and the ones dependent specifically on each balancing control algorithm. It provides a good agreement with the losses estimated using detailed simulations and errors between 3-26% compared to a real scale MMC station. Although all these methods have been proposed for the MMC, they have been used to assess the losses of other topologies of converters based on the series-connection of submodules, for example the DC-MMC in [14], but without assessing the validity of the method for such topologies.

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Time-domain simulations provide accurate results at the cost of long simulation times due to the detailed models with a high number of submodules. Some approaches to reduce the calculation time have been proposed in the literature. In [15], a virtual MMC arm model is proposed to estimate MMC losses. The steady-state arm current and voltage are analytically obtained from the input parameters. They are given to the virtual arm model, in which a balancing control algorithm selects the submodules to be inserted/bypassed. The losses are then calculated in a post-processing using the arm current and the switching actions. A 11-level Simulink detailed model is used for the validation. However, the proposed method is exclusively applied to the MMC and the validation is done with detailed simulations with a low number of submodules, which may not reflect the real situation. Another time-domain approach has been proposed in [16], where a first simulation of an average model MMC is performed to obtain the arm current and voltage. Those magnitudes are used as inputs for a second simulation, where only an MMC arm is simulated. The outputs of the simulation are used to estimate the losses in a post-processing stage. Nevertheless, the approach is only applied to the MMC and there is no comparison with other state-of-the-art methods or validation of the results.

The previous methods focus only on the AC-DC MMC, meaning that there is not a general methodology to estimate the switching losses applicable to any converter made with series connected submodules. Additionally, there is no analysis on the distribution of losses among the different submodules across time. In this context, this paper proposes a time-domain simulation method for calculating the switching losses of a series connection of submodules as a building block for different converter topologies. The objective is to achieve a trade-off between simulation time and precision, as well as to estimate losses for any power converter composed of submodule stacks. First, the methodology relies on the analytic calculation of the required parameters to simulate the stack model (stack current, voltage, etc.) from the converter operation point. Then, the simulation of the stack provides the necessary data (stack current and control actions of the submodules) to compute the switching losses in a post-treatment process also using the datasheet parameters of the selected semiconductors. Furthermore, the method can either use the data of one submodule or the data of all submodules of a given stack to improve precision with no major extra simulation time. Two case studies are considered, in which the losses of a half-bridge-based MMC and half-bridge-based DC-MMC are estimated. Results from the proposed method are compared with analytical methods and to a reference losses calculation tool (detailed simulation with a high number of submodules) to assess the precision of the method. Additionally, a statistical analysis to study the losses distribution among the different submodules and a sensitivity analysis are provided for the two converter topologies.

The contribution of this paper is the proposed time-domain simulation method to calculate the switching losses of converters based on stacks of submodules with acceptable accuracy and much less computing time, compared with other state-of-the-art methods. The method is validated by comparing it to long detailed time-domain simulations of different converter topologies with a high number of submodules unlike

previous work in the literature. Additionally, the losses distribution analysis performed on the paper provides an explanation for the low accuracy of other methods used in the literature.

This paper is organized as follows. Section II presents a submodule stack, its control system, and models. Section III explores the different losses in a modular converter, their causes, and their importance on the converter design. Section IV describes the methodology used in the study, detailing the applied calculation methods. The proposed method is extensively explained. Section V describes the case studies and Section VI exposes the results, hypothesis validations, the statistical analysis of the losses distribution among submodules for different methods and a sensitivity analysis. Finally, section VII brings the conclusions and perspectives of this study.

## II. SUBMODULE STACKS

### A. Structure

Cascaded submodules are usually series connected forming a submodule stack (Fig. 1). Each submodule is formed by power semiconductor devices and a capacitor. Different types of submodules have been reported in literature but the typical ones are the half-bridge and full-bridge submodules. In this paper only half-bridge submodules are considered.

The operation of a submodule stack relies on the individual control of each submodule. The switches on the submodule are controlled to insert or bypass the capacitor in the stack. Thus, a half-bridge-submodule generates at its terminals a voltage  $v_{SM_i}$  equal to the submodule capacitor voltage  $v_{C_{SM_i}}$  when is inserted, and zero when it is bypassed as shown in Fig. 2. In the case of the full-bridge-submodule, the capacitor can be inserted in positive or negative polarity.

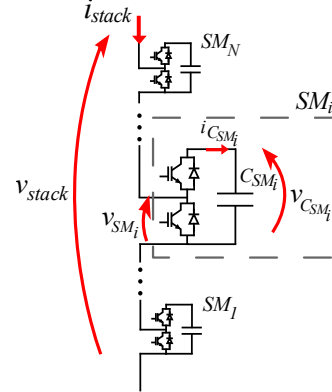


Fig. 1. A half-bridge submodule stack.

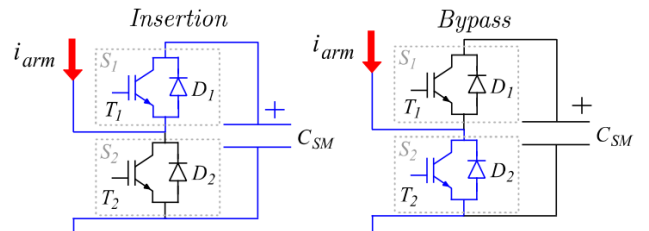


Fig. 2. Insertion and bypass state of a half-bridge submodule, illustrating the semiconductor that conducts in each state.

The voltage and current waveforms for a submodule stack depend on the converter in which it is used and the control

principles. Indeed, the waveforms can vary, for example if a third harmonic is generated, if second harmonic current circulation is considered, or according to the converter topology. The submodule stack losses are then affected by the converter topology and the control principles. In the following, the control principles of a submodule stack are explained.

### B. Control system

The control system of a converter is designed to maintain the submodules capacitor voltage controlled. The average value should be constant in steady state operation. To achieve this, the controller sets the submodule stack voltage and current ( $v_{stack}$  and  $i_{stack}$  on Fig. 1) to have DC and AC components as shown in (1)-(2). In principle, the AC components can be of any form and include any number of harmonics, but in this paper to explain the main phenomena, we consider only a sinusoidal waveform at one operating frequency  $f_{op}$ . The converter is assumed to have an energy control with indirect modulation, i.e. there are no second harmonic circulating currents. A more general analysis of the submodule stack energy balance including any number of harmonics can be found in [17]. In case of additional harmonics or circulating currents, (1) to (3) can be adapted to reflect these components.

$$v_{stack} = v_{dc} - v_{ac} \cos(2\pi f_{op} t) \quad (1)$$

$$i_{stack} = i_{dc} + i_{ac} \cos(2\pi f_{op} t + \phi) \quad (2)$$

$$\langle P_{stack} \rangle = v_{dc} i_{dc} - \frac{1}{2} v_{ac} i_{ac} \cos(\phi) = 0 \quad (3)$$

The parameters on (1)-(2) depend on the converter topology and are set according to the power balance on (3).  $v_{dc}$  and  $i_{dc}$  are the DC voltage and current of the stack (depending on the DC grid voltage and the power exchange of the converter);  $v_{ac}$  and  $i_{ac}$  are the amplitude of the AC voltage and current (depending on the energy balance of the converter).

The energy balance of the submodule stack is reflected in (3): if losses are neglected, during one cycle all DC power being absorbed/delivered by the submodule stack in DC form should be delivered/absorbed in AC form to prevent the submodule capacitors to be charged or discharged. In general, in a modular converter  $v_{dc}$  and  $i_{dc}$  are calculated to follow a power reference, while the AC components ( $v_{ac}$  and  $i_{ac}$ ) are calculated by the energy control to balance the submodule stack.

The simplified control scheme of a submodule stack, used in this paper, is presented in Fig. 3. This control is based on the approach used by the main control philosophies proposed for AC-DC and DC-DC modular multilevel converters [18], [19].

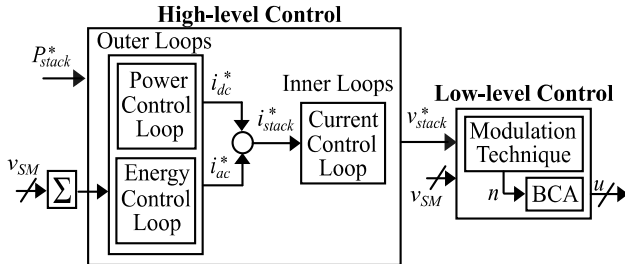


Fig. 3. Simplified control scheme of a submodule stack

The controller can be divided into a high-level control and a low-level control stage. The high-level stage defines the submodule stack voltage to be generated. This is calculated from a current controller. The current reference is calculated by a controller on the submodule stack energy and converter power. The power reference is given by the converter control according to the operating point, while the energy reference is generally given according to the nominal value of the voltage on the submodule capacitors.

While the high-level control is responsible of controlling the submodule stack voltage and currents, the low-level control (or switching algorithm) guarantees the balancing on the voltage of each submodule in the stack and selects which submodules to insert or bypass to generate the stack voltage requested by the high-level control.

Different approaches for low-level control have been proposed in the literature, including modulation techniques such as PWM or nearest level modulation, and multiple balancing control algorithms [4]. PWM provides a regular switching frequency that can be adjusted based on the carrier signal. However, PWM strategies could increase the switching frequency and implementation complexity compared to the nearest level modulation [4], [20]. For HVDC applications, the low-level control is mostly based in nearest level modulation with a balancing control algorithm. In this approach, the nearest level modulation finds the number of submodules to insert, and the balancing control algorithm selects the submodules depending on the voltage of each capacitor and the stack current. The total inserted voltage complies with the reference calculated by the high-level control while keeping the voltage balance between the different submodules. The considered balancing control algorithm and its parameters are discussed in Section V.

### C. Models

To analyze the switching losses, it is necessary to model the submodule stack in a way that includes the different control signals of all the submodules. In this paper we consider two different models: a semi-analytical detailed model and an ideal switch-based model.

Both models are presented in Fig. 4. In the proposed semi-analytical model, the cascaded submodules are modelled as a controlled voltage source given by (4), and the submodule voltage dynamics is modelled by (5). The submodule stack voltage according to the capacitor voltages ( $v_{c_{SM}}$ ) of inserted submodules is shown in (4), where  $u_i$  is the control signal of the  $i^{th}$  submodule ( $u_i = 1$  when the submodule is inserted, and 0 when it is bypassed) and  $N_{SM}$  is the total number of submodules in the stack. The voltage dynamics on each submodule capacitor is presented in (5), where  $C_{SM_i}$  is the capacitance of the  $i^{th}$  submodule, and  $i_{stack}$  is the stack current. The control signal  $u_i$  comes from the controller to generate the required stack voltage.

$$v_{stack}(t) = \sum_{i=1}^{N_{SM}} \left( v_{c_{SM_i}}(t) * u_i(t) \right) \quad (4)$$

$$\frac{dv_{c_{SM_i}}(t)}{dt} = \frac{1}{C_{SM_i}} (u_i * i_{stack}(t)) \quad (5)$$

In the switch-based model, each submodule is modelled with a circuit using ideal switches. The input variables are the control signal of the submodule  $u_i$  (output of the low-level control) which allows to compute the control order to each switch. The switches are modelled as variable resistors, the resistance value depends on the control order  $u_i$ .

The main hypothesis for both models in this paper is that it is assumed that switch losses do not impact the current and voltage waveforms: switches are modelled as ideal switches and losses are computed in post-processing.

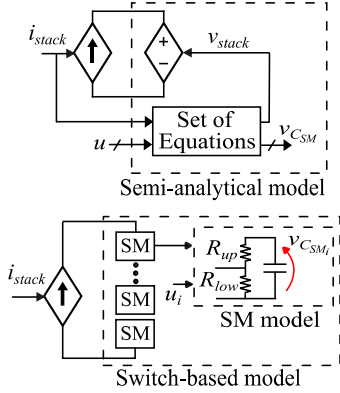


Fig. 4. Submodule stack models

### III. LOSSES IN SUBMODULE STACKS

As stated in the introduction, the analytical estimation of conduction losses provides a good agreement with the estimation using simulations, since the semiconductors in the current path are known at each instant [9], [21].

The estimation of the switching losses of converters based on submodule stacks brings more difficulty. It is generally based on summing all turn-on ( $E_{on}$ ) and turn-off ( $E_{off}$ ) energies of the semiconductors in the submodules and dividing by the elapsed time ( $t_{total}$ ) as shown in (6).

$$P_{sw} = \frac{1}{t_{total}} \sum (E_{on} + E_{off}) \quad (6)$$

The value of the energy loss during the switching of the semiconductors (either the turning-on and the turning-off) is influenced by the voltage and current at the instant of the switching (higher current and voltages lead to higher losses), the junction temperature of the semiconductor, and the gate resistance of the IGBTs (which affects the switching time). Manufacturers of semiconductors tend to give information about energy loss during switching events via datasheets or XML files. On the one hand, datasheets provide graphics with the turn-off and turn-on energy as a function of the current for a given junction temperature, gate resistance and switched voltage as shown in Fig. 5. On the other hand, XML files typically provide more data in the form of look-up tables giving the turn-off and turn-on energy as a function of current, voltage, junction temperature and gate resistance. Fig. 6 shows one of these 3D look-up tables for a specific junction temperature.

For any of both cases the difficulty for estimating the switching energies in submodule stack-based converters is to calculate the semiconductor current and voltage at the moment of the switching. Indeed, the insertion and bypass of the

submodules depend on the switching algorithms. When using a balancing control algorithm in the low-level control of the converter, the state of each submodule is difficult to predict without using detailed simulations. Since the exact moment of the switching event of each submodule is not known, it is not possible to identify the value of current and voltage at the switching instant, and so, the proper estimation of the switching losses becomes a challenge [10].

The use of detailed simulations can be used to precisely identify the switching instants, thus, estimating properly the losses, at the cost of increasing the simulation time, due to the large number of submodules in HVDC submodule stack-based converters. Thus, an appropriate method that gives a good compromise between rapidity and precision is required.

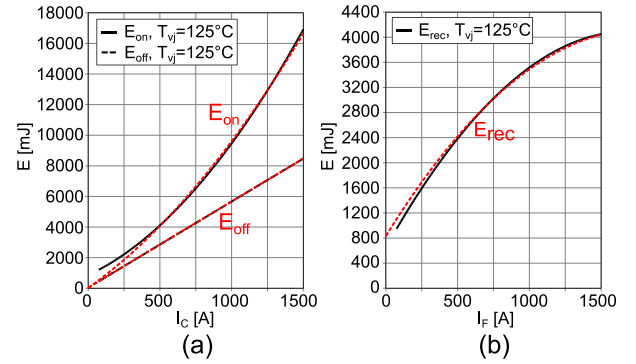


Fig. 5. Switching energies for the FZ750R65KE3 module with 2nd order regressions. (a) IGBT turn-on and turn-off energies. (b) Diode turn-off energy

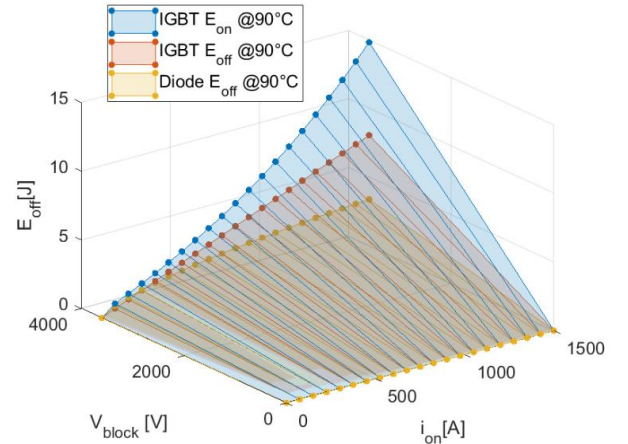


Fig. 6 - FZ750R65KE3 module switching losses data at the considered temperature.

### IV. METHODOLOGY FOR SWITCHING LOSSES EVALUATION

This section presents three different methods to estimate the switching losses in submodule stacks based on the parameters from the manufacturers mentioned in Section III. For method 1, the switching energy parameters are extracted from the XML model of the manufacturer of the switch. The parameters from the datasheet curves are used for method 2 and 3. The difference between the methods are the utilized models and the approach to estimate the switching energies.

### A. Method 1 – Coupled electro-thermal simulation

The first method is considered as the reference method for comparison, because of its accuracy. It is based on the electro-thermal modelling proposed by PLECS [22], which is a software package for modeling and simulation of dynamic systems dedicated to power electronics. Any other simulation

$$P_{sw_i} = f_{sw} \frac{1}{T} \int_0^T E(t) dt \quad (8)$$

software that allows computing losses using electro-thermal models could also be used. In this method, as well as for the other methods, only one submodule stack is simulated at a time.

In this method, a thermal model is coupled to an electrical model. For each simulation time-step, the losses on the semiconductor devices are computed considering their pre-switching on-state current for turn-off, post-switching current for turn-on, blocking voltage, instantaneous temperature, and gate circuit resistance. These losses are injected in the thermal model, which consists in a thermal network describing the thermal impedance between the semiconductor junction and the ambient or the heatsink fluid temperatures. In the end of each time-step, new temperatures for the devices junctions are calculated, as well as new electrical states, following this iterative process all long the simulation.

To calculate switching losses, the electrical inputs (on-state current, pre- and post-switching current or voltage, junction temperature) are confronted to 3D data chart such the one shown in Fig. 6. Instantaneous losses are calculated through linear interpolation with the input data. In addition, the data used in this work come from XML files provided by semiconductors manufacturers. Then the switching energies are added and divided into the total elapsed time.

### B. Method 2 – Analytical calculation

In this method, an analytical approximation of the switching losses is done. Since it is difficult to estimate accurately the current and voltages of the semiconductors at the moment of the switching, the strategy on this method consists in integrating the switching energy during one period and multiplying by the fundamental operating frequency of the submodule stack current. During the integration, the switching energy is weighted by a function  $p(t)$  as shown in (7). This equation gives the switching losses of one of the submodules in the stack. The total losses in the stack are obtained by multiplying by the number of submodules in the stack,  $N_{SM}$ , implying that method 2 assumes a uniform distribution of losses among the different submodules.

$$P_{sw_i} = f_{op} \frac{1}{T} \int_0^T p(t) E(t) dt \quad (7)$$

The submodule switching energy  $E(t)$  is calculated considering only its dependance on the submodule stack current, using the semiconductors datasheet information (Fig. 5) and the submodule stack current expression which is determined analytically from the converter steady state analysis (see (2)).

The function  $p(t)$  can be interpreted as the density function of the number of switching events over the time. For the estimation of  $p(t)$ , different strategies have been proposed in literature. In [10], [11], it is proposed that switching events are distributed uniformly in time, i.e.  $p(t) = n$  where  $n$  is a

constant that represents the number of switching events per period. In [12], the authors propose an estimation of  $p(t)$  separating in two terms, one that is constant and is related to the balancing actions of the balancing control algorithm, and other that represents the switching actions needed for generating the submodule stack voltage so depends on its derivative. In this paper the first approach is retained for comparison. Thus, (7) becomes (8), where  $f_{sw}$  represents the average switching frequency of one submodule in the stack.

The methods proposed in literature do not indicate an approach to estimate analytically  $f_{sw}$ . This value should be calculated from detailed model simulations in the case of using a balancing control algorithm as low-level control.

### C. Proposed method – Simulation-based post-processing

The proposed method in this paper to estimate the switching losses considers the semi-analytical model of a submodule stack introduced in Section II.C. The model is implemented in a simulation software (Matlab Simulink for this work) and makes use of additional scripts to calculate the input parameters and perform the post-processing calculation of switching losses (see Fig. 7). To exemplify the process, the steps of the proposed method are explained considering the submodule stack of the upper arm of one phase of an MMC and also for the DC-MMC. However, it can be applied to any converter made of submodule stacks by obtaining the steady-state solution in terms of current and voltage that the stack withstands.

#### 1) Steady-state calculation script

The MMC inputs of the simulation model are the DC voltage  $V_{DC}$ , line AC RMS grid voltage  $V_{AC}$ , DC power reference  $P$ , reactive power reference  $Q$ , AC frequency  $f_{op}$ , average voltage of the submodule  $V_{SM}$ , submodule capacitance  $C_{SM}$  (voltage ripple in submodule  $\Delta V_{SM}$ ), arm inductance  $L$ , number of phases  $N_{ph}$ . The switching energy parameters of the desired switch in the submodules have to be introduced as well to be able calculate the switching losses (see Section III). From the previous values it is possible to calculate the steady-state solution for the MMC (AC and DC voltage and currents). Then, the current through one stack of submodules  $i_{stack}$ , which is composed of a DC component ( $i_{stack}^{DC}$ ) and an AC component ( $i_{stack}^{AC}$ ), can be computed.  $i_{stack}^{DC}$  is given in (9) and the phase shift of  $i_{stack}^{AC}$  and its peak value can be calculated using (10) and (11), respectively.

$$i_{stack}^{DC} = \frac{P}{N_{ph} V_{DC}} \quad (9)$$

$$|i_{stack}^{AC}| = \frac{\sqrt{3}P}{\sqrt{2}N_{ph}V_{AC} \cos \phi} \quad (10)$$

$$\angle i_{stack}^{AC} = \phi \quad (11)$$

where,  $\phi$  is the phase shift between the grid voltage and current given by (12).

$$\phi = \text{atan} \left( \frac{Q}{P} \right) \quad (12)$$

The steady-state voltage that the submodule stack withstands has also a DC component ( $v_{stack}^{DC}$ ) and an AC component ( $v_{stack}^{AC}$ ), that for the upper arm stack of an MMC are given by (13) and (14), respectively. This voltage is used in the high-level control loop of the semi-analytical model.



$$v_{stack}^{DC} = \frac{V_{DC}}{2} \quad (13)$$

$$v_{stack}^{AC} = \frac{V_{AC}}{\sqrt{3}} \quad (14)$$

The semi-analytical model also requires the number of submodules in the stack and the capacitance of each submodule. The first is obtained from (15) the latter is given as input or obtained from an acceptable voltage ripple in the submodules.

$$N_{SM} = \text{ceil}\left(\frac{V_{DC}}{V_{SM}}\right) \quad (15)$$

Similar analysis can be done for the DC-MMC. For this DC-DC converter, the upper and lower submodule stack have different set points. The DC references are presented below, where  $V_{DC H}$  and  $V_{DC L}$  are the DC voltage on the high and low voltage side of the DC-DC converter, respectively. The AC references are calculated to balance the converter energy while reducing the losses. Further details can be found in [23], [24].

$$i_{stack\ up}^{DC} = \frac{P}{N_{ph} V_{DC H}} \quad (16)$$

$$i_{stack\ low}^{DC} = \frac{P}{N_{ph}} \left( \frac{1}{V_{DC H}} - \frac{1}{V_{DC L}} \right) \quad (17)$$

$$v_{stack\ up}^{DC} = V_{DC H} - V_{DC L} \quad (18)$$

$$v_{stack\ low}^{DC} = V_{DC L} \quad (19)$$

## 2) Simulation of the semi-analytical model

With inputs for the simulation model being calculated as described in the previous subsection, the model is executed  $N$  times, where  $N$  represents the number of different submodule stacks in one converter leg. It is assumed that the voltage and current waveforms are equivalent between legs but shifted the corresponding degrees, leading to equal losses between legs. For example, for an MMC with 3 legs, a simulation for the submodule stack in the upper arm and another for the submodule stack in the lower arm of one leg are required. Then, the losses of one leg are multiplied by 3 to obtain the total switching losses of the converter. Similarly, for a DC-MMC (with a DC voltage ratio different from 1/2) made of 3 legs, and each leg containing an upper and lower arm, requires one simulation for the upper arm and another simulation for the lower arm.

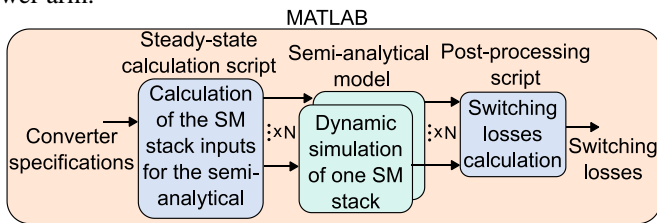


Fig. 7. General scheme of the proposed method to calculate the switching losses.

The simulation outputs for each submodule stack are the following ones:  $t$ , which contains the time steps of the simulation;  $i(t)$  which contains the submodule stack current waveform; and the control variable for each submodule,  $u_i(t)$ . Note that the actual voltage across the switch at the switching instant is not considered, instead, it is assumed that the

switching voltage corresponds to the average voltage of the submodule,  $V_{SM}$ . This could be easily improved by outputting the instantaneous voltage of each submodule. However, as it is shown in the results, approximating these voltages by the average voltage does not cause large errors.

### 3) Post-processing script for switching losses calculation.

Once the previous simulation variables have been obtained, it is possible to estimate the switching losses in the semiconductors in the post-processing script. To do this, the semiconductor switching energies ( $E_{on}^{IGBT}$  and  $E_{off}^{IGBT}$  for the IGBTs and  $E_{rec}^{Diode}$  for the diodes) are calculated approximating the curves provided in the datasheet (see Fig. 5). A second order polynomial approximation as a function of the current is done, which is shown in (20)-(22), where  $a$ ,  $b$ , and  $c$  are the regressions coefficients found for the energy losses at turn-on (subindex *on*), turn-off (subindex *off*), and turn-off of diodes (subindex *rec*).

$$E_{on}^{IGBT} = a_{on} + b_{on} i_{IGBT} + c_{on} i_{IGBT}^2 \quad (20)$$

$$E_{off}^{IGBT} = a_{off} + b_{off} i_{IGBT} + c_{off} i_{IGBT}^2 \quad (21)$$

$$E_{rec}^{Diode} = a_{rec} + b_{rec} i_{Diode} + c_{rec} i_{Diode}^2 \quad (22)$$

The switching energies are estimated for a constant junction temperature of the semiconductors that is given as a parameter. Thus, the method does not include any thermal model, in which the switching losses affect the final junction temperature. Therefore, the obtained losses can be used to size the cooling system that allows to keep the considered temperature. Also, it is considered that the junction temperature ripple during steady-state operation has a negligible impact on the switching losses. Then, the energy curves are interpolated to calculate the switching losses for the considered temperature.

Knowing the sign of the submodule stack current,  $i(t)$ , and the state of each submodule,  $u_i(t)$ , allows to identify which semiconductor turns off and which one turns on. An example to illustrate the logic of the switching losses calculation is shown in Fig. 2. Considering the submodule stack current in the direction of the red arrow, if the submodule goes from the insertion to the bypass state,  $D_1$  turns off and IGBT  $T_2$  turns on. Consequently, the  $E_{rec}^{D1}$  of the diode  $D_1$  and the  $E_{on}^{T2}$  of the IGBT  $T_2$  must be considered for this transition.

From the control variables  $u_i(t)$ , the transitions between the insertion and bypass states can be identified, along with the corresponding switching energy lost for each device. Considering that the switching energies depend on the current through the device at that instant, (23) obtains the switching losses of the half-bridge submodule  $i$  by summing all the switching energies of the semiconductors.

$$P_{Swi} = \frac{1}{t_1 - t_0} \sum_{t_0}^{t_1} (E_{rec}^{D1,D2} + E_{on}^{T1,T2} + E_{off}^{T1,T2}) \quad (23)$$

where,  $t_0$  is the time when the simulation has reached the steady state;  $t_1$  is the time when the simulation stops.

At this point, two variants of the proposed method, A and B, are considered.

Variant A presented in (24) assumes that, in steady state, switching losses are balanced among all submodules. Thus, the switching losses of one submodule are calculated using (23) and the value is multiplied by the number of submodules in the

stack,  $N_{SM}$ , to obtain the total switching losses (in that case only a control variable  $u_i(t)$  is used).

$$P_{SW}^A = N_{SM} P_{SWi} \quad (24)$$

However, the hypothesis that all the submodules have balanced switching losses may not always be valid. It may be affected by the simulation time, the balancing algorithm, the converter topology, etc. Then, the following approach (variant B) is proposed. In variant B, the switching losses of each submodule are calculated, making use of all control variables  $u_i(t)$  and (23). Then, each value of submodule switching losses is summed to obtain the total of switching losses of the submodule stack as show in (25).

$$P_{SW}^B = \sum_{i=1}^{N_{SM}} P_{SWi} \quad (25)$$

The case study in the next section allows to compare the results of the methods presented in this section and the correctness of the hypothesis when using variant A of the last method.

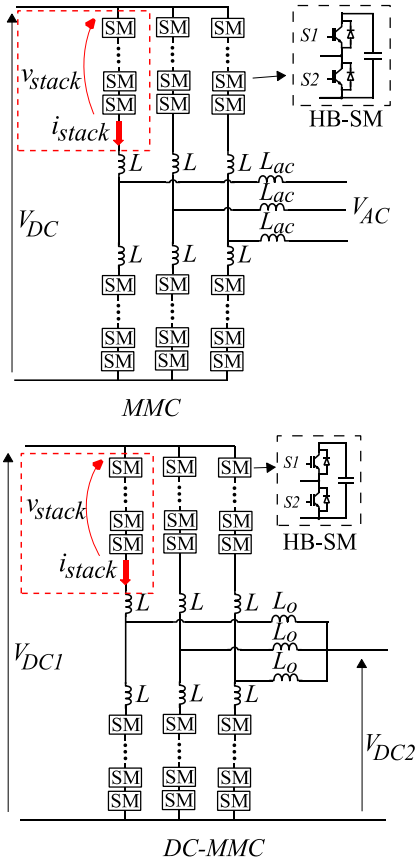


Fig. 8 – Topology of the considered converters: MMC and DC-MMC

## V. CASE STUDY

The considered topologies are the MMC and the DC-MMC as shows Fig. 8. The study focuses on calculating the switching losses in one of the upper stacks in the converters. The ratings of converters are given in Table I.

In the DC-MMC, the number of submodules on each converter stack is calculated based on the requirements to deal with DC faults. This implies that the stack voltage during operation given by (1) is less than the maximum voltage that the stack can generate. This will be seen in the voltage

waveforms presented in the section of results and is the main difference compared with the MMC submodule stack.

Table I  
Parameters of the studied converters.

Parameter	MMC	DC-MMC
DC Voltage / DC High Voltage [kV]	640	640
AC Voltage / DC Low Voltage [kV]	320	525
$I_{MAX}$ [kA]	1.25	1.29
Power rating [MW]	700	700
AC Frequency [Hz]	50	50
Submodule operation voltage [kV]	3.6	3.6
Arm inductance [mH]	50	20
Output inductance [mH]	-	400
AC Grid inductance [mH]	0	-
Upper arm submodule capacitor [mF]	3.0	1.1
Lower arm submodule capacitor [mF]	3.0	6.6
Number of submodules per stack	178	178
Analyzed stack	Upper	Upper

Both converters are considered to integrate Infineon FZ750R65KE3 6.5 kV IGBT based submodules [25]. The data for switch-on and switch-off losses of the IGBTs and the diodes included in this package are shown in Fig. 5 and Fig. 6.

For all simulations, the junction temperature is set at 90°C, turn-on gate resistance at 1.0  $\Omega$  and turn-off gate resistance at 6.8  $\Omega$ .

Both converters consider the same balancing control algorithm, which is based on the algorithm proposed in [26]. The algorithm reduces the commutation events by allowing a large voltage ripple in the submodule. Like most balancing control algorithms in the literature, this algorithm selects the submodule to be inserted based on the required voltage and the stack current. When the current is positive the submodules with the lower capacitor voltage are selected as a priority. On the other hand, when the current is negative, the submodules with the higher capacitor voltage are selected in priority. The considered balancing control algorithm is based on maximum and minimum voltage thresholds and dynamic shifts. It keeps the voltage of the capacitor in the submodules between the voltage thresholds. However, depending on the converter operation conditions, these thresholds might never be reached. The dynamic shifts are used to increase the priority of the previously inserted submodules, i.e. if the submodule was inserted in a previous balancing control algorithm step, the algorithm could assign a virtual voltage lower than the real capacitor voltage (if the current is positive) or a higher virtual voltage (if the current is negative). Thus, the previously inserted submodules have greater chances to be selected. Then, the submodule stack voltage is created with the real voltages considering the priorities previously mentioned. For this study, the operating voltage is fixed between 0.5 p.u. and 1.3 p.u., with two dynamic shift values of 64 V and 128 V. Further details can be found in [26].

## VI. RESULTS

The simulated time considers the time to reach the steady state, which is related to the uniform balance of the submodule voltages by the nearest level modulation balancing control algorithm low-level control. This way, for both cases, the steady state is reached at 2.5 s and simulations are performed



over 15 s. However, switching losses are only calculated considering the 12.5 s of simulation on steady state. It is important to notice that the simulation time here is chosen arbitrary. The effects of changing this parameter will be explored later.

### A. Results for the MMC

Fig. 9 shows some of the submodule voltages for the MMC case study. Note that the submodule voltage may fluctuate around 15% of the submodule reference value, which may not meet the requirements of a practical application. This can be reduced by modifying, for instance, the submodule capacitance. However, the proper sizing of the converters is not the purpose of this work.

The switching losses for the MMC stack are calculated considering the methods described in Section IV. The results are exposed in Table II for each method, showing the computing time, switching losses of the stack and relative error with respect to method 1. The computing time is the real measured time that it takes for the simulation software to perform 15 s of simulation time.

The average switching frequency  $f_{sw}$  required for the calculation of method 2 was obtained using a detailed model simulation and analyzing the control signal  $u_i$  of one of the submodules to count all the rising edge transitions and dividing in the total elapsed time.

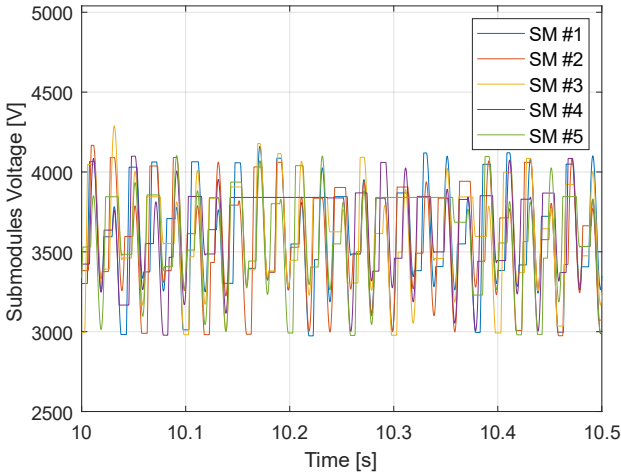


Fig. 9 –MMC submodules voltages (only 5 examples among the 178 simulated voltages are shown).

Table II

Submodule stack switching losses results considering different methods for the MMC.

	Computing time* [s]	Switching losses [kW]	Relative error
Method 1 (Ref.)	68000	193.6	-
Method 2	< 0.1	276.9	+43%
Method 3-A	65.7	197.5	+2.0%
Method 3-B	106.9	188.5	-2.6%

\*3 GHz; 128 GB RAM

One can see the extreme performances of method 1 and method 2. The first one is precise, being the reference method based on detailed electro-thermal simulations, but extremely long in terms of computing time. On the other side, method 2 based on analytical calculations is very fast but presents poor

precision. The proposed method (method 3-A and method 3-B) is in the midterm of computing time and precision.

To analyze the lack of precision of method 2, Fig. 12 presents the distribution of the switching actions of one submodule during the period of the arm current for the MMC obtained in simulation.

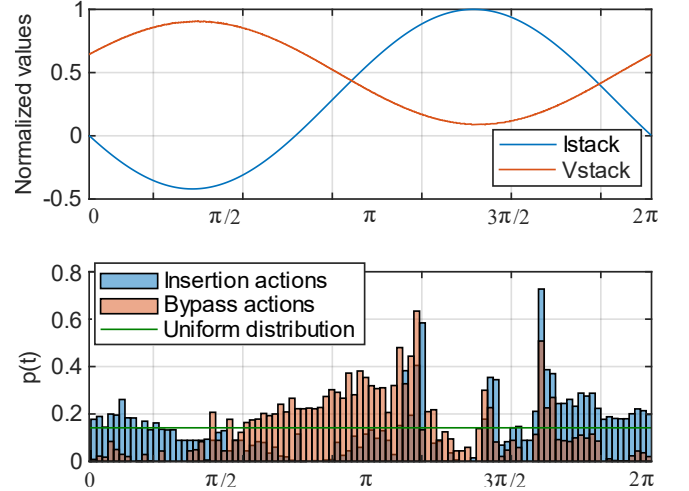


Fig. 10. MMC: Normalized stack current and voltage (top) and density of the switching actions of one submodule (bottom)

The distributions are normalized to  $2\pi$ . The hypothetical  $p(t)$  following a uniform distribution considering the obtained  $f_{sw}$  in simulation is shown as reference. The stack current and voltages are also shown, the currents are normalized with respect to the maximal current  $I_{MAX}$  obtained in simulation for each stack (see Fig. 10) and the voltage is normalized by the maximal voltage that the stack can generate, i.e.  $N_{SM} \times V_{SM}$ . It is seen that the distributions are not uniform, thus the assumptions made for  $p(t)$  on method 2 are not valid. The hypothesis of following the derivative of the submodule stack voltage is neither verified. In consequence, (8) gives inaccurate results. Method 2 can be then only used if the expression for  $p(t)$  is known precisely. In addition, this method requires to know the average switching frequency of the submodules  $f_{sw}$ , which needs a detailed model simulation to be estimated as for method 3 which provides better accuracy.

Regarding the proposed method, both variants (3-A and 3-B) give similar results (less than 3% of relative error). Method 3-A (variant A presented in Section IV. C. ), which calculates the losses with a single submodule chosen randomly, is slightly faster (65.7 s) than method 3-B (106.9 s), which considers all the submodules. The relative difference between the results of both variants is 5% for the MMC. In general, method 3 (either 3A or 3B) is seen as a good candidate for switching losses calculation for the MMC, since it provides accurate results (close to method 1) with much less computing time.

### B. Results for the DC-MMC

Fig. 11 presents some of the submodule voltages for the DC-MMC case study, showing that they are also kept within a certain range of the desired value.

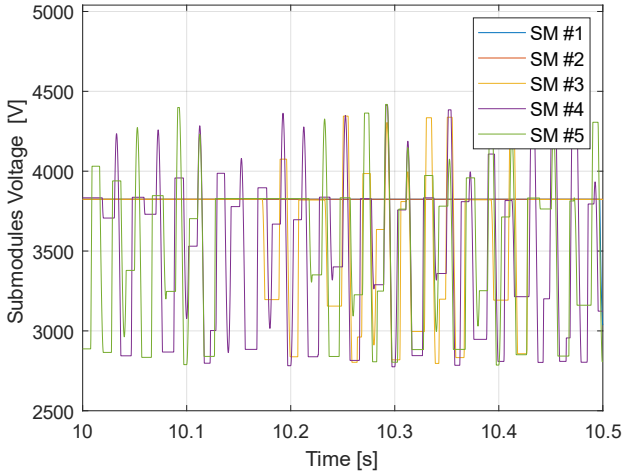


Fig. 11 – DC-MMC submodules voltages (only 5 examples among the 178 simulated voltages are shown).

The switching losses for the DC-MMC stack are calculated for each of the presented methods and the results are exposed in Table III for each method, showing the computing time, switching losses of the stack and relative error with respect to method 1.

As it can be seen, method 1 requires a lot of computing time similar to the MMC case. Method 2 is very fast but the relative error is 92%, something that is not reasonable. The proposed method (method 3-A and method 3-B) is in the midterm of computing time and precision.

Table III  
Submodule stack switching losses results considering different methods for the DC-MMC.

	Computing time* [s]	Switching losses [kW]	Relative error
Method 1 (Ref.)	38000	138.4	-
Method 2	< 0.1	265.9	+92%
Method 3-A	61.1	183.6	+33%
Method 3-B	102.9	151.8	+10%

\*3 GHz; 128 GB RAM

To analyze the lack of precision of method 2, Fig. 12 presents the distribution of the switching actions of one submodule during the period of the arm current for the DC-MMC obtained in simulation. Similarly, to the MMC case, the switching actions are not uniformly distributed along the period, which contradicts the hypothesis of method 2, thus, giving inaccurate results.

Method 3-A and 3-B present similar computing times (being 3-A also faster), but with a higher relative error (33% for 3-A and 10% for 3-B), compared to the MMC case. However, between the two variants, there is a remarkable difference in terms of accuracy, something that is not happening for the MMC case in the previous subsection. The relative difference between the results of both variants is 20% for the DC-MMC. Then, for the DC-MMC, the proposed method 3-A is not seen as a convenient candidate to perform the switching losses calculation due to their high relative error. Method 3-B should be used if low computing time is required, though the relative error with method 1 (10%) is higher than for the MMC case (2.6%).

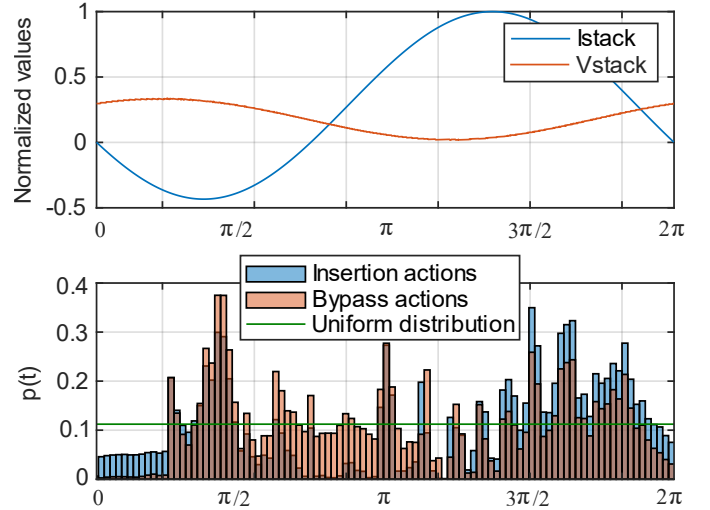


Fig. 12. DC-MMC: Normalized stack current and voltage (top) and density of the switching actions of one submodule (bottom).

### C. Losses distribution among the submodules in the MMC and DC-MMC

This subsection analyses the losses distribution among the submodules in the MMC and DC-MMC in order to explain the differences between using method 3-A and method 3-B, which are not negligible for the case of DC-MMC.

While, for the MMC, the analysis with a single submodule chosen randomly (method 3-A) gives as good results as considering all submodules (method 3-B), for the DC-MMC important differences are seen. The relative difference between the results of both variants is 5% for the MMC and 20% for the DC-MMC, as presented in the previous subsections.

The A-variant supposes that the steady-state characteristic imposes equally distributed losses for all submodules. In other words, even if the losses are not strictly the same on all submodules, the given distribution of losses on all submodules presents a standard deviation small enough to validate this hypothesis. To check this assumption, a statistical analysis of the losses on the submodules of MMC and DC-MMC is proposed.

The data from simulations performed by method 1 and by method 3-B are used. The data consists of the switching losses of all the semiconductor devices in each submodule, which are the upper diodes, lower diodes, upper IGBTs and lower IGBTs. The average power losses over the total steady state duration of each of these devices is compared between different submodule to create four statistical populations. Each population has the size of the number of submodules in one submodule stack, i.e., 178 individuals for this study.

It can be noticed that the distribution of losses on the semiconductor devices on MMC (see Fig. 13) and on DC-MMC (see Fig. 14) have different forms. In addition, one can see that the distribution of losses has greater standard deviations for the DC-MMC converter. A difference between the results of both converters is expected since the converters have a different ratio between the AC and DC components.

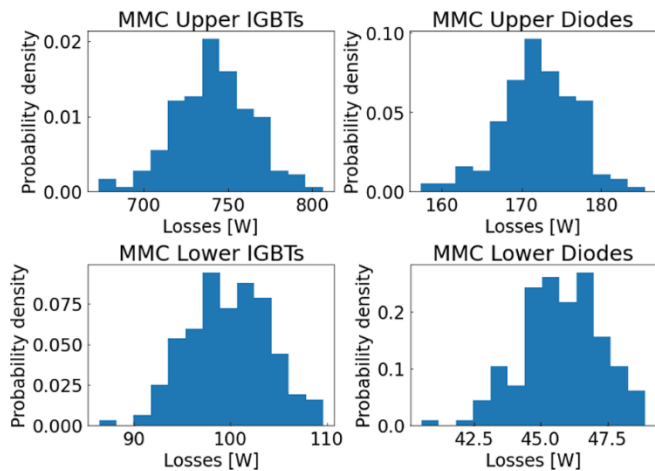


Fig. 13 - MMC switching losses statistical distributions per device.

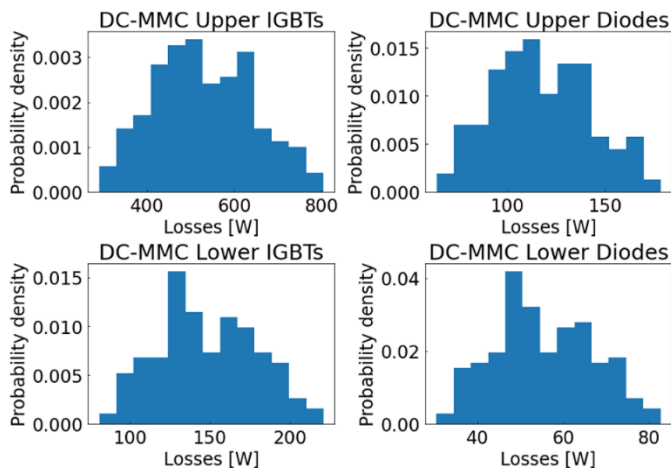


Fig. 14 - DC-MMC switching losses statistical distributions per device.

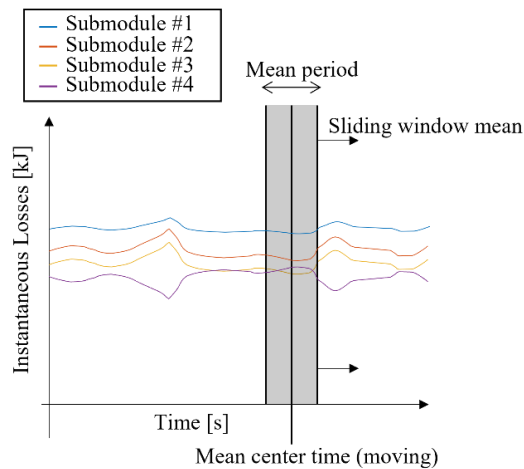


Fig. 15 - Sliding window mean definition.

Furthermore, this result partially explains the difference of 20% between the methods 3-A and 3-B for DC-MMC calculations. High standard deviations on the losses distributions can result on higher relative errors when choosing a submodule randomly to calculate the whole stack losses. However, if the standard deviation of any population is sufficiently low, the proposed variants are equivalent.

In this context, the ceil of 1% of standard deviation is arbitrarily chosen to justify the use of variant method 3-A. To consider the influence of the mean time of instantaneous losses to achieve power losses, a sliding window mean as defined in Fig. 15 is applied on the total switching losses of each one of the 178 submodules. The mean calculation is applied between  $t_0$  and  $t_1$ .

Fig. 16 shows the standard deviation for different mean periods and mean center time for the DC-MMC. A 90 s simulation is performed of a DC-MMC topology for this purpose. It is seen that moving the mean center time does not significantly impact the standard deviation results meaning that the steady state operation is achieved. However, it suggests that the standard deviation decreases with the mean period. Thus, calculations considering a variable mean period are considered. Results for MMC and DC-MMC in a 12.5 s simulation are shown in Fig. 17. It is seen in both cases that the standard deviation decreases with the increase of the mean period. It can be noticed that the 1% ceil is reached with a mean period of 10 s for the MMC, while the DC-MMC remains above 5%. The simulation over 90 s is then explored to find the ceil of standard deviation for the DC-MMC. However, within this time, the standard deviation is 2.5%, still not reaching the 1% ceil to justify the proposed method A. Since longer simulations would not be possible because of calculation limitations, a linear extrapolation was set to find the ceil of 1% of standard deviation, which was found to be around 150 s for the DC-MMC. This way, longer simulations are required to apply the proposed method A to DC-MMC. This result justifies the better precision of proposed method B in this case.

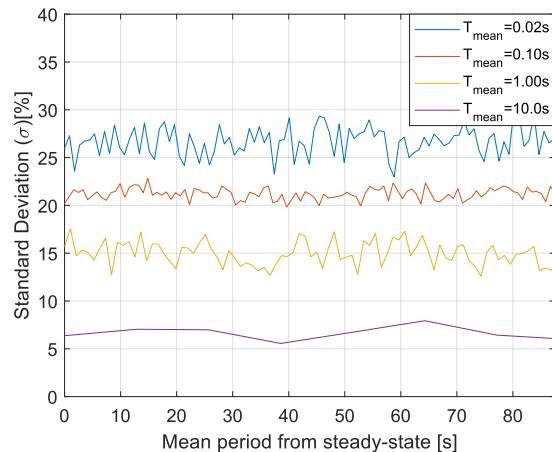


Fig. 16 – Standard deviation of switching losses between DC-MMC submodule stack considering different mean center time and period.

In any case, the results on standard deviation raise some questions around the pertinence of the considered balancing control algorithm for the DC-MMC study case. For this converter, extended time is needed to balance the losses, which can result in unequal temperature distribution along different semiconductor devices and may cause unbalanced ageing of the converters submodules. As a low standard deviation needs to be reached within a reasonable time of operation, the time to reach a ceil standard deviation of 1% for instance could be used as a quality parameter to assess different balancing control algorithm solutions.

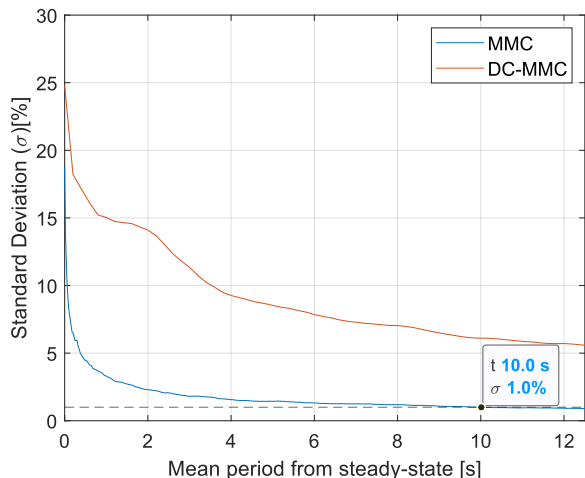


Fig. 17 – Standard deviation of switching losses of each MMC and DC-MMC submodule stack considering different mean periods. 1% ceil reached for MMC topology.

#### D. Sensitivity Analysis

A sensitivity analysis is proposed to validate the application of the proposed methods for different operation points and considering different parameters of the analyzed converters. For these calculations, method 3-B is applied and only one parameter is changed at a time.

Firstly, the losses for the MMC are calculated considering different operating points. Fig. 18 shows the switching losses for different active and reactive power ratings. The limits of 200 MVar are applied in order to not exceed the RMS current limits of the chosen semiconductor power device. In this case, 45 operating points are calculated. When analyzing the losses for unitary power factor, it is possible to see that the switching losses per arm are around 0.03% of the converter nominal power. However, no clear conclusions could be set regarding the reactive power. For this purpose, a detailed analysis considering the variation of the power factor with more operating points would be needed.

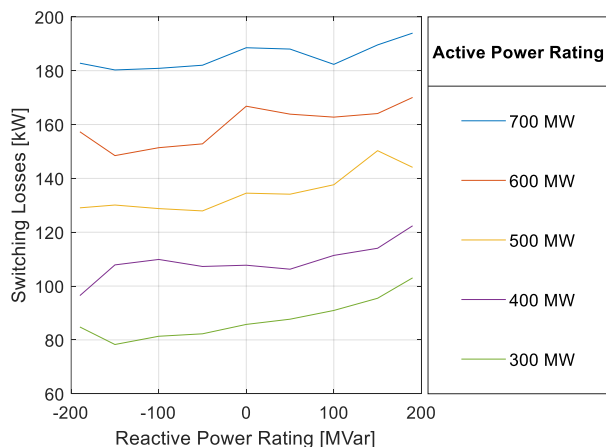


Fig. 18 – Switching losses on MMC converter considering different operating conditions.

Furthermore, a sensitivity study is performed considering the variation of certain parameters. Among the parameters considered in this study, only the arm inductance and the submodule capacitor can be directly adjusted. The other

parameters, such as the number of submodules, the voltage levels and the submodule operating voltage are directly dependent on the choice of the power semiconductors installed on the converter, which is fixed in this study in order to be able to compare the losses properly.

In this case, the losses are calculated varying the arm inductance and the submodule capacitor for the studied converter topologies from 50% to 100% of their nominal values as defined in Table I. This way, Table IV shows the results for the losses on the MMC topology, while

Table V shows the results for the losses on the DC-MMC topology. The variation of the inductances in both cases does not produce a clear effect on the switching losses. However, the decrease of the submodule capacitance in both cases leads to increased switching losses. The reason for that may be that with the same balancing control algorithm parameters, the submodules reach the voltage limits with less time, causing more insertion and bypass action, thus, increased switching losses.

Table IV  
Losses varying one parameter at a time according to the nominal value for the MMC

(% of nominal value)	Losses varying the arm inductance according to the nominal value [kW]	Losses varying the submodule capacitor to the nominal value [kW]
50	183.2	270.1
60	179.1	239.3
70	185.8	218.8
80	189.6	213.6
90	194.3	187.0
100	188.5	188.5

In this analysis, 69 different losses calculations were done within around 150 minutes or 2.5 hours of computing time. If the same results were to be produced by the reference method (method 1) and considering the computing time shown in Table I, more than 1300 hours would be needed, the equivalent of around 2 months of calculation without considering any post-treatment of the results.

Table V  
Losses varying one parameter at a time according to the nominal value for the DC-MMC

(% of nominal value)	Losses varying the arm inductance according to the nominal value [kW]	Losses varying the submodule capacitor according to the nominal value [kW]
50	151.3	283.2
60	152.6	252.6
70	152.3	218.5
80	151.7	193.3
90	151.8	169.3
100	151.8	151.8

## VII. CONCLUSIONS

This paper proposed a method to estimate switching losses in power converters based on submodule stacks. The proposed method is based on time-domain simulations and data treatment of a set of semiconductors in a given submodule stack. Two case studies were shown, considering MMC and DC-MMC topologies. Four switching losses calculation methods were applied: a reference method, an analytical method (most-common method in the literature) and two variants of the

proposed method. Proposed method A considered the data of a single submodule of a stack while method B considered the totality of submodules. Results show a good balance between accuracy and time required for the proposed methods, and poor accuracy for the analytical method. For MMC, method A and B presented equivalent accuracy. Since method A requires 50% less time to accomplish losses calculation, this method is suitable for this converter. In the case of DC-MMC, a difference of 20% between method A and method B was identified, making method B more accurate. It was shown that this behavior is caused by the distribution of losses between different submodules in the stack. In this case, the distribution of losses of the considered DC-MMC presents higher standard deviations compared to MMCs within the same time simulation, requiring long-time simulations to reach the same level of standard deviation. This way, choosing randomly one submodule to calculate the overall stack losses results either in high imprecisions for DC-MMC or in very time-demanding calculations. For this converter, method B should be prioritized. A sensitivity analysis was performed showing that the switching losses increase when increasing the transmitted active power and when decreasing the submodule capacitance. Considering the instantaneous submodule voltage, instead of the average capacitor voltage, can be explored as a further study to improve the accuracy of the proposed method. The proposed method also allowed to highlight that the considered balancing control algorithm is not always able to balance switching losses among the submodules of a stack in a reasonable duration, questioning its pertinence for some applications. Further studies on low-level controls can be performed. In this matter, different balancing control algorithms with different variations in the submodule stack such as changes on individual capacitors, can be evaluated rapidly, calculating the switching losses using the proposed method 3B, which can improve the efforts needed. For further works, it can be also noted that, for the cases where the computation of losses using only one submodule is valid, the post-processing stage can be done using another approach. For instance, coupled electro-thermal simulation could be considered. In comparison with method 1, the main advantage and difference would be that only one submodule is modeled in detail leading then to a dramatic computational effort reduction.

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## IX. BIOGRAPHIES



**Benhur Zolett** received the engineer degree of the Ecole Centrale de Lyon, Lyon, France, in 2020, with a double degree in Energy Engineering from the Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil. His research was mainly focused on power quality aspects of renewable energy integration in high voltage grids. In 2020, he joined SuperGrid Institute, France, as R&D engineer on power conversion solutions for medium and high voltage direct current systems. Currently, his focus is on developing collaboration frames with industrial and academic partners of SuperGrid Institute towards the development of power electronics technologies for medium and high voltage direct current applications.



**Juan Paez Alvarez** received the bachelor’s degree in electronics engineering from the National University of Colombia in 2013 and the master’s degree in electrical engineering from the National Institute of Applied Sciences in France in 2015. He received a PhD degree from the University of Grenoble Alpes, France in 2019 thanks to his works on DC-DC converters for HVDC applications. He worked in the SuperGrid research institute in Lyon from 2015 to 2022 mainly on power conversion for medium and high voltage DC networks. He is now working at OPAL-RT Technologies as an electrical modelling and simulation specialist in power electronics for HVDC and FACTS. His current research focuses on modelling, control, and real-time simulation of power converters.



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**Florent Morel** (S’06–M’07–SM’15) is an alumnus of École normale supérieure (ENS) de Cachan, France. In 2002, he obtained his “agrégation” in Electrical Engineering and he received an MSc in Electrical Engineering from INSA de Lyon, France in 2004. He pursued his PhD at INSA de Lyon on the control of electrical drives. He considered especially the association of a permanent magnet synchronous machine with a three-phase matrix converter. From 2007 to 2019, he was Associate Professor at École Centrale de Lyon and the Ampère Laboratory. He taught electrical engineering and power electronics. His research activities focused on power electronics converter design. He especially considered electromagnetic compatibility (EMC), use of silicon carbide devices, power supply of circuits with a high-voltage insulation and converters for high voltage grids (including railway). He is currently with Supergrid Institute, Villeurbanne, France. He is working on converters for HVDC applications.