



Failure Degradation Similarities on Power SiC MOSFET Devices Submitted to Short-Circuit Stress and Accelerated Switching Conditions

Joao Oliveira, Pascal Frey, Hervé Morel, Jean-Michel Reynes, Jérémie Burky, Fabio Coccetti, Francesco Iannuzzo, Michel Piton

► To cite this version:

Joao Oliveira, Pascal Frey, Hervé Morel, Jean-Michel Reynes, Jérémie Burky, et al.. Failure Degradation Similarities on Power SiC MOSFET Devices Submitted to Short-Circuit Stress and Accelerated Switching Conditions. Microelectronics Reliability, 2023, 148, pp.115166. 10.1016/j.microrel.2023.115166 . hal-04316701

HAL Id: hal-04316701

<https://hal.science/hal-04316701>

Submitted on 30 Nov 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Failure Degradation Similarities on Power SiC MOSFET Devices Submitted to Short-Circuit Stress and Accelerated Switching Conditions

J. Oliveira^{a,*}, P. Frey^a, H. Morel^b, JM. Reynes^a, J. Burky^c, F. Coccetti^a,
F. Iannuzzo^d, M. Piton^{a,e}

^aIRT Saint Exupéry, Toulouse, France

^bUniv Lyon, INSA Lyon, UCBL 1, Ecole Centrale Lyon, CNRS, AMPERE F-69621, Lyon, France

^cAlter Technology, Toulouse, France

^dAAU Energy, Aalborg, Denmark

^eAlstom, Séméac, France

Abstract

The aim of this paper is to present a comparison between failure analyses results performed on power SiC devices. Various devices have been submitted to SC (Short-circuit) stress and ITASC (Inverter Test with Accelerated Switching Conditions) method. Some similarities have been detected, as well as the same failure mode represented by a gate-source shorted-circuit.

1. Introduction

Future electrification demands drastic improvements in power electronics by enhancing power density and efficiency, without a negative impact on reliability and lifetime for the industry and transport sectors like automotive, railways, aeronautics, and electric grids. High reliability and large robustness in extreme conditions are among the first requirements for power devices, including extreme operations [1]. However, both the lack of insight into SiC MOSFETs specific failure-mechanism and ad-hoc tests covering real mission profiles are hindering their extensive adoption.

SiC MOSFETs present a significantly lower specific on-resistance (Ωcm^2) compared to silicon counterparts. Moreover, a higher short-circuit current is observed, which generates very high temperatures in a few microseconds [2]. The same holds for the current density through bond wires, ending up in a systematic overcurrent through them [3].

A lot of studies has been already done on this topic, including extensive accelerated testing. Thus, it is well-known that degradation mechanisms occur on SiC MOSFETs caused by short-circuit events, and hard switching conditions.

In this paper, repetitive SC have been performed

to lead the SiC device to failure, however not in complete destruction of the DUT (Device Under Test). ITASC method is used to define a hard switching condition up to device degradation. The operation point is located within SOA (Safe Operating Area) limits. An internal visual inspection have showed a fail-to-open (FTO) of the device, identified by a gate-source shorted-circuit.

2. Repetitive Short-circuit Stress

2.1. DUT and test bench used

This study is performed on ST MicroelectronicsTM device 1200 V, 75 m Ω , 33 A @ $T_{\text{Case}} = 25^\circ\text{C}$ planar-type device, in an automotive-grade 3-lead TO-247 case. The device was placed on the low side of a phase-leg power test bench presented in Fig. 1 [4]. SC tests up to 900 V can be performed with the test bench. A protection system composed of circuit breaker is used to interrupt current in a case of thermal runaway. Gate-source voltage (V_{GS}) and output-drive voltage (V_{buffer}) are measured with a Rohde & Schwarz RT-ZP10-400V, 500 MHz bandwidth probe. Drain-source voltage (V_{DS}) is measured with a Testec HV 250-2500 V, 300 MHz bandwidth probe. Drain-

*Corresponding author. joao.oliveira@irt-saintexupery.com
Tel: +33 6 25 71 40 30;

source current (I_{DS}) is measured through a shunt T&M Research SDN-414-01, 6 J, 400 MHz coaxial shunt. The drop voltage on gate resistance is used to estimate gate current (I_G).

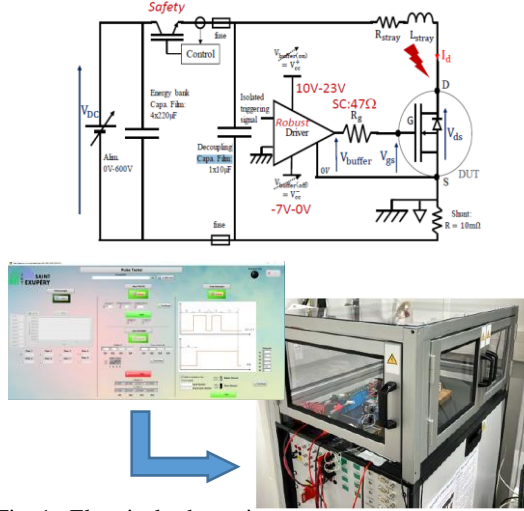


Fig. 1. Electrical schematic of the test bench [1], and the Pulse Tester User Interface developed at IRT Saint Exupery.

2.2. Methodology and experimental results

A repetitive short-circuit test is applied to the DUT with a time between each pulse of 5 seconds. The test conditions are $V_{DS} = 600$ V, $V_{buffer} = -5V/+18V$ and $T_{CASE} = \text{room temperature}$. Previous studies [1, 3] have been performed to estimate the average T_{SCWT} (Short-circuit Withstand Time), about 5 μs . Once this time is found, a percentage of 70% T_{SCWT} (3.5 μs) is set for the pulse width. Thus, a thermal runaway and then a catastrophic drain-source failure-mode are prevented. All tested devices in SC showed gate-source degradation only.

In Fig. 2, the waveforms during a first short-circuit event (#cycle1, blue lines), and the last (#cycle400, red lines), for this test are shown. The abnormal effect (current bump) observed on gate current (I_G) is probably due to an electromagnetic disturbance caused by parasitic elements of the PCB (Printed Board Circuit), and associated common mode current.

The drain-source current peak decay between the first and last cycles is due to the self-heating of the device. A thermocouple is used to monitor temperature increase during repetitive cycles, by ensuring the definition of waiting time. Furthermore, it is important to mention that this effect is not a degradation.

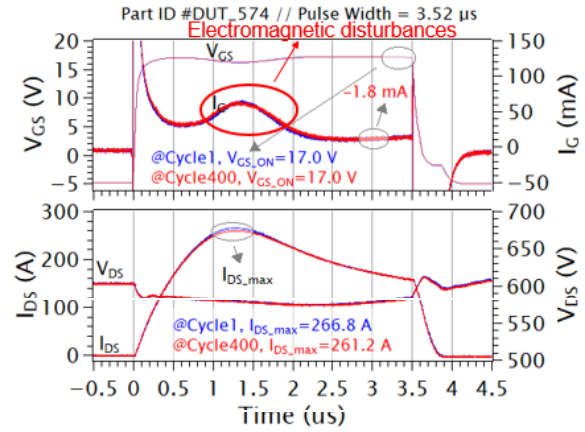


Fig. 2. Gate-source (V_{GS}) voltage, gate current (I_G), drain-source current (I_{DS}), and drain-source voltage (V_{DS}) during short-circuit event.

The gate current is also measured at the final of each pulse (3.5 μs instant) to verify any variation along the repetitive short-circuits. In addition, gate charge is calculated. These results are presented in Fig. 3.

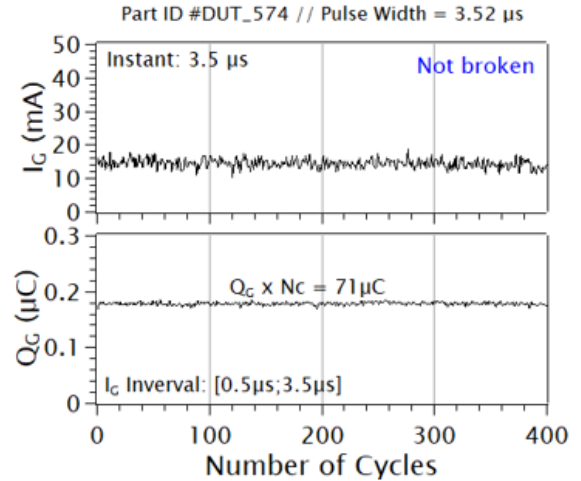


Fig. 3. The gate current (I_G) remains nearly constant between @Cycle1 and @Cycle400. Gate charge (Q_G) about the same 71 μC for 400 cycles.

This test is part of an aging protocol that aims to verify the evolution of static and dynamic parameters such as leakage drain/gate current, output capacitance, etc. Threshold voltage (V_{TH}) presented a maximum variation of about 5%, for example. TDDB (Time-dependent Gate Oxide Breakdown) was not affected after aging.

3. ITASC method

3.1. Test bench used

The DST (Double Source Test) bench is an alternative to classical DPT (Double Pulse Test). It allows to stress a power device through a high voltage/current switching. Thanks to the electrical schematic of the test, it is possible to define a constant value for voltage and current on the DUT [5]. In this way, the main goal is to define an aging law, regarding different stressor parameters, such as: applied voltage/current (up to 1000 V and 100 A), switching speed (R_G), number of cycles ($10^5 \sim 10^6$), negative/positive pre-conditioning, etc. In Fig. 4, the electrical schematic and the mounted test bench are presented.

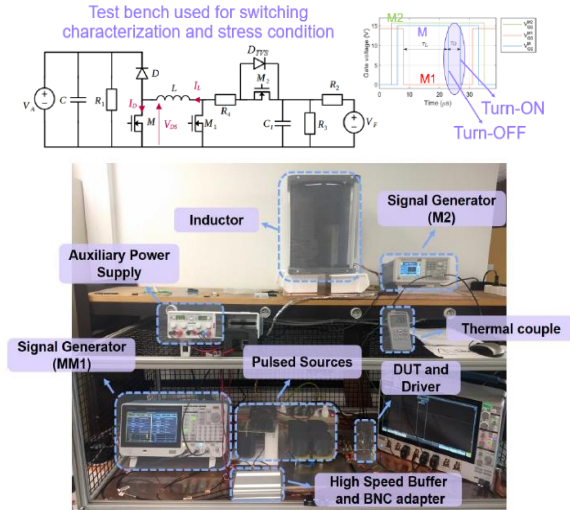


Fig. 4. Electrical schematic of the test bench [4]. This platform is based in Ampere Laboratory in Lyon, and it was developed in collaboration with IRT Saint Exupery.

3.2. Methodology and experimental results

A repetitive hard switching test is performed with the DUT applying a time of 1 second between each pulse. This prevents any self-heating effect. The test conditions are $V_{DS} = 1000$ V, $I_{DS} = 65$ A, $V_{DRV} = -5V/+18V$ and initial temperature $T_{CASE}^1 = \text{room temperature}$, and final temperature $T_{CASE}^2 = 52$ °C. The test bench enables to increase the nominal switching energy by a ratio of 30. The phase of current rise in the DUT corresponds to about 2 ms, and it is also a high stress, however this operation point is inside SOA (Safe Operating Area) limits. In Fig. 5, the target stress condition can be seen. In addition to current rising, a higher gate resistance is also used. Some degradations have been observed for currents

around 65 A at 1000 V. Tests on some specimens in this condition showed a maximum number of cycles of about 100, before total failure of device. In the observed degradations, a short-circuit between gate and source is always detected for all tested devices.

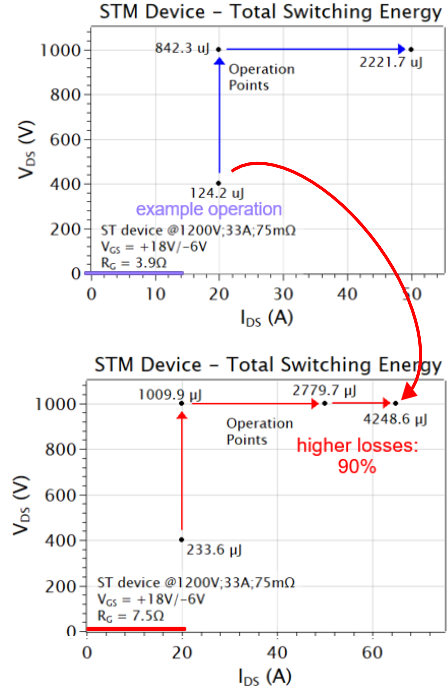


Fig. 5. Switching energy comparison an example operation point (400V/20A), and the hard stress condition (1000V/65A). An increase greater than a factor of 30 is observed for the switching energy.

For lower current values, no static parameters ($R_{ds(on)}$, V_{th} , I_{gss} , I_{dss} , etc) variation was detected. A current of 50 A allows to achieve 200k cycles without degradation. Seen that, the target current is increased until reaching SOA limits. In this case, the device presents total failure without any precursor previously.

Voltage and current waveforms of DUT can be seen in Fig. 6. The total stress is the result of two phase that are the conduction during current rising by inductor, and switching events. Total energy during one cycle of ITASC method has the same magnitude of SC test, some hundreds of milijoules.

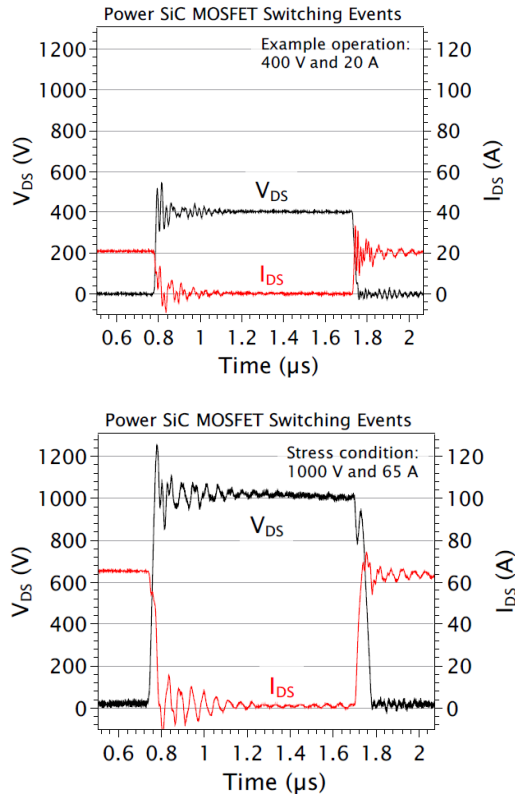


Fig. 6. Switching transients of a Power SiC MOSFET for an example operation point (400V/20A), and the hard stress condition (1000V/65A).

The charging time defined to reach the target current level is also an additional stress. Thus, some tests at low voltage (100 V) but with the same current level have been performed to attempt observing any degradations. The results are presented in Fig. 7. During the test, after 6k cycles the switching is paused to perform a gate leakage current measurement. Thereafter, when the test is re-started, the initial current (at #cycle6000) is monitored and compared to its value at #cycle0. The current remains the same, therefore, there is probably no degradation of ON resistance. As seen in Fig. 7, the device has the same current capability (65 A) after 10k cycles, and none gate leakage current is detected. A preliminary conclusion is that the degradation is due to high power switching about 63 kW (at 1000 V).

Stress condition: $V_{DS} = 100$ V and 65 A

Waiting time = 1 s

- 65A: 0 cycles (T_{CASE} about 24.2°C);
- 64A: 1200 cycles (T_{CASE} about 42.4°C) hot

Waiting time = 0.5 s

- 60A: 6000 cycles (T_{CASE} about 73.4°C) hot
- 65A: 6000 cycles (T_{CASE} about 24.7°C) cold
- 61A: 10000 cycles (T_{CASE} about 67.2°C) hot
- 65A: 10000 cycles (T_{CASE} about 24.9°C) cold

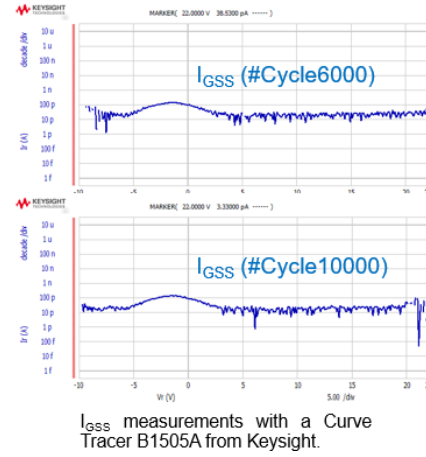


Fig. 7. ITASC method in low voltage level (100 V) applied to a SiC power device. Cold state represents to 10 minutes of waiting time, before re-starting tests.

4. Failure Analysis Comparison

The failure analysis have been performed by Alter Technology Laboratory. After short-circuit stress, an analysis was performed. Four different Aluminum (Al) reconstruction levels were observed at source pad edge and wedge bond edge. The high-power stress applied on the component makes a thermal-mechanical stress on ILD (Inter Layer Dielectric) leading to aluminum propagation in the crack inducing electrical leakage [5, 7]. Fig. 8 shows the crack observed at ILD level after 636 cycles, under the conditions previously mentioned (section 2.2). This generates a path for the melted Al-metallization causing a short-circuit between gate and source.

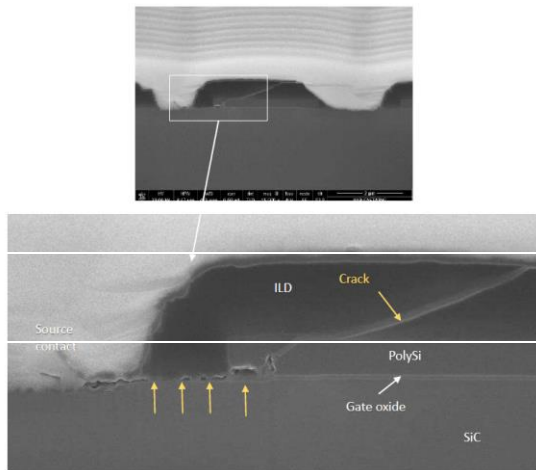


Fig. 8. Fusing point between PolySilicon layer & Source ohmic contact. ILD damaged until Ti barrier.

The metal crack can happen due to a temperature gradient between active and edge area. Two contributors seems to be significant in Al source reconstruction phenomenon: the very high temperature gradient at border of active area, and the melting of source metal in active area. This phenomenon has been already observed in the literature [7, 8]. It is important to mention that SC leads the DUT to operate outside the SOA.

ITASC method allows for a hard stress with 65 kW of power peak on the device, but inside the SOA. After certain failure analysis, it was observed the same failure mode: gate-source short-circuited. However, the mechanism is distinct when compared to SC stress. In Fig. 9, it is possible to see an aluminium migration near of source and gate. This causes the gate-source short-circuit. Furthermore, it is observed Al reconstruction likewise for the SC stress, what shows some similarities. Therefore, it could be estimated a surface temperature near 660 °C, melting point of Al. This is local phenomenon (in the center), and probably if the gate finger was not present, this failure would not arise.

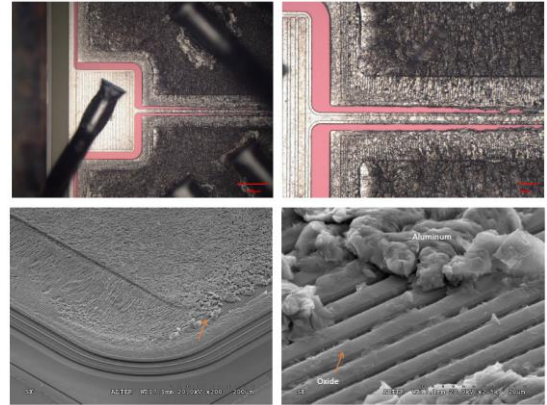


Fig. 9. Aluminum melted and displaced near edge of source gate (orange arrow).

Conclusions

The failure analysis performed on power SiC MOSFET devices after two different stress tests (SC and ITASC) shows a same failure mode: shorted gate-source. It is important to mention that the failure are related to a high dissipated power on the DUT. In addition, for both stresses an aluminum reconstruction has been observed, but not at the same location. After SC events, the Al migration occurs towards the cracked ILD, however after ITASC stress this migration happens on border region of the surface pad, located in center of active area. Thus, both stresses present different failure mechanisms.

Results for ITASC method at low voltage have been presented. This allowed to show that the degradation is only due to the high switching power (65 kW), and not the current charging phase.

Another issue will be to better address in the future the SOA in such short and high power stresses because they strongly differ from those observed in silicon devices.

Acknowledgements

This work was carried out in the framework of the IRT Saint Exupéry's project SiCRET (SiC Reliability Evaluation for Transport). We acknowledge the financial support from the SiCRET's industrial and academic members and the financial support from the French National Research Agency (ANR).

SiCRET's Industrial members: Alstom, Alter Technology, Emotors, Liebherr, Nucletudes, Safran, SuperGrid Institute, Thales, Vitesco Technologies.

SiCRET's academic members: Ampère, LAAS, IES, LAPLACE.

The authors would also like to thank Francesco Pintacuda from STMicroelectronics and ST Microelectronic Automotive Discrete Group (ADG) for the valuable support (components and expertise).

The authors would also like to thank Sylvain Jouanolle from the French MoD (DGA) for the valuable support (physical analysis).

References

- [1] Shoji, T., Kuwahara, M., & Usui, M. (2021). Dependence of short-circuit withstand capability of SiC MOSFETs on short-circuit failure time. *IEEE Transactions on Power Electronics*, 36(10), 11739-11747.
- [2] Romano, G., Fayyaz, A., Riccio, M., Maresca, L., Breglio, G., Castellazzi, A., & Irace, A. (2016). A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(3), 978-987.
- [3] Reigosa, P. D., Iannuzzo, F., Luo, H., & Blaabjerg, F. (2016). A short-circuit safe operation area identification criterion for SiC MOSFET power modules. *IEEE Transactions on Industry Applications*, 53(3), 2880-2887.
- [4] Reigosa, P. D., Iannuzzo, F., & Ceccarelli, L. (2018). Effect of short-circuit stress on the degradation of the SiO₂ dielectric in SiC power MOSFETs. *Microelectronics Reliability*, 88, 577-583.
- [5] Garrab, H., Allard, B., Morel, H., Ammous, K., Ghedira, S., Amimi, A., ... & Guichon, J. M. (2005). On the extraction of PIN diode design parameters for validation of integrated power converter design. *IEEE Transactions on Power Electronics*, 20(3), 660-670.
- [6] Burky, J., Forgerit, B., Barazi, Y., Reynes, J.M., (2021). Failure Analysis on SiC device after short circuit stress. NRTW2021, National Reliability Technology Workshop. Oral presentation without proceedings.
- [7] Cavallaro, D., Pulvirenti, M., Zanetti, E., & Saggio, M. (2019). Capability of SiC MOSFETs under short-circuit tests and development of a thermal model by finite element analysis. In *Materials Science Forum* (Vol. 963, pp. 788-791). Trans Tech Publications Ltd.
- [8] Ceccarelli, L., Reigosa, P. D., Iannuzzo, F., & Blaabjerg, F. (2017). A survey of SiC power MOSFETs short-circuit robustness and failure mode analysis. *Microelectronics Reliability*, 76, 272-276.