New Methodology for Defining Integration Limits Used for Switching Energy Computation in Power Devices

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***Index Terms*—Switching losses, SiC MOSFET, Hard switching, Calculation method, Wide bandgap devices.**

***Abstract*—Switching losses of a power converter is a relevant factor that contributes to total losses. For building an optimized design, it is essential to accurately estimate switching energy in order to define certain parameters such as maximum operating frequency and cooling system. Power SiC MOSFETs have high switching-speed capability, thus the voltage and current alignment should be performed carefully during classical dynamic characterization methods. In addition, the definition of integration limits of instantaneous power during switching events can generate erroneous results. In this paper, a new methodology for switching energy computation is proposed and validated for different manufacturers. This method**

is less sensitive to oscillations on voltage and current waveforms with respect to other classical methods.

I. Introduction

Accurate switching energy measurement is essential to design power converters, especially those operating in high switching frequency. In addition, cooling system volume is directly impacted by the amount of dissipated energy [1]. Energy stored in the output capacitance of power SiC MOSFETs is much lower than that for MOSFETs based on Si material, which yields lower switching losses and higher efficiency in hard switching applications. However, this is also a source of spurious measurements of switching losses due to the resonance effect between capacitance and inductance elements associated to the test bench, and the power device [2]. High frequency oscillations in the device, current and voltage, are found and become hard to separate the reactive power and the real dissipated power on the device under test. Classical methods for defining integration limits of device's instantaneous power have short integration duration, therefore they are often sensitive to these oscillations.

Different criteria act on limits integration definition of power signal. Reliability tests performed on SiC devices, especially on gate level, can generate voltage and current waveforms distortion during switching events [3]–[5]. During most of these tests, switching energy evolution is monitored according to an applied stress, thus an accurate measurement should be ensured. This can lead to erroneous switching energy measurement, depending on the considered initial and final switching instants.

This paper proposes a new methodology for defining limits integration used to switching energy computation. This method is less sensitive to oscillations on voltage and current waveforms with respect to other classical methods. Thus, compared to classical methods, the proposed methodology is more adapted to compute switching energy after aging tests. To validate this approach, switching energy is calculated before and after the reliability test GSS (Gate Switching Stress) [6].

II. Switching Energy Computation

The DPT (Double Pulse Test) is widely used to analyze switching behavior of power devices, due to its simple circuit implementation [7], [8]. The main focus of the DPT is to characterize the dynamic performance, and performs switching energy measurements. The turn-ON switching energy (E_{on}) and turn-OFF switching energy (E_{off}) are calculated by the integral of the drain-source voltage (V_{DS}) and drain-source current (I_{DS}) product, over on-transient (t_{on}) and off-transient t_{off}, respectively [9]. The key points for accurate E_{on} and E_{off} calculation when DPT bench is used are: switching V-I timing alignment and integration limit definition of the power switching. Thereby, inaccurate measurements of switching energy can be associated to probe delays and bandwidth of instruments, and also to erroneous integration limit definition on switching power signal [7]. WBG devices are more sensitive than Si-based devices due to their high-speed transients. Thus, even some nanoseconds of misalignment between voltage (V_{DS}) and current (I_{DS}) waveforms can generate significant error.

Delay compensations are widely discussed in the literature. In [10], the deskew is performed by using a common square waveform generated by a function generator. One probe is used as baseline, and the other (voltage or current probe) is adjusted to align its rising or falling edge. DPT circuit is modified in [11] by removing the inductor and replacing the diode with a low inductance resistance. This allows for performing the deskew between voltage and current probes.

The total switching energy ($E_{SW\_total} = E_{on}+E_{off}$) measured in DPT can be used to estimate switching losses. However, it is known that E_{on} and E_{off} are not exactly the energy lost during turn-ON and turn-OFF, mainly because of the energy stored in the semiconductor device output capacitance (C_{OSS}). However, the integration over a switching period of the power corresponds well to the switching losses. This is due to the fact that over a cycle, the stored energy at the beginning and at the end of the cycle are the same, as the definition of a cycling system [12].

Based on a half-bridge power module, reference [7] proposes calculating the difference between the input energy supplied by a DC capacitor and the output energy stored in a load inductor. However, this method takes into account a system without resistive losses, that can imply to an erroneous total switching energy.

A Modified Opposition Method was proposed in [2] as a non-intrusive method for switching energy computation. It consists of an indirect measurement, in which four similar devices are tested in a full-bridge configuration through a test bench with accurately characterized elements. This method requires an accurate estimation of dissipated energy associated to circuit elements.

For this paper, an alternative to DPT bench is used. This new test bench allows to reduce total time the DC bus voltage is applied to the DUT, consequently it

reduces the stress on DUT during switching characterization. More details will be presented in Section III.

A. Integration Limit Criteria

The definition of start and end points used to define integration limits on power signal ($V_{DS}I_{DS}$ product) is a major challenge associated to DPT analysis [13]. Depending on the considered initial and final switching instants, different energies can be calculated. In Table I, three methods from manufacturer application notes are presented for integration limit definition applied to power SiC MOSFETs.

TABLE I
INTEGRATION LIMIT DEFINITION ACCORDING TO DIFFERENT MANUFACTURERS.

Integration Limit Definition Based on V_{DS} and I_{DS} curves				
Manufacturer	**Turn-ON**		**Turn-OFF**	
	Start	End	Start	End
Rohm [14] (Method A)	10% final V_{GS}	10% initial V_{DS}	90% initial V_{GS}	90% final V_{DS}
Wolfspeed [15] (Method B)	10% final I_{DS}	10% initial V_{DS}	10% final V_{DS}	10% initial I_{DS}
Infineon [16] (Method C)	10% final V_{GS}	2% initial V_{DS}	90% initial V_{GS}	2% initial I_{DS}

Guidelines to select the integration limits cannot be universally applied for all SiC MOSFETs. A device with low rating current can have strong oscillations on gate input, therefore an integration window defined by use of gate-source voltage can generate spurious results, as it will be shown in Section V.

III. Test Bench for Switching Energy Measurements

The DST (Double Source Test) bench is an alternative to DPT that allows to stress a power device through high voltage/current switching. In Fig. 1 and Fig. 2, the electrical schematic and the used test bench are presented, respectively. With this test bench, it is possible to define independent applied values for the voltage and current on the DUT [17]. In this way, the main goal is to perform switching characterization, i.e. switching energy measurement, with the possibility of varying several parameters, such as applied voltage/current (up to 1000 V and 100 A), switching speed (by changing gate resistance R_G), negative/positive applied gate voltages, etc. Signal generators are used to control the switches of the pulsed current source and the DUT. Switching signals are led to each gate driver boards by means of optical fiber. An auxiliary power supply is used to generate two different voltage levels: 12 V (for driver PCB) and 5 V (for optical isolator PCB). Two power supplies (not seen in Fig. 2) are used to define the required voltage (V_A) and current I_L, which depends on (V_F).

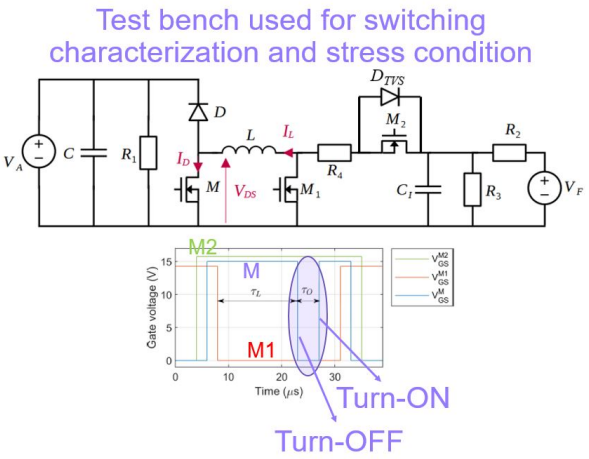

Fig. 1. Electrical schematic of double source test.

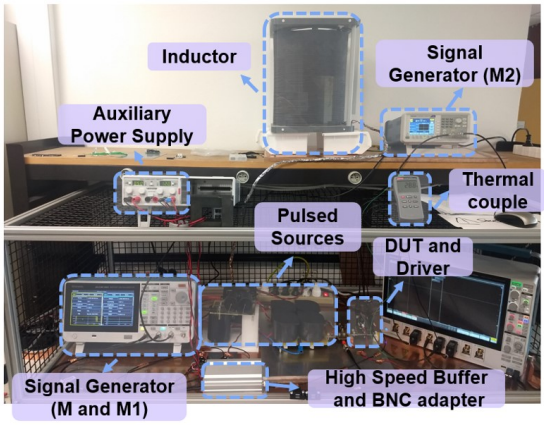

Fig. 2. DST bench used for switching characterization.

For the experimental tests shown in section V, three 1200 V SiC MOSFETs from different manufacturers were used. In Fig. 3, experimental waveforms of voltage and current on a SiC MOSFET can be seen. These signals were extracted from the DST bench and will be used as reference to present the new methodology for switching energy computation.

IV. New Proposed Methodology

Classical measurement precautions have to be taken in order to ensure large bandwidth by using suitable instruments for high speed signals. Moreover, the delay compensation between voltage and current probes is performed based on the propagation speed of traveling waves through the transmission line [18], [19]. Integration intervals, as shown in Table I, are usually defined

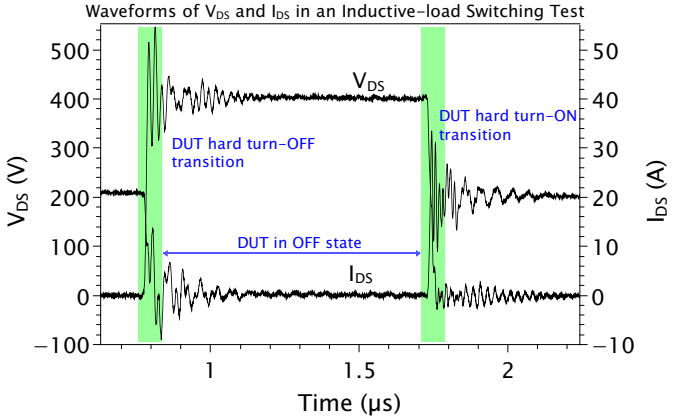

Fig. 3. Waveforms of drain-source voltage and drain-source current in an inductive-load switching test. Green areas highlight the switching transient fronts.

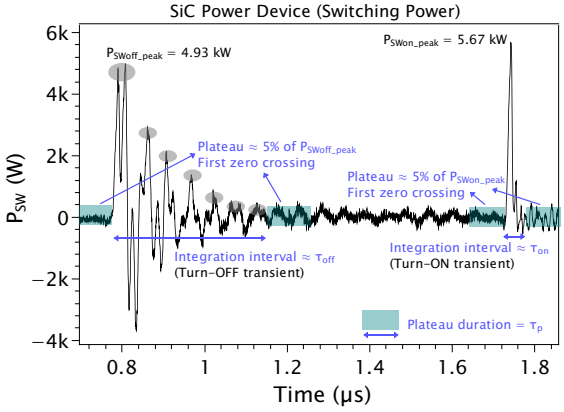

Fig. 4. Instantaneous switching power of a SiC device. The criteria used to define the new integration intervals define a plateau. Parameters: $\tau_{off} = 400\,ns$, $\tau_{on} = 40\,ns$, and $\tau_p = 40\,ns$ (adjustable). The number of positive areas (gray ellipses) is also a reference.

based on drain-source voltage and current waveforms. This can lead to some inconsistencies when high oscillations are observed due to the fast switching transients. In addition, common-mode disturbances may cause abnormal effects on waveforms. Thus, the integration limit definition is very sensitive to all elements around the DUT.

The new proposed methodology, the Plateau Limits based Energy Computation (PLEC), is based on the switching power signal, as seen in Fig. 4. A plateau is defined by a flat part of a signal. It is described as a signal part included in a rectangle whose main parameters are a minimum width (duration) and a maximum height (fluctuation). The integration period of switching power signal is specified using plateau definition. The vertical fluctuation is set to 5% of the peak power in OFF or ON state. This parameter is experimentally validated by analyzing the primitive integral of power signal. It is important that the plateau duration is compatible with switching speed of the device, otherwise conduction losses will be taken into account in the switching energy computation.

Integration interval is defined by two points that correspond to two plateaus of 5% of the peak power. Inside the plateau, any integration interval produces a very similar energy. Thereby, this method is less sensitive to disturbances on voltage and current waveforms. Final integration point of the boundary should respect the plateau, where oscillations are nearly constant. The primitive integral of power signal corresponds to the switching energy. It was calculated for turn-OFF and turn-ON events, as can be seen in Fig. 5 and Fig. 6, respectively.

During turn-OFF transient, the oscillations are mainly due to a resonance between common-mode capacitance and output capacitance of DUT (C_{OSS}), and power loop inductance. This corresponds to an oscillating reactive energy stored essentially on the DUT, and it can cause erroneous measurements whether a short integration boundary is considered. After the plateau, it is possible to see a slight increase of the switching energy related to this phenomenon, as seen in Fig. 5.

For turn-ON transient, the parasitic capacitance discharging increases the power peak. In addition, at the end of the switching event, fewer oscillations are detected. After the plateau, the primitive integral has a negative slope due to a negative switching power, as seen Fig. 6. This is mainly related to an inaccurate measurement of the drop voltage on DUT during ON state, which can be compensated on signal post-processing.

PLEC method is based on power signal integral, and the final limit it is defined when minimum fluctuation of plateau is observed. This ensure that only switching losses is considered for computation. By definition of a plateau, a small change of a integration boundary inside a plateau do not change significantly the value of the computed switching energy.

V. Comparison of the Different Methods

PLEC methodology is compared to the methods mentioned in Table I. In order to have a better understanding of the difference on integration limits on power signal of a SiC MOSFET device, it is plotted, from experimental measurements, the drain-source voltage (V_{DS}) and current (I_{DS}), and gate-source voltage (V_{GS}), with the integration limits for three classical methods and the PLEC method. These results are shown in Fig. 7

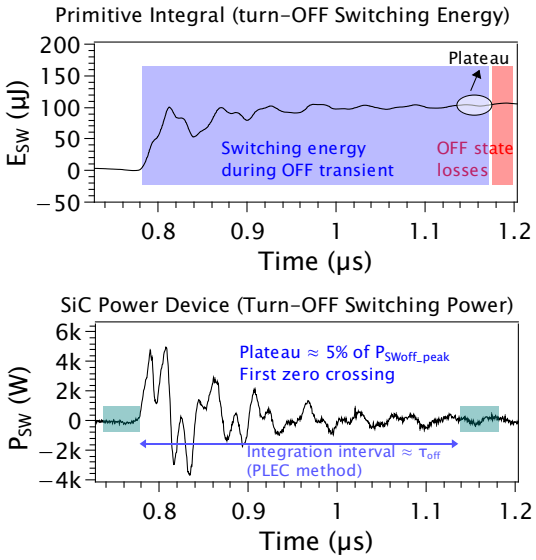

Fig. 5. Primitive integral of switching power during turn-OFF event. Parameters: $\tau_{off} = 400\,ns$.

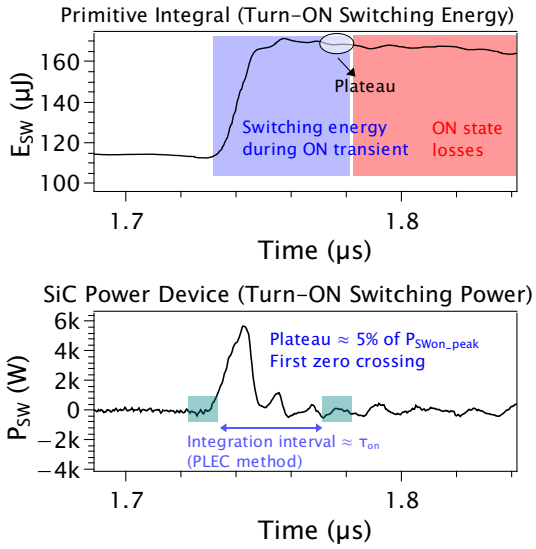

Fig. 6. Primitive integral of switching power during turn-ON event. Parameters: $\tau_{on} = 40\,ns$.

and Fig. 8. It is important to mention that the measured V_{GS} is not the real signal at die level, but the voltage at the TO-247 terminals, which has higher oscillations than the real V_{GS} at die level [12]. Thereby, methods for integration limits definition based on V_{GS} signal can generate spurious results. Oscillations seen in Fig. 8 are mainly due to the strong coupling between power and gate loops, given that the used device has a 3-leads package, and also to common-mode current introduced by probe. The use of optically isolated probe could reduce these oscillations.

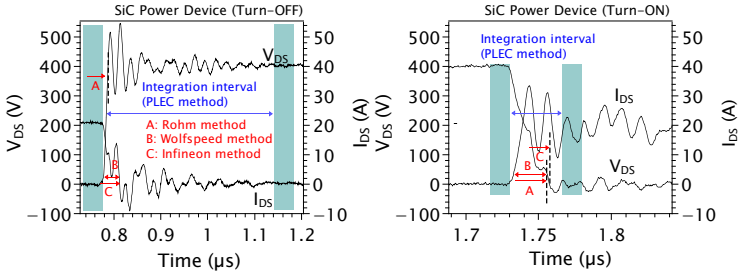

Fig. 7. Waveforms of drain-source voltage and drain-source current during turn-OFF and turn-ON events. Red arrows correspond to the integration limits for the methods A and B, and the final integration limit for the method C.

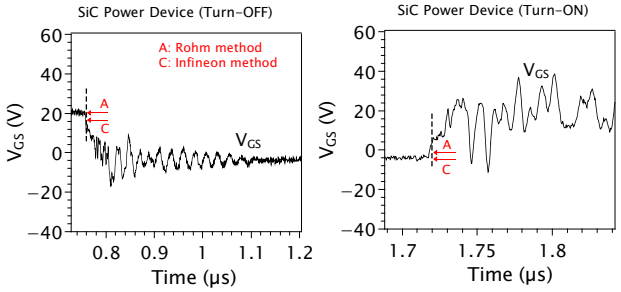

Fig. 8. Waveforms of gate-source voltage during turn-OFF and turn-ON events. The red arrows correspond to the initial integration limit for the method A and C.

The instantaneous power curve is generated after delay compensation performed between voltage and current probes. The integration limits on switching power according to each discussed method are depicted in Fig. 9, and Fig. 10.

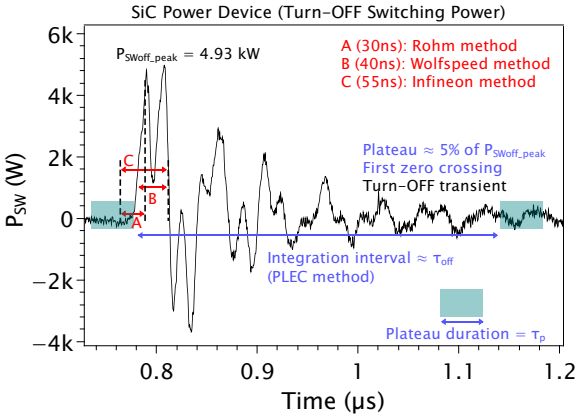

Fig. 9. Switching power during turn-OFF event. The red arrows correspond to the integration limits for the methods A, B, and C. The blue arrows correspond to PLEC method. Parameters: $\tau_{off} = 400\,ns$, and $\tau_p = 40\,ns$ (adjustable).

Comparison between the methods found in the literature, limited to 3 cases in this proposed study, and

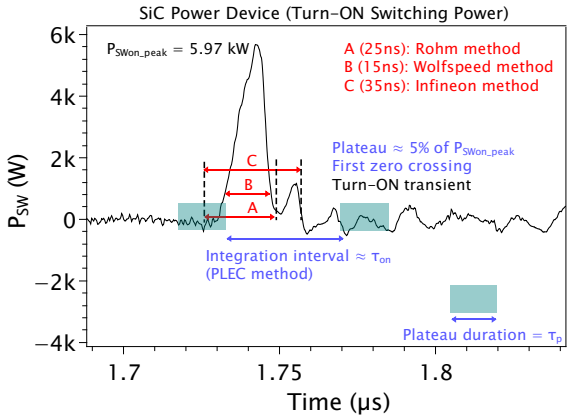

Fig. 10. Switching power during turn-ON event. The red arrows correspond to the integration limits for the methods A, B, and C. The blue arrows correspond to PLEC method. Parameters: $\tau_{on} = 40\,ns$, and $\tau_p = 40\,ns$ (adjustable).

the PLEC method shows a large difference regarding the integration interval. A short integration period can be highly sensitive to oscillations due to the test bench or measurement instruments used during the tests. The insensitivity to oscillations is essential when it comes to aging tests that can modify harmonics on voltage and current waveforms. The device can have the same behavior, thereby presenting nearly the same total switching energy, but in a condition with sightly different oscillations.

Comparison between the mentioned methods, and the PLEC method for switching energy computation are presented in Table II, Table III, and Table IV. Three different power SiC MOSFETs, regarding rating current and manufacturer, are considered. Method A presents the highest deviation regarding the other methods. This is essentially due to the fact that integration limits definition is related to both V_{GS} and V_{DS} signals.

For device 1, the difference between total switching energy calculated by the PLEC method and others is very low. This is due to fact that this device presents lower oscillations among tested components. Device 2 presents the highest deviation which is about 38% regarding the PLEC method, when compared to the average value of total switching energy computed using methods A, B, and C. For device 3, a deviation of about 28% is observed.

TABLE II
COMPARISON OF SWITCHING ENERGY COMPUTED ACCORDING TO DIFFERENT METHODS FOR A POWER SIC MOSFET (1200V;33A).

DEVICE 1				
Operation Point (400V;20A)	Method A	Method B	Method C	PLEC
Turn-ON Energy (µJ)	52.1	52.7	57.9	56.5
Turn-OFF Energy (µJ)	19.1	95.7	99.9	103.6
Total Switching Energy (µJ)	71.2	148.5	157.7	160.1
Total Switching Energy variation regarding PLEC	0.44	0.93	0.99	1.00

TABLE III
COMPARISON OF SWITCHING ENERGY COMPUTED ACCORDING TO DIFFERENT METHODS FOR A POWER SIC MOSFET (1200V;38A).

DEVICE 2				
Operation Point (400V;20A)	Method A	Method B	Method C	PLEC
Turn-ON Energy (µJ)	61.7	61.7	62.0	65.9
Turn-OFF Energy (µJ)	14.3	46.4	45.4	90.8
Total Switching Energy (µJ)	76.1	108.1	107.4	156.7
Total Switching Energy variation regarding PLEC	0.49	0.69	0.69	1.00

TABLE IV
COMPARISON OF SWITCHING ENERGY COMPUTED ACCORDING TO DIFFERENT METHODS FOR A POWER SIC MOSFET (1200V;4.7A).

DEVICE 3				
Operation Point (400V;20A)	Method A	Method B	Method C	PLEC
Turn-ON Energy (µJ)	19.4	19.0	19.7	19.6
Turn-OFF Energy (µJ)	37.1	67.2	67.4	86.9
Total Switching Energy (µJ)	56.5	86.2	87.1	106.5
Total Switching Energy variation regarding PLEC	0.53	0.81	0.82	1.00

VI. METHOD VALIDATION AFTER AGING TEST

Switching energy is often used as monitoring parameter during aging tests. Thereby, accurate measurements are essential to detect possible degradations. GSS reliability test is applied on several samples of a power SiC MOSFET, and total switching energy is computed based on different methods presented in this paper. The goal is to perform a comparison between PLEC and other methods, before and after aging phase. The total time of stress test is 4000 hours, and the devices are stressed

under two different temperatures that are 125 °C and 200 °C. In Fig. 11 and Fig. 12, the results are presented and compared to fresh devices (without stress).

After GSS test at 125 °C, method A presents higher losses when compared to after GSS test at 200 °C, which seems to be curious. Methods B and C do not reveal same trending after stress period at high temperatures. They present negative variation for the stress at 125 °C, and positive variation at 200 °C. Considering PLEC method, the energy variation after GSS test at 125 °C and 200 °C is about 3% and 10%, respectively. Higher oscillations found after stress period can modify integration limits, and thus generate erroneous measurements of switching energy. Proposed methodology presents more accuracy because the limits definition on power signal is more strictly defined, given that it is based on peak power and plateau definition.

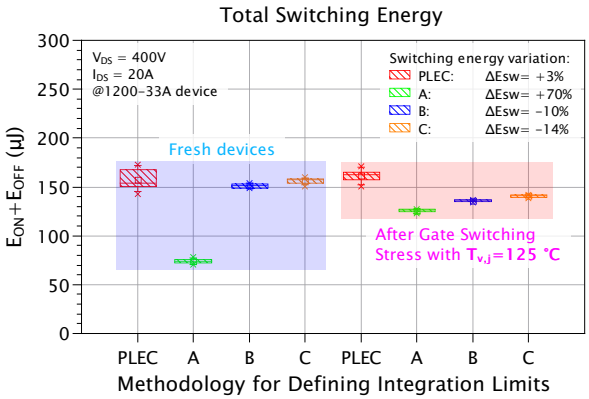

Fig. 11. Total switching energy according to PLEC, A, B and C methods. GSS test is performed with devices under 125 °C.

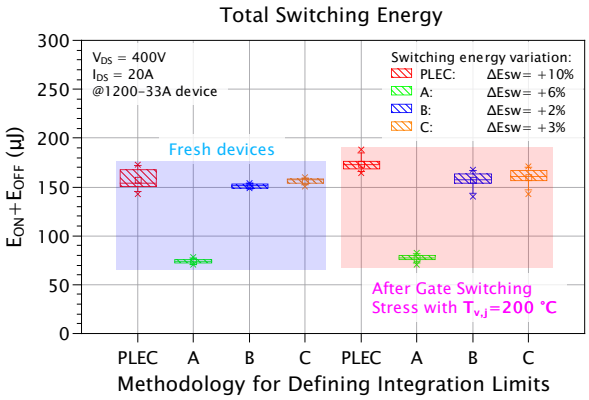

Fig. 12. Total switching energy according to PLEC, A, B and C methods. GSS test is performed with devices under 200 °C.

VII. Conclusion

A new methodology (PLEC) for integration limit definition for switching energy computation in SiC power devices was proposed. This new method is based on the primitive integral of the switching power ($V_{DS}I_{DS}$ product). A plateau is used as criterion for defining initial and final integration limits, by ensuring low dispersion of switching energy if the limits remains inside the plateau. The proposed method presents less sensitivity to oscillations when compared to classical methods found in the literature. This is essential, for instance, to correctly estimate switching energy when aging tests are applied to the DUT that can modify switching waveforms.

The PLEC method was defined and compared to classical methods using experimental waveforms from characterization of three different devices. After stress test applied on one device, switching energy was computed using these four different methods. PLEC method presented more coherent results regarding GSS stress in different temperatures.

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