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Youssef Hamdaoui, Idriss Abid, Sondre Michler, Katir Ziouche, F Medjdoub. Demonstration of avalanche capability in 800 V vertical GaN-on-Silicon diodes. *Applied Physics Express*, 2023, 17 (1), pp.016503. 10.35848/1882-0786/ad106c . hal-04313786

**HAL Id: hal-04313786**

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Submitted on 29 Nov 2023

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To cite this article before publication: Youssef Hamdaoui *et al* 2023 *Appl. Phys. Express* in press <https://doi.org/10.35848/1882-0786/ad106c>

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## Demonstration of avalanche capability in 800 V vertical GaN-on-Silicon diodes

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High-quality pseudo-vertical p-n diodes using a GaN-on-silicon heterostructure are reported. An optimized fabrication process including a beveled deep mesa as edge termination and reduced ohmic contact resistances enabled high on-state current density and low on-resistance. A uniform breakdown voltage was observed at 830 V. The positive temperature dependence of the breakdown voltage clearly indicates the avalanche capability, reflecting both the high material and processing quality of the vertical p-n diodes. The Baliga figure of merit, around 2 GW/cm<sup>2</sup>, which is favorably comparable to the state-of-the-art, combined with avalanche capability paves the way for fully vertical GaN-on-Silicon power devices.

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3 As part of the development of next generation low-cost power devices, GaN-based high  
4 electron mobility transistors (HEMTs) stand out as an undeniable candidate due to their high  
5 electric field, high electron mobility, and large band gap<sup>1-5</sup>). In addition to its physical  
6 properties that exceed the limitations of silicon, GaN technology is cost-effective when  
7 grown on silicon (Si). While lateral GaN HEMTs have demonstrated high performances up  
8 to 900 V voltage operation, several challenges still plague the widespread use of this  
9 technology, including:

- 14 1. Electron trapping caused by complex hetero-epitaxy and surface states.
- 15 2. Destructive breakdown (in contrast to avalanche), resulting from the peak electric  
16 field at the vicinity of the gate terminal.
- 17 3. Relatively large device size due to the substantial gate-to-drain distance required  
18 to increase the breakdown voltage.

23 On the other hand, vertical GaN architectures offer the potential to overcome these  
24 limitations<sup>6,7</sup>). A vertical structure takes advantage of junction-based N- and P-doped  
25 epitaxial layers, leading to a better distribution of the electrical field enabling to avoid peak  
26 electric field and charge trapping issues<sup>8-16</sup>). The device breakdown voltage scales with the  
27 drift layer thickness, allowing small fingerprints. Furthermore, it has been demonstrated by  
28 several groups that fully vertical GaN structures grown on GaN bulk substrate or pseudo-  
29 vertical devices on sapphire substrate exhibit avalanche breakdown capability<sup>17-20</sup>).  
30 Nevertheless, for widespread market adoption, a cost-effective substrate such as silicon  
31 would be preferred. Recently, pseudo-vertical GaN-on-Si p-n diodes have been  
32 demonstrated, as well as fully vertical GaN-on-Si device proof of concept<sup>21-27</sup>). However,  
33 the avalanche breakdown capability has not yet been proved, even though it is a crucial  
34 feature required for power electronic devices. Indeed, avalanche capability ensures a non-  
35 destructive behavior close to the breakdown region and thus enhances the device robustness,  
36 and reliability of the overall system. Sidewall parasitic leakage current through the mesa,  
37 high dislocation density within the GaN drift layer, and point defects are some of the issues  
38 that lead to destructive and non-uniform breakdown, which is a significant barrier to  
39 achieving avalanche capability in GaN-on-Silicon based power devices<sup>7</sup>).

42 In this letter, pseudo-vertical GaN-on Si p-n diodes with a drift layer thickness of 4.5  $\mu\text{m}$ ,  
43 are discussed. Uniform breakdown with avalanche capability around 800V, and low on-  
44 resistance ( $R_{\text{on}}$ ) is achieved, reflecting the high material quality.

51 The heterostructure was grown by metalorganic chemical vapor deposition (MOCVD)

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3 on 6-inch silicon substrate. A schematic cross-sectional diagram of a vertical GaN-on-Si p-  
4 n diode is shown in Fig. 1(a). The growth process began with a proprietary buffer layer stack,  
5 followed by a 800-nm thick n+ GaN Si-doped layer ( $5 \times 10^{18} \text{ cm}^{-3}$ ), a 4.5- $\mu\text{m}$  thick n-type (Si-  
6 doped) drift layer ( $3 \times 10^{16} \text{ cm}^{-3}$ ) and a 700-nm thick p-type GaN Mg-doped layer ( $5 \times 10^{19}$   
7  $\text{cm}^{-3}$  with  $3 \times 10^{17} \text{ cm}^{-3}$  hole concentration). Capacitance–voltage (C-V) measurements were  
8 performed on the diodes in order to confirm the net ionized doping concentration in the drift  
9 region, which was found to be  $\sim 9 \times 10^{15} \text{ cm}^{-3}$ . Additionally, SIMS analysis was carried out  
10 with identical growth conditions to verify the epitaxial doping of the various species (Fig.  
11 1(b)). The fabrication process started with the deposition of thick  $\text{SiO}_2$  layer by plasma-  
12 enhanced chemical vapor deposition (PECVD), which is patterned by Reactive-ion etching  
13 (RIE) plasma. This layer serves as a hard mask for the mesa etching. To reach the n+ layer,  
14 deep mesa etching were performed (about 5.2  $\mu\text{m}$ ) using an optimized  $\text{Cl}_2/\text{Ar}$  based  
15 inductively coupled plasma (ICP) recipe. The developed recipe reduced the sidewall leakage  
16 current and produced a beveled etching for edge termination<sup>28</sup>). The angle appears in Fig. 2,  
17 which was obtained with a focused ion beam by etching a vertical cross section using  
18 platinum metal as etching mask (white region in Fig. 2). The angle of the sidewalls was  
19 estimated to be around  $75^\circ$ . The resulting angle is used to spread the electric field at the edge  
20 of the device over a distance that is larger than the drift region thickness. This technique  
21 results in a gradient of the electrostatic potential and thus helps to manage the electric field  
22 around the anode electrode. The n+ layer was then contacted with the deposition and  
23 patterning of Ti/Al/Ni/Au metal stack by evaporation using a standard lift-off process.  
24 Subsequently, a Pd/Ni/Au stack was deposited using evaporation on top of the p-GaN layer.  
25 Both n-type and p-type contacts were optimized to achieve low ohmic contact resistances  
26 using  $500^\circ\text{C}$  annealing for 10 min. The corresponding contact resistances are around  $5 \times 10^{-6}$   
27  $\Omega \cdot \text{cm}^2$  and  $10^{-4} \Omega \cdot \text{cm}^2$  for n-type and p-type contacts, respectively.  
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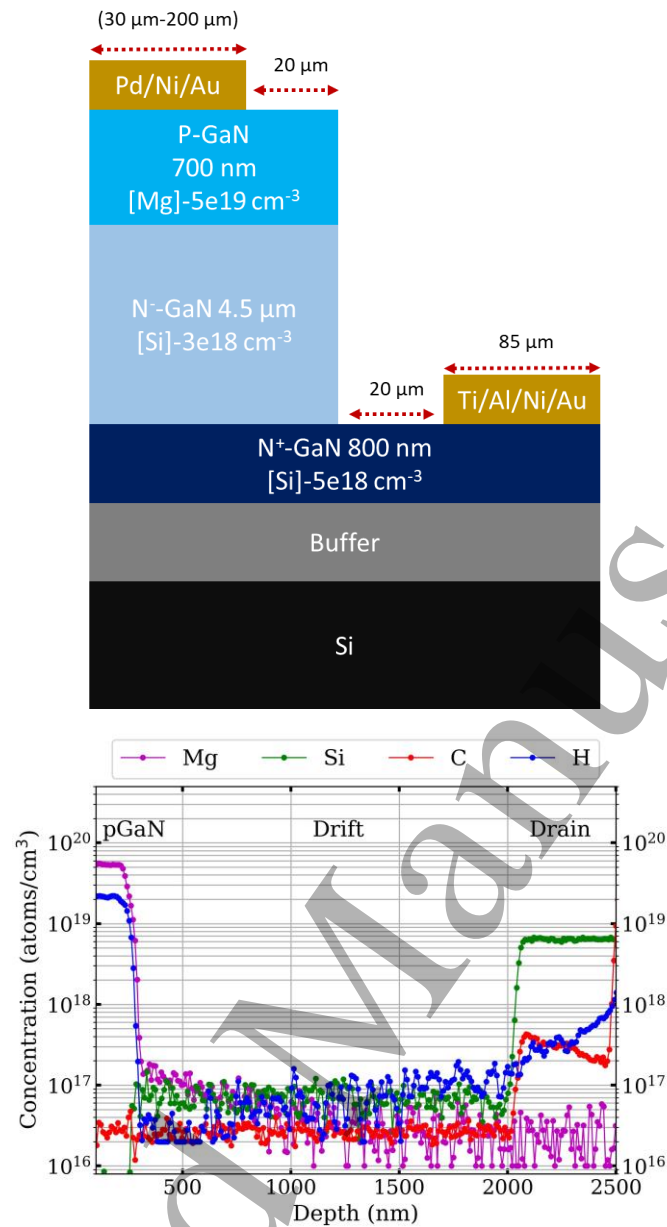


Fig.1. (a) Cross section of pseudo vertical GaN-on-Silicon p-n heterostructure

(b) SIMS analysis of a similar wafer with identical growth conditions

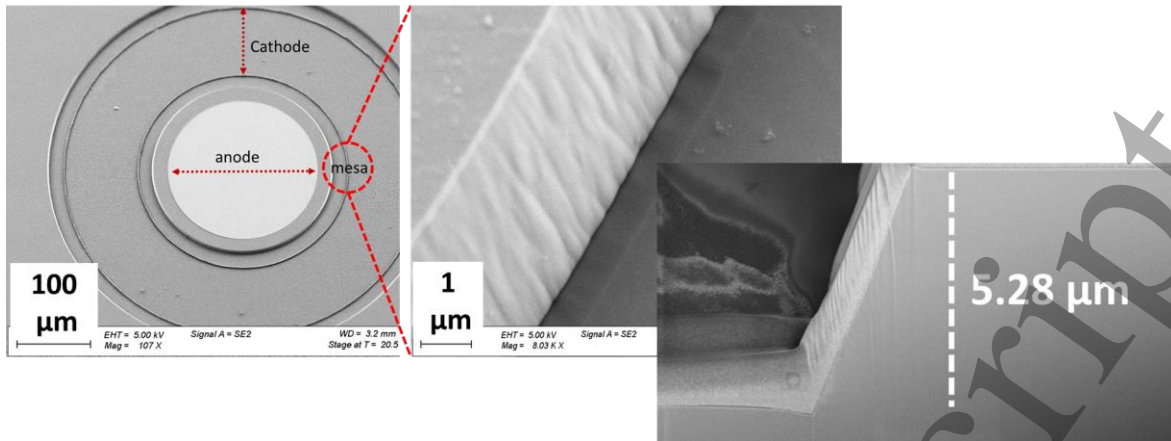


Fig.2. SEM images of the sidewalls from a vertical GaN-on-Si p-n diode. The inset shows a FIB cross section of the beveled sidewalls

Forward characteristics of 30  $\mu\text{m}$  anode diameter vertical diodes, with 70  $\mu\text{m}$  as top mesa diameter, were evaluated using DC measurements from 0 to 20 V as a function of temperature. The device delivered a high current density (J) with low differential on-state-resistance ( $R_{on} < 0.35 \text{ m}\Omega\cdot\text{cm}^2$ ) and a threshold voltage ( $V_{th}$ ) of 4.5 V (Fig. 3.a and b). The  $V_{th}$  value can be reduced by further optimizing the p-type ohmic contacts. The on-state resistance value was extracted ( $\frac{\Delta V}{\Delta J} (V)$ ) in the linear region at 12 V, where the slope is constant and normalized according to the anode area. Two distinct regimes can be observed: 1) between  $V_{th}$  and 12 V, the current spreads towards the epitaxial layers and the slope of  $R_{on}$  decreases before stabilizing. When reaching 12 V, a saturation of the forward current and a degradation of  $R_{on}$  are observed. This is attributed to the pseudo-vertical architecture, where the current crowds at the edge of the n+ layer, limiting the current spreading under high bias due to thermal dissipation issues. From TCAD simulations (see Fig. 4.a) using Silvaco Atlas software, the current crowding contribution can be estimated to be about 40 % of  $R_{on}$  value. Indeed, the current of the pseudo vertical structure flows vertically from the edge of the anode area towards the N+ layer where the charge transport change direction, generating a crowding effect that degrades the specific on-resistance. This results also in a critical length of the current spreading (Fig. 4.a) above which the  $R_{on}$  becomes dependent on the anode diameter. In turn, the size of the contact should be smaller than the critical length. This issue is specific to the pseudo-vertical architecture and does not occur in a fully vertical structure (Fig. 4.b)<sup>(07),23)</sup>. Therefore, this explains the choice in this work of a small anode diameter (30  $\mu\text{m}$ ), which is near the critical length of current spreading and in line with the literature<sup>24–27)</sup>. For a more in-depth analysis of the on-state behavior of the diodes,

I(V) measurements were conducted at various temperatures (Fig. 3.a). Elevated temperatures slightly decrease  $V_{th}$  and enhance the current spreading due to increased thermal diffusion of carriers and narrowing of the bandgap. However, in the second regime (beyond 12 V), the degradation of  $R_{on}$  is more pronounced at high temperature (Fig. 3.b), confirming the thermal dissipation challenges associated to the pseudo-vertical design. Increasing the thickness of the n+ layer can reduce the thermal dissipation issue, but the additional resistance corresponding to the crowding effect will persist.

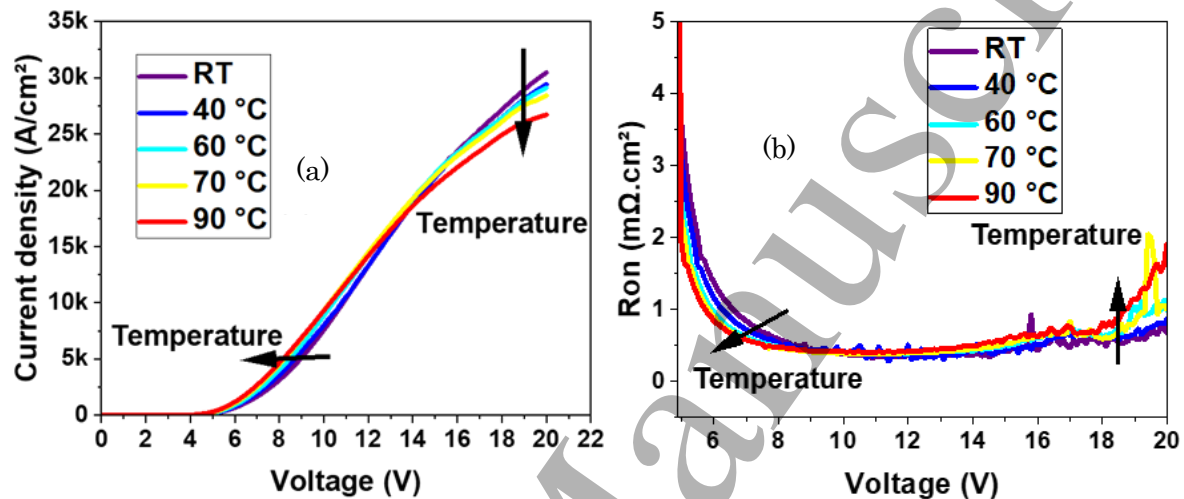


Fig.3. (a) Forward current measurements and (b) Differential on-state resistance measurements at various temperatures.

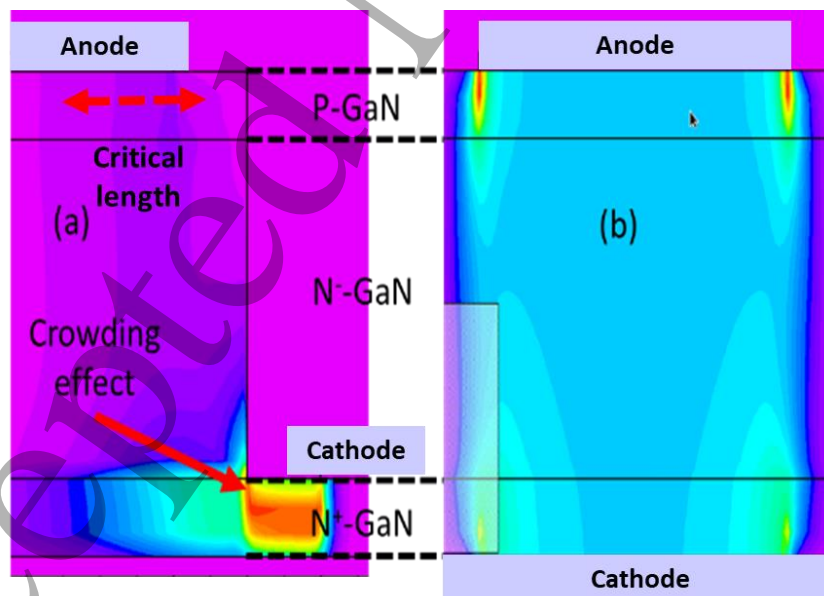


Fig. 4. Distribution of the current density extracted from Silvaco TCAD in on-state conditions for a pseudo-vertical diode (a) and a fully-vertical diode (b).

Typical reverse characteristics of the vertical GaN-on-Si p-n diodes are shown in Fig. 5. The diodes exhibit a high blocking capability (BV) above 800 V, resulting in a high electric field



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3 at the p-n junction of 2.3 MV/cm. This translates to an average electric field across the drift  
4 layer close to 2 MV/cm. Moreover, a uniform breakdown voltage across the sample was  
5 observed with similar values as a function of the anode sizes (up to 200  $\mu\text{m}$  as diameter).  
6 Further improvement of the edge termination process should allow withstanding even higher  
7 critical field. Low leakage current density is observed to be below  $10^{-1}$  A/cm<sup>2</sup> all the way to  
8 the device breakdown. This is a strong indicator of the good material quality as well as the  
9 reduction of sidewall parasitic leakage current achieved through the optimized mesa etching  
10 step. Additionally, it provides solid evidence of low electrically active dislocations within  
11 the structure (although this has not yet been assessed). Fig. 5 shows the temperature  
12 dependence from room temperature up to 100°C of leakage current for reverse biased p-n  
13 diodes. It can be pointed out that the diode survived many voltage sweeps up to 800 V  
14 suggesting avalanche capability. This assumption is confirmed with the temperature  
15 dependence of the reverse J–V characteristics. Under high reverse bias, charge carriers flow  
16 through a specific path with high energy, enabling the accumulation of additional charge  
17 carriers. This corresponds to the so-called impact ionization, which enables for the avalanche  
18 capability<sup>29),30)</sup>. As the temperature increases, phonon scattering delay the onset of impact  
19 ionization. To achieve the same kinetic energy level at higher temperature, a higher voltage  
20 is thus required. Therefore, the increased breakdown voltage with increasing temperature is  
21 a strong indication of the avalanche capability in the devices. A clear avalanche breakdown  
22 signature is observed (Fig. 5.b), as the blocking voltage increases with temperature due to  
23 higher phonon scattering, which delays the onset of impact ionization. The demonstration of  
24 avalanche capability in 800 V-class pn diodes represents a key feature that highlights the  
25 potential vertical GaN-on-silicon heterostructures for power electronics. Fig. 6 illustrates the  
26 benchmark of  $R_{\text{ON,sp}}$  versus BV for vertical GaN-on-Si diodes. The corresponding Baliga  
27 FOM ( $\text{BV}^2/R_{\text{ON}}$ ) around 2 GW/cm<sup>2</sup> is therefore favorably comparable to the state-of-the art.  
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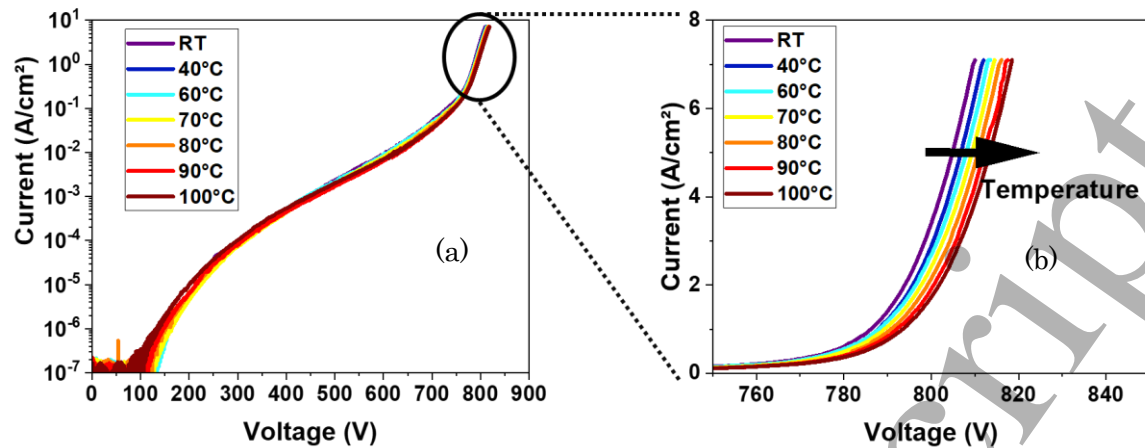


Fig. 5. (a) Temperature dependence of pseudo vertical GaN-on-silicon p-n diode reverse characteristics (b) Zoom of the breakdown region

To conclude, we investigated the potential of vertical GaN-on-Si p-n diodes. With a drift thickness of 4.5  $\mu\text{m}$ , the pseudo-vertical GaN-on-Si diodes exhibited high current spreading with low on-state resistance. Furthermore, we demonstrated a high blocking voltage at 800 V with avalanche capability, resulting in a state-of-the-art BFOM of approximately 2  $\text{GW}/\text{cm}^2$ . The demonstrated avalanche breakdown capability through temperature measurements is a strong indicator of the material and processing quality. This is attributed to an optimized deep mesa etching yielding low leakage current through the sidewalls, and low electrically active dislocations. These results pave the way for medium voltage vertical GaN-on-Si based power devices. It can be pointed out that the limitations related to the pseudo-vertical architecture in terms of current crowding effect can be overcome with the use of a fully vertical structure that can be realized by means of local substrate removal<sup>5)</sup>.

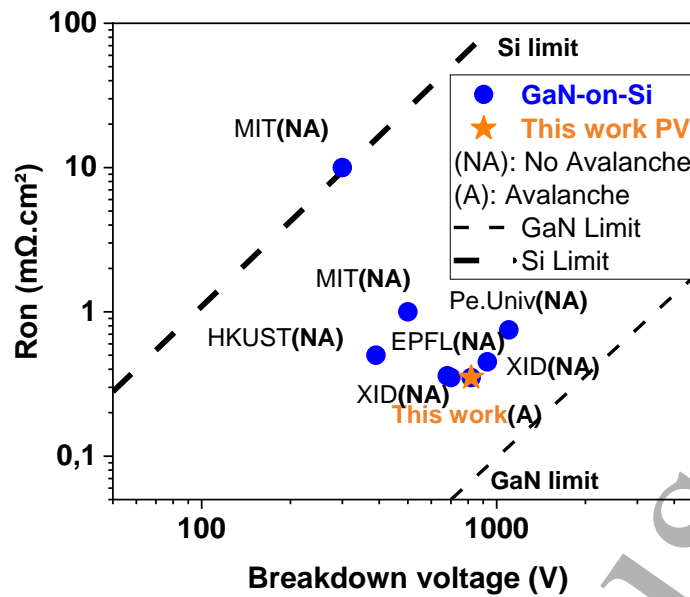


Fig.6. Baliga benchmark of GaN-on-Si silicon p-n diodes indicating avalanche capability<sup>21–27</sup>.

### Acknowledgments

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research & innovation programme and Germany, France, Belgium, Austria, Sweden, Spain, Italy. This work was also supported by the French RENATECH Network.

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## Figure Captions

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