Static characterization on-state of an industrial Si Power MOSFET at cryogenic temperature

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***Abstract*—To reduce fuel consumption and CO_2 emissions, an effort has been made in aircraft industry to investigate a superconducting application requiring an on-board cryogenic system. In this investigation, the question of cryogenic power electronics arose in an effort to reduce losses. Switches are the core of power electronics converters, which means that reducing their losses is a key point for the whole converter. But cryogenic temperatures may alter their behavior due to material contractions and changes in charge carrier behavior. It is therefore important to determine the optimum temperature for the switches, or at least the range within which there is a compromise between reducing losses and ensuring that the switches behave correctly. The Si-MOSFET was initially chosen to better understand the behavior of a single material at cryogenic temperature. The main losses of the MOSFET come from the Drain–Source resistance R_{DSON}. In addition, to ensure the switch operates correctly, the evolution of the voltage threshold V_{TH} as a function of temperature must be determined. This paper presents new results on the study of R_{DSON} Drain-Source resistance at cryogenic temperatures. Results and discussions are also conducted on the V_{TH} voltage threshold and $I_D(V_{DS})$ curves of an industrial Si power MOSFET from 300 K down to 10 K.**

***Index Terms*— Cryogenic characterization, MOSFET, power electronics, power applications, Silicon.**

I. Introduction

To reduce fuel consumption and CO_2 emissions; the aviation industry is investigating the potential of superconducting applications such as motors or generators and cables. As these applications require a cryogenic system on board to operate, the question of a complete cryogenic electric chain, namely: turbine - generator - power electronics - cable - power electronics - engine - fans, naturally arose in order to reduce losses.

Reducing switch losses is a key issue for power converters and the whole cryogenic electrical chain. However, cryogenic temperatures can modify the behavior of switches due to the contraction of materials and changes in the behavior of charge carriers, so it is important to determine the optimum operating temperature range. If it is not possible to use the component at this temperature, then it will be a question of finding a compromise between reducing losses and correct operation of the switch.

Among the switches generally used in the industry, one can mention MOSFETs and IGBTs. Planar power MOSFET's structure was chosen first for the tests because it has a simplest structure than IGBT's. Choosing a silicon-based MOSFET gives us a better understanding of how things work at cryogenic temperature. The static losses of MOSFET come from its R_{DSON} drain-source resistance. To check whether the switch can still be used, the change in threshold voltage V_{TH} as a function of temperature must also be determined.

In the literature [1]–[8], studies are mainly carried out using cryogenic fluids such as helium and nitrogen, i.e. at almost fixed cryogenic temperatures. This means that the complete characterization of the components, and in particular the exact optimum operating temperature, cannot be observed. So-called signal MOSFETs have also been studied at cryogenic temperatures, but they cannot be compared with our work because their structure and doping are very different from those of power components with currents in excess of a hundred amperes.

First, this article describes the component used, citing the main quantities of interest. The cryogenic system is then presented in its entirety, together with the associated

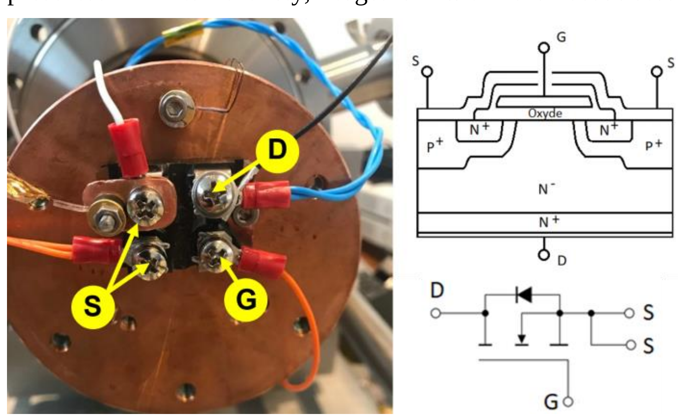

Fig. 1. Presentation of the MOSFET component installed on the cold plate of the cryogenic system and its terminals: Drain (D), Source (S) and Gate (G) (left), the structure of the component (top right) and the electrical diagram of the component (bottom right).

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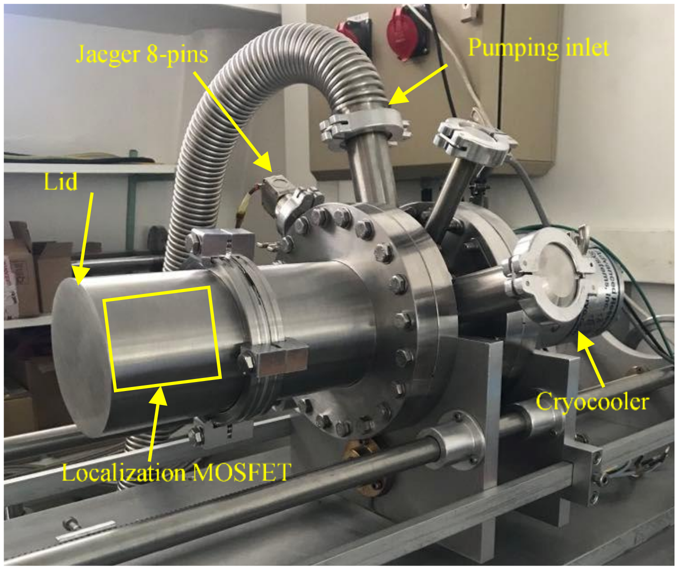

Fig. 2. Presentation of the cryogenic system.

instrumentation. Finally, the experimental results from the characterization at cryogenic temperature are detailed.

II. MOSFET STE180NE10 PRESENTATION

The choice of a MOSFET as a switch is arbitrary. However, the component is chosen to be representative of power components. STMicroelectronics' STE180NE10 MOSFET is a planar power MOSFET, and therefore with an internal power structure, not a signal structure (see Fig. 1): the structure has a N– layer to increase the breakdown voltage and tens of thousands of MOSFET structure are in parallel to do a component. It has a rated current of 180 A, a nominal voltage of 100 V and a length of 38 mm. The MOSFET STE180NE10 is therefore size and power fully compatible with our characterization system.

Table I shows some static characteristics at room temperature of the component given by the manufacturer in its technical document [9], namely: R_{DSON}, V_{TH}, V_{GS} and T_J. The manufacturer guarantees an operating temperature of the junction up to –55 °C, i.e., 218 K but not below.

Having presented the interesting static characteristics of the MOSFET, the system for characterizing it at cryogenic temperature will now be presented.

TABLE I
STATIC CHARACTERISTICS OF THE MOSFET STE180NE10 GIVEN BY THE MANUFACTURER IN [9]

Symbol	Parameters	Test conditions	Value	Unit
R_{DSON}	Static drain-source on resistance	V_{GS} = 10 V, I_D = 40 A	4.5	mΩ
V_{TH}	Gate threshold voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	2 to 4	V
V_{GS}	Gate-source voltage	-	± 20	V
T_J	Operating junction temperature	-	–55 to 150	°C

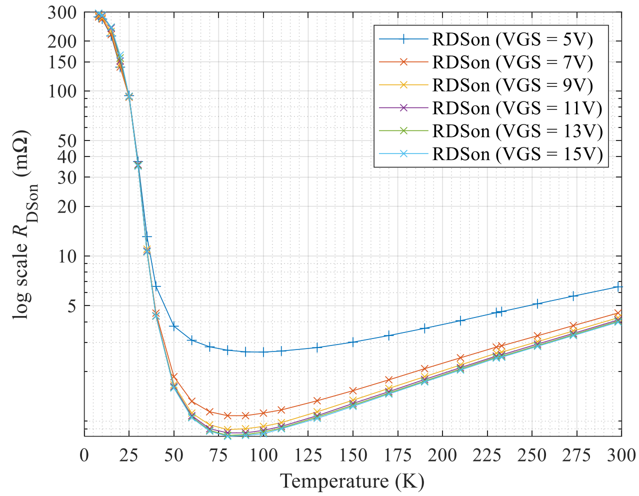

Fig. 3. R_{DSON} evolution with temperature for I_D = 1 A and different V_{GS}.

III. CHARACTERIZATION SYSTEM

A. Cryogenic system

The cryogenic system shown in Fig. 2 is composed of an ARS DE-202 cryocooler and a vacuum chamber. This system, combined with a Lakeshore temperature controller, can regulate and maintain the component temperature within a range of 10 K to 300 K.

B. Measurement system and methods

The measurement system can measure R_{DSON}, V_{TH} and $I_D(V_{DS})$ curves. To measure R_{DSON}, a conventional 4-wire measurement technique is used: a current source injects a current I_D of 1 A with an accuracy of a milliamp, and a voltmeter reads the value of the voltage V_{DS} with an accuracy of a microvolt. To avoid too much heating by Joule's effect of the component, the current is maintained less than 2 seconds. In addition, a dSpace device makes it possible to control the voltage V_{GS} with an accuracy of the order of millivolts.

To measure V_{TH}, the voltage V_{DS} is imposed at 10 V to the nearest millivolt by a voltage source. By varying the voltage V_{GS}, $V_{TH} = V_{GS}$ is obtained when the current I_D is 1 mA.

The $I_D(V_{DS})$ curves are acquired thanks to a Tektronix oscilloscope module for TDS series and a current probe linked to an oscilloscope. A pulsed current with a maximum amplitude of 180 A is applied on the drain, and the voltage is measured between the drain and the source. The on-state duration is 0.85 ms.

The results are finally obtained by averaging 16 pulses. Each pulse is separated by 10 seconds to allow the component to cool down. These protocols were carried out for different gate voltage values and for temperatures between 300 K and 10 K.

IV. MEASUREMENT RESULTS AND DISCUSSIONS

Three quantities will be determined: R_{DSON} to find the temperature where static losses are minimal, V_{TH} to ensure that the component is not saturated and $I_D(V_{DS})$ curves to ensure that the component is in the correct operating range.

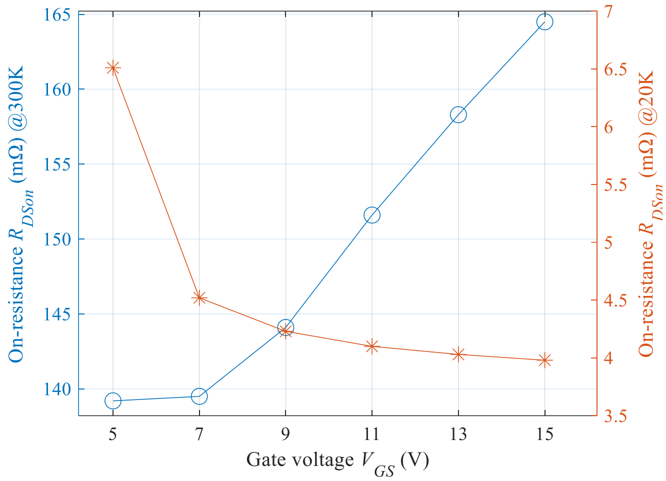

Fig. 4. R_{DSON} curves as a function of V_{GS} for 300 K and 20 K.

A. R_{DSON} resistance measurement

The R_{DSON} measurements shown in Fig. 3 is made for I_{DS} = 1 A and for different values of V_{GS}. They then reveal that the ideal temperature for Si-MOSFET is around 80 K, close to the temperature of liquid nitrogen, used in most high-temperature superconducting applications. At 80 K, the reduction in resistance and static losses is 79% compared with the value at 300 K. These measurements also show that the resistance does not tend towards infinity at very low temperature, as some theories predict [4], but towards a constant.

These measurements also show that there is an inversion from 25 K of the order of the curves in relationship to the gate voltage. Indeed, as illustrated in Fig. 4, at 300 K the higher is the gate voltage, the higher is the resistance, but at 20 K, the higher is the gate voltage the higher is the resistance.

Fig. 5 shows the structure of a power MOSFET and the on-state resistances schematic that can be expressed as:

$$R_{DSON} = R_{N+} + R_{CH} + R_a + R_{JFET} + R_{N-/Drift} + R_{Sub} \quad (1)$$

where R_{N+} is the source region's diffusion resistance, R_{CH} the channel resistance, R_a the access resistance where the current change direction, R_{JFET} the resistance that represents the parasitic JFET transistor, $R_{N-/Drift}$ the resistance of the Drift area and R_{sub} the resistance of the substrate. The wire bonds resistances are not included here. However, as these are metallic junctions, a Seebeck effect can occur and influence the measurements, but it is considered negligible.

The reversal of the curves shown in Fig. 4 and the asymptotic value of the R_{DSON} resistance at low temperatures can be explained by two reasons.

The first reason that can explain this phenomenon is the saturation of the channel. Indeed, the higher the gate voltage, the more the depletion zone increases, decreasing the thickness of the channel and consequently the R_{CH} resistance. The channel thickness is minimum when V_{GS} is maximum. Thus, for low values of V_{GS} the thickness of the channel is greater and allows electrons to pass more easily.

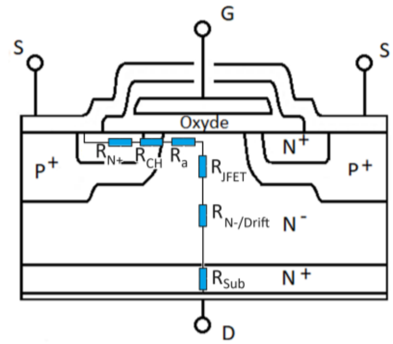

Fig. 5. On-state resistances schematic of a MOSFET and its structure.

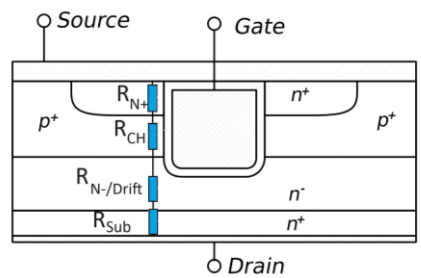

Fig. 6. On-state resistances schematic of a UMOSFET/Trench-MOSFET and its structure.

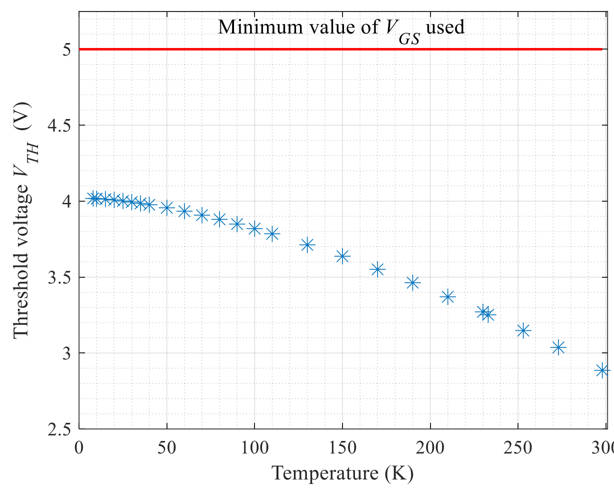

Fig. 7. Evolution of threshold voltage V_{TH} with the temperature defined for I_D = 1 mA.

The second reason would be an influence of the R_{JFET} resistance of the JFET transistor in combination with the access resistance R_a. The JFET tends to reduce the width of the current flow, and that effect can increase with temperature decreases. In addition, at cryogenic temperatures, the carriers start to freeze which could make difficult for them to change direction and thus, could increase the access resistance, R_a. If it's the case then a high gate voltage may saturate the area and increase furthermore the resistance for high value of V_{GS} but not for lower value, explaining the curves. Measuring the R_{DSON} of a power UMOSFET also called power Trench-MOSFET can invalidate this idea. Indeed, the power Trench-MOSFET don't have the R_{JFET} and R_a resistances as shown in Fig 6. So, if the reversal of the curves is still present, then those resistances are

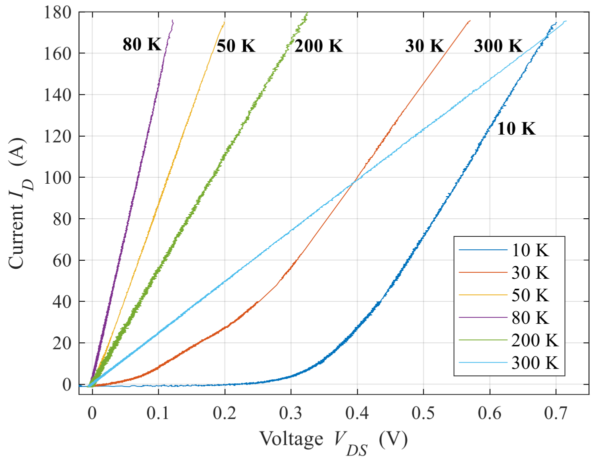

Fig. 8. Evolution of $I_D(V_{DS})$ with temperature @ V_{GS} = 15 V.

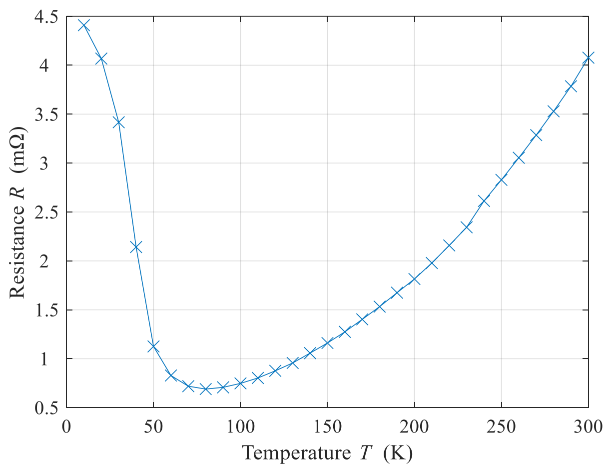

Fig. 9. Resistance evolution with temperature for V_{GS} = 15 V, estimated from the slope of the $I_{DS}(V_{DS})$ curves between 120 A and 170 A, i.e. in the Ohmic region.

not responsible for it. As the structure of power MOSFET is extremely complex, the ideas presented above remain very difficult to affirm.

Having the R_{DSON} evolution with temperature determined, and some explanation of the reversal of the curves given, it seems necessary to explain why the resistance does not tend towards infinity at low temperature. To be sure that the component is not saturated the measurement of the threshold voltage V_{TH} is needed.

B. V_{TH} threshold voltage measurement

The V_{TH} measurements are plotted in Fig. 7 revealing an increase in threshold voltage as the temperature decreases. However, this is not significant to saturate the component nor in preventing the control of a power MOSFET in an inverter, as the control is often powered by 15 V. In addition, over the entire temperature range of the measurements, the lowest grid voltage of 5 V was always higher than the threshold voltage.

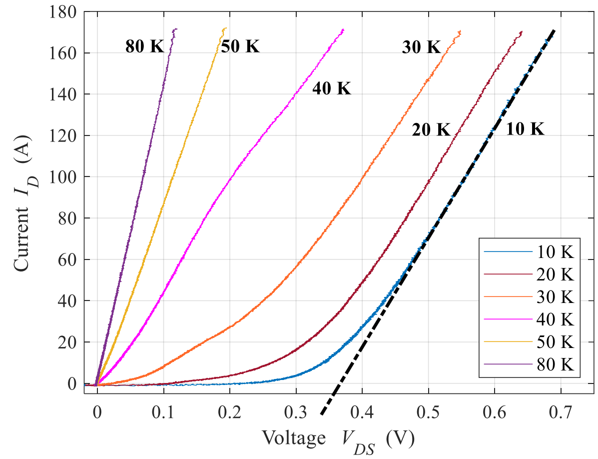

Fig. 10. Evolution of the $I_D(V_{DS})$ curves into diode shape curves @ V_{GS}= 15 V, starting at 40 K and below.

If the threshold voltage is not responsible for the resistance tending towards a constant, then the $I_D(V_{DS})$ curves must be plotted to ensure that the MOSFET is still working in the proper ohmic region.

C. $I_D(V_{DS})$ and ohmic region measurement

If the MOSFET works in the saturated region that would explain why the resistance tends toward a constant. The $I_D(V_{DS})$ curves were then measured from at a temperature ranging from 10 K to 300 K with a step of 10 K. For ease of reading and analysis, only a few temperatures are shown in Figure 8. What is interesting to observe is that the slopes of the curves are following the R_{DSON} evolution with temperature: between 300 K and 80 K, the slope of the $I_D(V_{DS})$ curves is increasing, e.g. 300 K cyan, 200 K green, and 80 K purple, while below 80 K the slopes are decreasing, e.g. 50 K yellow, 30 K orange, and 10 K blue. Although the R_{DSON} resistance shown in Fig. 3 has been determined at a low current of 1 A, which does not always reflect an operation in the Ohmic region, a similar behavior to Fig. 3 have been observed on the dynamic resistance determined by using the linear part of the $I_D(V_{DS})$ curves between 120 A and 170 A and reported in Fig. 9. Below 80 K, the dynamic resistance also increases as the temperature decreases, with a value at very low temperatures, i.e. below 10 K, which seems to tend towards a constant rather than infinity.

Because the MOSFET should normally operate in the ohmic region, the $I_D(V_{DS})$ curves are meant to be linear. But what can be seen are diode-shaped curves from 40 K and below, as shown in Fig. 10. By taking the slope of the 10 K curve to determine what would be the threshold voltage of this diode shape curved, the obtained threshold voltage is between 0.3 V and 0.4 V which is typically a diode Schottky's threshold voltage. The fact that the MOSFET acts as a gate piloted diode explains why the resistance does not tend towards infinity.

D. Explanation of the Schottky diode effect

The power MOSFET structure in Fig. 5 shows an N+ substrate layer just above the drain. One utility of this layer is to prevent a diode Schottky's effect. Indeed, a Schottky diode is made of a junction between a metal and a low doping semi-conductor as the N– layer, so the presence of the substrate, the N+ layer, is preventing this effect because the N+ is a high doping layer. Assuming that doping of N+ layer is virtually decreasing because of the freezing of the carrier; the substrate is then considered as a low doping semi-conductor in junction with a metal which creates a Schottky diode.

V. Conclusions

The work reported in this article clearly demonstrates the benefits of using cryogenics in power electronics, with a sharp reduction in R_{DSON} resistance and associated losses of the order of 80% at 80 K.

Evolution of the R_{DSON} with temperature and gate voltage have been observed in detail. The $I_D(V_{DS})$ curves were used to explain why the resistance does not tend towards infinity by the apparent diode effect from 40 K. In addition, a hypothesis linked to the MOSFET structure was proposed to explain the observed Schottky diode effect.

In the future, in order to assess the dynamic losses, a flyback converter will be built as a power application of the Si MOSFET at cryogenic temperatures. A next step will be to carry out cryogenic characterization on SiC MOSFETs to validate the influence of internal resistances and N+ zone doping. Tests on MOSFETs with higher voltage withstand will also be carried out to see the influence of the N– zone. IGBT, Si Diode and Schottky (Si and SiC) structures will be also studied at cryogenic temperatures, with the aim of sizing and building a converter with these structures.

References

[1] C. Jia, "Experimental investigation of semiconductor losses in cryogenic DC-DC converters," d_ph, University of Birmingham, 2008. Accessed: Dec. 09, 2022. [Online]. Available: https://etheses.bham.ac.uk/id/eprint/161/

[2] K. K. Leong, A. T. Bryant, and P. A. Mawby, "Power MOSFET operation at cryogenic temperatures: Comparison between HEXFET®, MDMeshTM and CoolMOSTM," in *2010 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Jun. 2010, pp. 209–212.

[3] K. K. Leong, B. T. Donnellan, A. T. Bryant, and P. A. Mawby, "An investigation into the utilisation of power MOSFETs at cryogenic temperatures to achieve ultra-low power losses," in *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA: IEEE, Sep. 2010, pp. 2214–2221. doi: 10.1109/ECCE.2010.5617827.

[4] H. Gui *et al.*, "Review of Power Electronics Components at Cryogenic Temperatures," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5144–5156, May 2020, doi: 10.1109/TPEL.2019.2944781.

[5] A. Beckers, F. Jazaeri, A. Grill, S. Narasimhamoorthy, B. Parvais, and C. Enz, "Physical Model of Low-Temperature to Cryogenic Threshold Voltage in MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 780–788, 2020, doi: 10.1109/JEDS.2020.2989629.

[6] H. Mhiesan, M. M. Hossain, A. U. Rashid, Y. Wei, and A. Mantooth, "Survey of Cryogenic Power Electronics for Hybrid Electric Aircraft Applications," in *2020 IEEE Aerospace Conference*, Big Sky, MT, USA: IEEE, Mar. 2020, pp. 1–7. doi: 10.1109/AERO47225.2020.9172807.

[7] K. Rajashekara and B. Akin, "A review of cryogenic power electronics - status and applications," in *2013 International Electric Machines & Drives Conference*, Chicago, IL, USA: IEEE, May 2013, pp. 899–904. doi: 10.1109/IEMDC.2013.6556204.

[8] R. Jurčo, A. Vaskuri, B. Curé, A. Dudarev, and M. Mentink, "MOSFET-based HTS flux pump," *Supercond. Sci. Technol.*, vol. 36, no. 11, p. 115025, Nov. 2023, doi: 10.1088/1361-6668/acfbfc.

[9] "MOSFET STE180NE10.pdf." Accessed: Dec. 15, 2022. [Online]. Available: https://docs.rs-online.com/1b3e/0900766b80478588.pdf