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Stabilizers for REBCO Conductors for High Performance SFCL

P. Tixador, J. Vialle, A. Zampa and A. Badel

Abstract—Resistive REBCO Fault Current Limiter (FCL) is a promising solution to the fault current issue in electric grids, which is not fully satisfactorily solved. But the cost of the Superconducting (SC) REBCO conductor should be lowered to facilitate the deployment of this innovative device. What we refer to as REBCO conductor is usually a bare REBCO tape bonded to a stabilizer. The design of the stabilizer is fundamental to optimize the conductor and lower the SFCL cost. The goal is to limit the temperature rise for any fault conditions, notably for any amplitude of the prospective fault current. The specificities of SC tapes, including critical current inhomogeneities along the length, must be considered in the design. Here we study various stabilizer configurations. First the case of “dielectric stabilizer”, electrically insulating is presented. The theoretical performances are interesting in terms of electric field under limitation, but the low thermal diffusivity remains an issue, as well as the implementation. Some experimental investigations are shown. The results are compared to classical metallic stabilizer designs, which are simpler to implement. To enhance the electric field under limitation, a variant of metallic stabilizer is then introduced, using a corrugated structure. A design showing an electric field under limitation of 200 V/m (clearing time of 50 ms) is presented. Further optimizations and higher electric fields seem achievable even if practical implementation remains very challenging.

Index Terms—Superconducting Fault Current Limiter, optimization, limitation, hot spot, stabilizer

I. INTRODUCTION

Superconducting Fault Current Limiter (SFCL) is a satisfying and unique response to today’s demand for higher security and quality in power grids. This is why SFCL, along with SC cables, shows the highest TRL (Technology Readiness Level) among SC applications [1]. Several SFCLs have already been put into operation in grids. A prominent recent example is the SuperOx 220 kV/460 MVA 3 phase device installed in Moscow, Russia, since 2019 [2]. So even under very high voltages, solutions close to commercialization are available. However, the length of conductor required remains an obstacle in terms of costs. The SuperOx 220 kV SFCL uses 8 km per phase. The electric field under limitation is about 16 V_{RMS}/m (clearing time: 400 ms). Brought back to a clearing time of 50 ms considered in this paper the electric field reaches 45 V_{RMS}/m. This electric field has to increase

significantly to lower the superconducting conductor length and make the cost of the SFCL acceptable. That was the main goal of the EC project FASTGRID [3] and this article aims to go further.

We will only study here conductors based on REBCO tape as they show the best performances for SFCL among commercially available HTS. A conductor refers to a bare REBCO tape bonded to a stabilizer. We will consider resistive FCL. In the FASTGRID project, it was shown that conductors sustaining electric fields up to 130 V/m during 50 ms are experimentally possible even when operating at 65 K, a significant enhancement compared to classical values (50 V_{RMS}/m during 50 ms at 77 K in the EccoFlow project [4] for example). We want to go further with an objective of 300 V_{RMS}/m. The conductor developed in FASTGRID derives from previous works on conductor optimization for SFCL [5, 6]. Within FASTGRID a solution using REBCO tape based on a sapphire tape substrate is also investigated. It sustains electric fields overstepping 1000 V_{RMS}/m [7]. A lot of research and development are still required to enhance the I_c, to industrialize this breaking solution. Its cost remains an open question. So in this article we only consider conventional REBCO tapes with a metallic substrate.

The SC conductor design must fulfill two contradictory requirements which are the safe operations for both low and high prospective currents experienced in power grids. Due to the variety of possible faults, fault currents in power grid may vary from just above the rated current to the highest prospective RMS current (I_{Pros}^{Max}), which is given by the short circuit power of the source (S_{SC}):

$$I_{Pros}^{Max} = \frac{S_{SC}}{3 V_r} \quad (1)$$

This equation is valid for a three-phase grid where V_r is the operating line-to-neutral RMS voltage. Of course, this value becomes fully theoretical when using a SFCL, which will limit the fault current at a much lower value.

For both low and high prospective current cases, the conductor will dissipate energy, either along its full length or along a short length, before a switchgear isolates it from the grid after a

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predefined clearing time (Δt). The design approach is basically a thermal study: the temperature of the SC conductor must be kept below a threshold value set by either the SC layer degradation or the melting of solder in the conductor.

For high prospective currents, the power grid behaves like a voltage source (V) and the dissipative power is given by V^2/R_l where R_l is the resistance of the SFCL. This case is called limitation regime, in which a large conductor resistance is favorable to lower the dissipation.

But the prospective fault current may take any value up to I_{Pros}^{Max} (equation (1)) whereas the critical current of a REBCO tape intrinsically varies along its length. Reference [8] shows that the I_c distribution follows a Weibull probability distribution characterized by a minimum critical current I_{c^*} which decreases with the conductor length. Fig. 1 plots the measured I_c every 1.1 mm along 100 m for a THEVA tape at 77 K. The minimum, maximum and mean I_c are respectively 642.7 A, 785.6 A and 743.5 A. A SFCL does not require very long unit lengths. It consists of modules put in series or/and in parallel to meet the specifications. The voltage for one module will be in the range of tens of kV, corresponding to a length of the order of a hundred meter. Fig. 1 then represents right the typical length of a SFCL module.

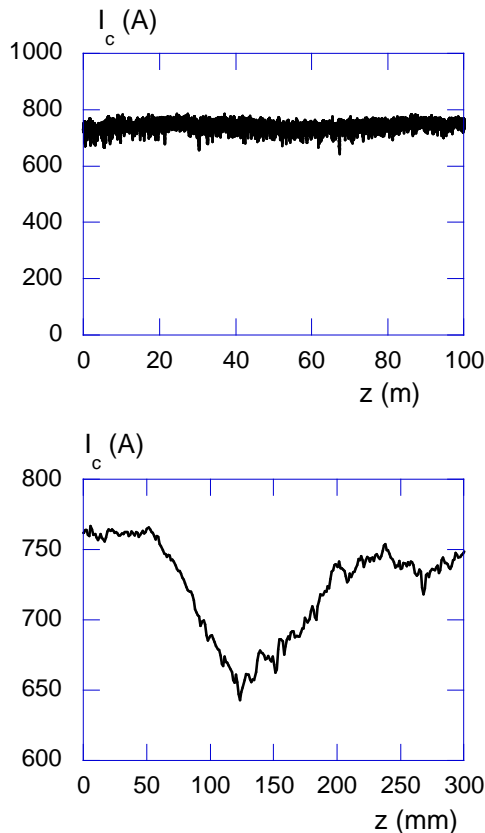


Fig. 1. I_c (77 K sf) along 100 m of a REBCO tape (THEVA data), zoom on the right (z in mm) for the lowest I_c zone.

Fig. 1 shows that the minimum I_c is very localized in the length. In the case of a prospective current in the range of this minimum I_c only this short spot would initially dissipate.

The expansion of this dissipative spot is very limited since the Normal Zone Propagation Velocity (NZPV) is low for REBCO tape, up to about 0.1 m/s for a bare tape at 77 K at the critical current [9], except if using special architecture like Current Flow Diverter (CFD) [10]. The normal zone still remains very short at the time of clearing (50 ms: 5 mm): it is a “spot” which rapidly may become hot, hence the name of “hot spot” given to this regime. The hot spot shows a negligible resistance (proportional to its length) compared to the fault impedance. The source then behaves like a current source (I). The dissipation power is therefore $R_2 I^2$ where R_2 is the hot spot resistance. Contrary to the limitation regime and much like the case of a magnet, a small resistance per unit length is favorable. We can see that a compromise has to be found to optimize the conductor to cope with both low and high prospective currents. The stabilizer plays a key part in the conductor optimization and we present some solutions in this work.

Fig. 2 summarizes the behaviour of a REBCO conductor with typical inhomogeneity for the full range of prospective RMS fault current related to its critical current. It shows the maximum temperature reached at the clearing time for any fault. The two strongest thermal constraints are for the hot spot regime ($I_{pros} \approx I_c$) and the limitation one (here $I_{pros} = 15 I_c$). This curve is a calculated plot for the FASTGRID THEVA conductor, in agreement with experimental curves [11]. The FASTGRID conductor uses a 12 mm wide THEVA tape [12] with 1.6 μm of silver above the 3 μm HTS layer and 1 μm silver on the edges and the bottom. The tape is soldered to a 500 μm thick Hastelloy[®] tape (stabilizer) with a Ni coating (1 μm) to make the soldering possible. The solder is tin and 10 μm thick. This conductor has been designed to get the same peak temperature (400 K) for the hot spot regime and the limitation one.

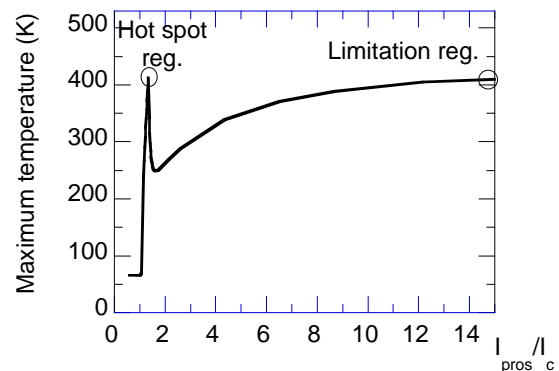


Fig. 2. Typical maximum temperature of the SC conductor at the clearing time (50 ms) versus the ratio of the prospective RMS current to the critical one.

The quantitative values of the maximum temperature depend on the conductor. The peak temperature depends on its length for example [13]. But we nearly have always the same behaviour with an increase of the maximum temperature with the prospective current then a decrease and an increase again with

an asymptotic value. References [14, 15] show similar experimental curves for SuperPower tapes and reference [16] gives a comparable simulation plot.

This article presents first some analytical conductor design with a solution to reach 200 V_{RMS}/m. Strong questionable hypothesis will be of course made. Nevertheless, analytical expressions have the great advantage to clearly show the relevant parameters to optimise the conductor. They show in particular that a dielectric and corrugated stabilizers could be attractive. The real designs are then carried out using numerical approach which limits the expected performances. A few experiences about dielectric stabilizer are presented. They confirm the limitations and the rather good agreement between measurements and simulations even if differences exist. Preliminary optimisations of the corrugated stabilizer are presented. They also highlight the difficulties to implement this solution.

II. ANALYTICAL CONDUCTOR DESIGN

A SC conductor is a SC tape bonded to a stabilizer. These two elements are electrically in parallel and thermally connected. That is the case when using a metallic stabilizer soldered to the tape, as for the FASTGRID conductor. It must be noted that the design approach presented below remains valid for studying a tape bonded to a dielectric material, by simply setting the electrical conductivity of the stabilizer to zero. This makes the use of bonded dielectric material simply a particular case of electric stabilizer, hence the name of dielectric “stabilizer” that we will use later on.

A very strong assumption for analytical expressions is the isothermal cross section of the conductor. This is questionable even in case of a metallic stabilizer but mandatory to get analytical expressions to identify the relevant parameters. For the real design numerical simulations will be used to avoid this strong assumption.

A. Limitation regime

The power source is in that case a voltage source. The high prospective current quenches the full length. With the isothermal assumption the thermal equation is then:

$$\frac{v(t)^2}{R_l} dt = (Vol_{tape} c_p^{tape} + Vol_{stab} c_p^{stab}) dT \quad (2)$$

where $v(t)$ is the instantaneous voltage, R_l the resistance of the conductor, Vol_{tape} Vol_{stab} the volumes of the tape and the stabilizer respectively and c_p the specific heat per unit volume (J/m³/K). The regime is supposed adiabatic since the dissipation is huge with heat fluxes much higher than what can be absorbed by the cooling fluid. Temperature sensors show a very good agreement ($\Delta T/T < 5\%$) of the measured temperature with the calculations assuming adiabatic conditions at least for 30 ms [17]. The calculations are also very close to the temperature extracted from the R(T) of the tape or conductor.

The tape and the stabilizer being electrically in parallel the equation becomes:

$$\left(\frac{1}{R_{tape}} + \frac{1}{R_{stab}} \right) v(t)^2 dt = (L_{tape} w_{tape} e_{tape} c_p^{tape} + L_{stab} w_{stab} e_{stab} c_p^{stab}) dT \quad (3)$$

The tape and the stabilizer do not have necessarily the same lengths (L_{tape} and L_{stab}) nor the same widths (w_{tape} and w_{stab}). The thicknesses of the tape and of the stabilizer are respectively e_{tape} and e_{stab} .

$$\left(\frac{v(t)}{L_{tape}} \right)^2 dt = \frac{e_{tape} c_p^{tape}(T) + \frac{L_{stab} w_{stab} e_{stab} c_p^{stab}(T)}{L_{tape} w_{tape}}}{\frac{e_{tape}}{\rho_{tape}(T)} + \frac{e_{stab} w_{stab} L_{tape}}{\rho_{stab}(T) w_{tape} L_{stab}}} dT \quad (4)$$

ρ_{tape} and ρ_{stab} are the equivalent resistivity of the tape and of the stabilizer respectively. One only has to integrate to get the maximum temperature (T_{max}) when the SFCL is electrically isolated after Δt (clearing time). Let us fix the starting temperature not to the initial one (T_0) but to the critical one (T_c) so that the regime under T_c where the resistivity of the tape depends on the current is neglected. This has a very limited impact on the results while simplifying greatly the calculations. The only consequence is that the maximum temperature is slightly overestimated by 10 K as order of magnitude. With this hypothesis the integration of equation (4) gives:

$$E_{lim}^{tape2} \Delta t = \int_{T_c}^{T_{max}} \frac{e_{tape} c_p^{tape}(T) + \frac{L_{stab} w_{stab} e_{stab} c_p^{stab}(T)}{L_{tape} w_{tape}}}{\frac{e_{tape}}{\rho_{tape}(T)} + \frac{e_{stab} w_{stab} L_{tape}}{\rho_{stab}(T) w_{tape} L_{stab}}} dT \quad (5)$$

E_{lim}^{tape} is the RMS value of the tape electrical field.

In case of a thick ($e_{stab} > 5 e_{tape}$) stabilizer design, we can even neglect the tape itself in the thermal balance and the equation of the tape electrical field simplifies to:

$$E_{lim}^{tape} \approx \frac{L_{stab}}{L_{tape}} \sqrt{\frac{\int_{T_c}^{T_{max}} \rho_{stab}(T) c_p^{stab}(T) dT}{\Delta t}} \quad (6)$$

The objective is of course to maximize the tape electric field E_{lim}^{tape} to use the shortest length of the SC tape. Equations (5) and (6) show that we have to:

- Increase the ratio L_{stab}/L_{tape} .
- Foster high electric resistivities for the tape and the stabilizer.
- Use tape and stabilizer with high specific heats.
- Lower the clearing time.

On the other hand, the thicknesses and the widths play little part, but we will see that they are important for the hot-spot regime.

Commercial REBCO tape structures are more or less similar. The tape is made of a substrate, electrical insulated thin buffer layers, the REBCO layer and an Ag metallization layer above. REBCO tape based on a Hastelloy® substrate are preferable due to the Hastelloy® high resistivity. Silver is not ideal for a high

resistance but tests carried out to pollute it to increase its resistivity were unsuccessful within FASTGRID. Likewise, its thickness cannot be lowered too much, as a continuous and regular protection layer is required. A total Ag thickness of about 2 μm is reasonable. Nevertheless, we will see that it would be useful to increase the resistance of the metallization layer by decreasing its thickness and/or its electrical conductivity. The substrate thickness may be adapted: it can vary typically from 30 μm to 100 μm .

The clearing time Δt is fixed by the speed of the switch gear but also by the risk that it fails to open. In that event the opening of a second switch clears the fault. Considering this back-up the clearing time reaches about 50 ms [18]. This value will be considered in the rest of the article knowing that most of the time (normal operation without failure of the first switch gear) the clearing time is about 20 ms, decreasing the maximum temperature a lot. This low clearing time is not common for today switch gears but fully possible and demonstrated

The specific heat per unit volume does not significantly vary between materials above 60 K.

The use of a stabilizer materials with zero electric conductivity, so called dielectric stabilizers is an option and some experiments will be shown in part II A.

Longer and wider stabilizer compared to the tape can be imagined with corrugations for example (Fig. 3). We will see that the corrugated stabilizer will be very different compared to Fig. 3 due to thermal considerations.



Fig. 3. REBCO tape with corrugated stabilizer (same width).

But before we study more in detail these stabilizers, we have to consider the conductor design for the hot spot regime.

B. Hot spot regime

The power source is in that case a current source. The thermal equation is then:

$$R_2 i(t)^2 dt = Volume c_p dT \quad (7)$$

The regime is also supposed to be adiabatic even if this hypothesis is less valid compared to the limitation regime. This effect of the thermal exchanges has to be studied especially in subcooled nitrogen at 65 K since the exchanges may be better compared to 77 K saturated nitrogen [19].

The tape and the stabilizer being in parallel electrically equation (7) becomes:

$$i(t)^2 dt = \left(\frac{1}{R_{tape}} + \frac{1}{R_{stab}} \right) \left(L_{tape} w_{tape} e_{tape} c_p^{tape}(T) + L_{stab} w_{stab} e_{stab} c_p^{stab}(T) \right) dT \quad (8)$$

$$\left(\frac{i(t)}{w_{tape}} \right)^2 dt = \left(\frac{e_{tape}}{\rho_{tape}(T)} + \frac{e_{stab}}{\rho_{stab}(T)} \frac{w_{stab}}{w_{tape}} \frac{L_{tape}}{L_{stab}} \right) \left(e_{tape} c_p^{tape}(T) + \frac{L_{stab}}{L_{tape}} \frac{w_{stab}}{w_{tape}} e_{stab} c_p^{stab}(T) \right) dT \quad (9)$$

The RMS prospective fault current which leads to the hot spot regime is close above the critical current (Fig. 2) so we fix it at I_c in the calculations. As for the limitation regime the integration starts at the critical temperature:

$$I_{c-w}^2 \Delta t = \int_{T_C}^{T_{max}} \left(\frac{e_{tape}}{\rho_{tape}(T)} + \frac{e_{stab}}{\rho_{stab}(T)} \frac{w_{stab}}{w_{tape}} \frac{L_{tape}}{L_{stab}} \right) \left(e_{tape} c_p^{tape}(T) + \frac{L_{stab}}{L_{tape}} \frac{w_{stab}}{w_{tape}} e_{stab} c_p^{stab}(T) \right) dT \quad (10)$$

I_{c-w} is the critical current per unit width of the tape (I_c/w_{tape}). This expression makes possible to design the stabilizer (thickness and width) so that the conductor survives the hot spot regime. Once again for thick stabilizer we may neglect the tape influence to get an ultra-simplified expression:

$$e_{stab} \frac{w_{stab}}{w_{tape}} = I_{c-w} \sqrt{\frac{\Delta t}{\int_{T_C}^{T_{max}} \frac{c_p^{stab}(T)}{\rho_{stab}(T)} dT}} \quad (11)$$

The hot spot regime mainly defines the stabilizer thickness. To reduce it (thinner and more flexible stabilizer) equations (10) and (11) show that we have to:

- Increase the ratio w_{stab}/w_{tape} .
- Foster low resistivities for the tape and the stabilizer.
- Use tapes and stabilizers with high specific heats.
- Lower the clearing time.

The relative lengths play little part contrary to the limitation regime.

Of course, for the hot spot regime high resistivities are logically not favorable but we have however to maximize the resistivities to lower the tape length. That is the objective of this work. The stabilizer has to be adapted to meet the hot spot regime as we will see. It will be thick (< 0.5 mm). Increasing the width of the stabilizer is also interesting to lower the recovery time of the SFCL since it increases the heat transfer surfaces with the cooling fluid and the area over volume ratio.

Unfortunately, this increase of the stabilizer width compared to the tape will be limited by the thermal diffusion in the total width of the stabilizer. In addition, we will see that a wider stabilizer introduces a harmful thermal gradient within the tape.

C. Intermediate conclusion

The main conclusions deduced from the previous expressions to get an “optimized” conductor for the SFCL are:

- A stabilizer longer compared to the tape (corrugation e.g.).
- A stabilizer wider compared to the tape.
- A highly resistive stabilizer, even possibly an electric insulator (dielectric material).

We have nevertheless to emphasize that these conclusions are based on a questionable isothermal section, as thermal simulations will show.

These conclusions will be applied now to two types of stabilizers:

- Dielectric stabilizer.
- Metallic corrugated stabilizer.

III. STABILIZER

A. Dielectric stabilizer

Such a stabilizer opens the way of high electric fields (equation (5) and (10) with infinite resistivity for the stabilizer):

$$E_{lim}^{tape2} \Delta t = \int_{T_c}^{T_{max}} \left(c_p^{tape}(T) + \frac{L_{stab}}{L_{tape}} \frac{w_{stab}}{w_{tape}} \frac{e_{stab}}{e_{tape}} c_p^{stab}(T) \right) \rho_{tape}(T) dT \quad (12)$$

$$\frac{I_{c-w}^2 \Delta t}{e_{tape}^2} =$$

$$\int_{T_c}^{T_{max}} \frac{1}{\rho_{tape}(T)} \left(c_p^{tape}(T) + \frac{L_{stab}}{L_{tape}} \frac{w_{stab}}{w_{tape}} \frac{e_{stab}}{e_{tape}} c_p^{stab}(T) \right) dT \quad (13)$$

Neglecting the temperature dependence of the parameters, the expression of the electric field under limitation becomes very simple:

$$E_{lim}^{tape} = \frac{\rho_{tape}}{e_{tape}} I_{c-w} \quad (14)$$

The electrical conductivity and the thickness of the tape should be as low as possible: tape with only its thin metallization layer and thin Hastelloy® substrate (50 μm, even 30 μm). Using equation (14), the electric field may be very high:

$$\rho_{tape} = 0.2 \mu\Omega m, e_{tape} = 55 \mu m, I_{c-w} = 120 \text{ kA/m (65 K):}$$

$$E_{lim}^{tape} = 440 \text{ V/m}$$

This is extremely attractive but the hypothesis behind this extreme value must be fulfilled, in particular the isothermal section of the tape and above all the stabilizer. Using equation (13) the stabilizer thickness is about 2 mm ($L_{stab}/L_{tape} = 1$; $w_{stab}/w_{tape} = 1$; $\Delta T = 350 \text{ K}$; $\Delta t = 50 \text{ ms}$). This is a lot taking into account the low diffusivity of dielectric materials during the clearing time Δt .

We carried out some tests on SuperOx 4 mm wide tapes encapsulated in bulk epoxy and on SuperPower 2 mm wide tapes with Stycast® coatings on both sides.

1) SuperOx epoxy encapsulated tape

The 4 mm wide tape is encapsulated in a bulk epoxy block 10 mm thick and 10 mm wide. Fig. 4 gives its longitudinal cross section with two external connections and three temperature sensors (Pt100 resistances, S1, S2 and S3). S1, S2 and S3 are respectively 1 mm, 2 mm and 5 mm above the tape (S3 is near the external surface). The SuperOx tape has a Hastelloy® substrate 100 μm thick. In addition to the micronic Ag layer, 3 μm of Cu and 10 μm of solder (Sn₆₂Pb₃₂Ag₂) are deposited on both sides of the tape. Outside the 90 mm central part, a second Cu layer 10 μm thick protects the tape in the parts without encapsulation (200 mm long) (Fig. 4).

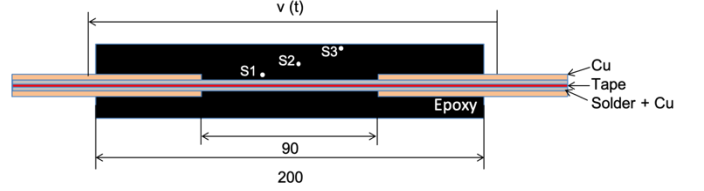


Fig. 4. SuperOx tape encapsulated in epoxy with current leads and thermal sensors (not to scale).

Fig. 5 shows the time evolutions of the current, voltage for a 70 ms short circuit in DC conditions at 77 K. The short-circuit power of the source is insufficient to keep the voltage constant. The critical current is about 150 A (100 μV/m, 77 K sf). The peak current is high due to the low resistance even in the middle (solder and Cu) and the high electric field. Limitation is strong due to the reduction of the voltage and the high sample heating.

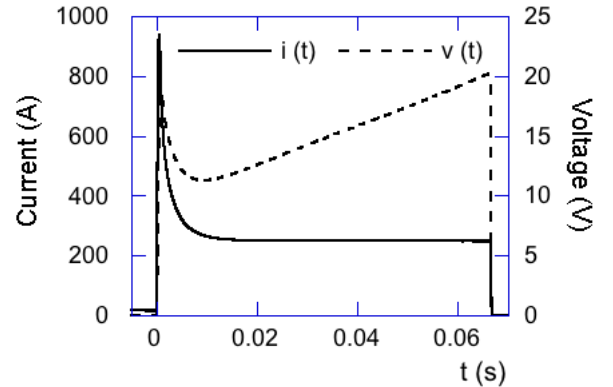


Fig. 5. DC short-circuit test, current and voltage for the SuperOx tape encapsulated in epoxy at 77 K.

Fig. 6 and Fig. 7 show the temperatures of the 3 sensors (S1, S2 and S3, see Fig. 4) for this short circuit for different durations (0-0.2 s for Fig. 6 and 0-10 s for Fig. 7). In addition, for Fig. 6, we also plot the calculated hot spot temperature (T_{max}) of the conductor including the epoxy encapsulation in adiabatic condition [20]:

$$\int_0^t i(x)^2 dx = A \int_{T_c}^{T_{max}} \frac{c_p(T)}{R_l(T)} dT \Rightarrow T_{max}(t) \quad (15)$$

where A is the conductor cross section of the tape (including epoxy) and R_l its resistance per unit length. The integration of the square of the current starts at $t = 0$ and the temperature is supposed to be T_c ($T_{max}(t = 0) = T_c$) to avoid the regime under T_c where the resistance depends of the current. This equation assumes again an isothermal conductor cross section, the real temperature of the tape will be much higher as some simulations will show. However, the encapsulation definitely plays a part and protects the tape. Indeed, the theoretical hot spot temperature calculated considering only the tape without epoxy exceeds several thousands of K. This is clearly not possible since the tape survived several tests: the tape shows a non-linear behaviour. However, no I_c measurement at $100 \mu\text{V/m}$ was carried out to observe possible slight degradations.

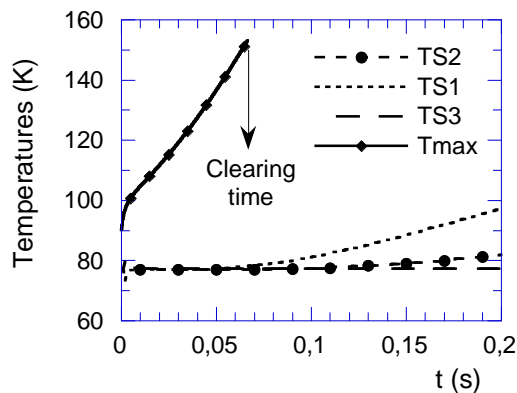


Fig. 6. DC short-circuit test, measured temperatures (TS1, TS2 and TS3) and calculated hot spot temperature (T_{max}) including epoxy at the beginning.

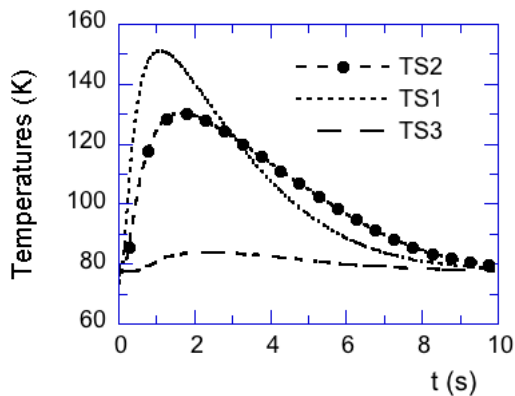


Fig. 7. DC short-circuit test, measured temperatures evolution up to the recovery.

The temperature curves show the low thermal diffusion in the thickness of the epoxy stabilizer: the temperature variation quickly decreases as soon as we move away from the tape. Even close to the tape the temperature only rises after the clearing time. The external temperature (TS3) increases only a little and after a very long delay.

Due to the diffusion in the stabilizer thickness the maximum temperature within the epoxy occurs after the end of the fault and it takes about 10 s to go back to the initial temperature (77 K, Fig. 7).

Fig. 8 and Fig. 9 plot the temperatures of the tape at the locations of the 3 sensors calculated by finite elements for two different durations (0-0.5 s for Fig. 8 and 0-10 s for Fig. 9). The tape temperature increases very rapidly and is strongly limited after the clearing time.

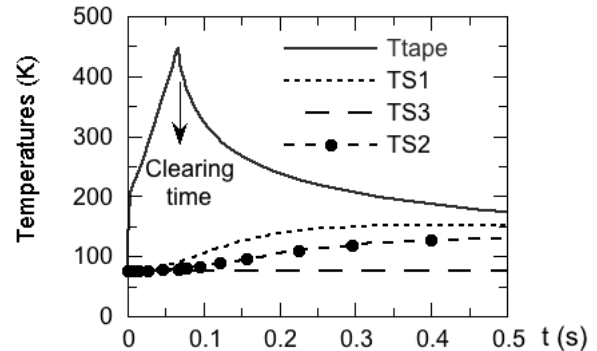


Fig. 8. Simulated temperatures (tape and at the 3 sensors) during the limitation and just after.

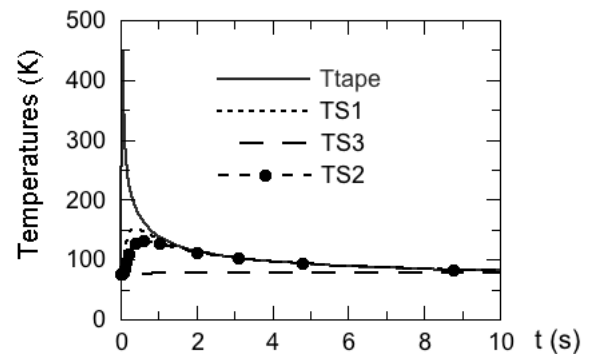


Fig. 9. Simulated temperatures (tape and at the 3 sensors) up to the recovery.

The simulated and measured temperatures are in rather good agreement especially in terms of maximum value (Fig. 10) but there is a time lag of about 1 s between them. This difference may be due to thermal contacts between the layers not considered in the simulation, the thermal conductivity is also not accurately known. In addition, the locations of the sensors are not very precise. We put indeed the sensors after we received the encapsulated tapes.

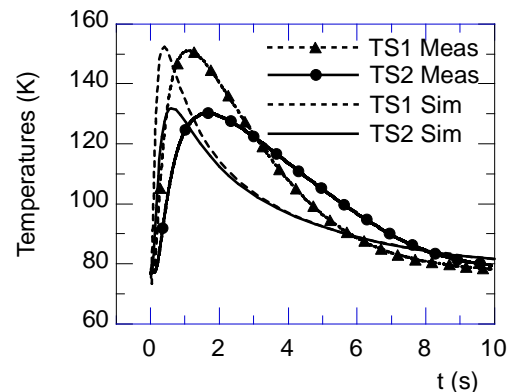


Fig. 10. Simulated and measured temperatures (sensors 1 and 2).

Simulations show that due to the thermal diffusivity of epoxy the thickness of the epoxy stabilizer should be lower than 0.5 mm. This is what we tried in the next step.

2) SuperPower 2 mm wide tapes with Stycast® coatings

We have coated a 2 mm wide SuperPower tape ($I_c = 50$ A ($100 \mu\text{V/m}$, 77 K sf)) with 0.5 mm Stycast® 2850FT with catalyst 24LV on both sides. The tape has an Hastelloy substrate of $50 \mu\text{m}$ thick and its total thickness is about $52 \mu\text{m}$, so $1 \mu\text{m}$ of silver. Fig. 11 shows a limitation curve. The electric field nearly reaches 180 V/m during 33 ms and the tape survived this test but the Stycast® layers were fully delaminated after. The calculated hot spot temperatures reached about 400 K and 1000 K at the clearing time considering the total section or the section of the bare tape respectively. Since the tape still was superconducting after the tests, the Stycast® definitely plays a part. However, the I_c was not measured after the test so that slight tape degradations could occur. By lowering the electric field, the delamination of the stabilizer occurred less quickly. For 170 V/m the delamination occurred during the second limitation test.

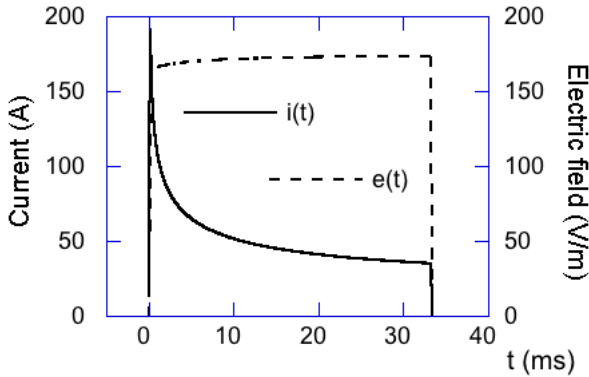


Fig. 11. Current and electric field during a limitation experiment on a SuperPower tape with 0.5 mm epoxy on both sides.

In conclusion the dielectric stabilizer concept shows interesting perspectives. Nevertheless, the poor diffusivity of dielectric material limits the performance. Indeed, contrary to the case of metallic stabilizer where the stabilizer itself dissipates, here the stabilizer acts only as a thermal drain. All the power is still dissipated in the tape and diffuses to the stabilizer by thermal conduction. Temperature differences should be limited to avoid differential contraction mechanical issues. The stabilizer thermal expansion should be adapted to that of the tape for the same reason. The good thermal contact between the tape and the stabilizer is another challenge. References [21] and [22] give some studies about insulated or high c_p stabilizer.

The recovery time may be an issue but it depends on the SFCL use and location. For some locations the recovery time can be short but for other locations, a grid with cables for example the recovery time is unproblematic. In opposition to an overhead line where a fault may be fugitive for a cable, the fault cannot be fugitive with no automatic reclosing.

Due to these difficult implementation issues, we moved from this solution toward metallic corrugated stabilizer.

B. Metallic corrugated stabilizer

Equation (5) clearly shows the advantage to increase the length of the stabilizer compared to that of the tape to enhance the tape electric field. Without increasing the stabilizer length compared to the tape length, the ultimate electric field (metallization layer neglected) using an Hastelloy® stabilizer is:

$$E_{lim}^{ult} \approx \sqrt{\frac{\rho_{Hast}(H_{hast}(T_{max}) - H_{hast}(T_c))}{\Delta t}} \quad (16)$$

where H is the conductor enthalpy per unit volume. For $T_{max} = 415$ K and $\Delta t = 50$ ms the ultimate electric field reaches 160 V/m. The stabilizer is Hastelloy® for two reasons: this superalloy shows a high electrical resistivity ($1.25 \mu\Omega\text{m}$) and matches the expansion of the tape, mainly Hastelloy®.

Fig. 12 gives the increase of the tape electric field with the ratio $L_{stabilizer}/L_{tape}$. The tape is a $55 \mu\text{m}$ thick tape with a Hastelloy® substrate and $2 \mu\text{m}$ Ag layer. The geometrical ratio $e_{stabilizer}/e_{tape}$ is calculated using equation (10) and considering a maximum temperature of 415 K (50 ms). The critical current per unit width is 1200 A/cm-w since we operate at 65 K to lower the quantity of tape. This is the lowest temperature possible with liquid nitrogen, the only cheap and industrially available cryogenic fluid.

Fig. 12 shows that 300 V/m is reached for a stabilizer 3.2 times longer than the tape.

In addition to the increase of the stabilizer length compared to the tape length, the corrugated configuration increases the exchange surfaces with the cooling fluid. This decreases the recovery time after a limitation and increase the NZPV for the tape parts between the ribs. Indeed, the NZPV is larger for a bare tape compared to that of an electrically-stabilized tape [9] since the dissipation per unit length is higher.

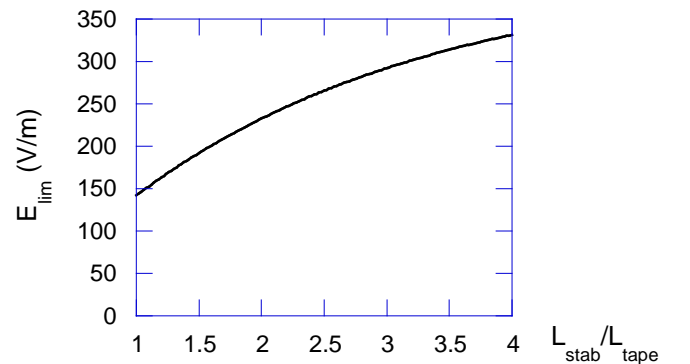


Fig. 12. Electric field versus stabilizer to tape length ratio.

If equation (5) shows the large interest to increase the length and width of the stabilizer compared to the tape, it is based on a strong hypothesis, that the temperature remains uniform in the section. This hypothesis is nearly valid when the stabilizer is fully bonded with the tape despite the low thermal diffusivity of Hastelloy® since the stabilizer itself is heated by Joule effect

during the limitation phase. Nevertheless, the power dissipation per unit volume in the stabilizer remains in general much lower than in the tape: the stabilizer is often heated mainly by conduction. The thermal diffusivity of Hastelloy® is about $3 \cdot 10^{-6} \text{ m}^2/\text{s}$ (it varies with temperature). This means that temperature diffuses over about 200 to 300 μm in the 50 ms of the clearing time (Fig. 13) without internal heating. Since the stabilizer length is higher than the tape, its resistance is also higher and less current flows in the stabilizer still lowering its heating by Joule effect. This is why it would be all the more interesting to increase the resistance of the tape by lowering the metallization thickness and its electrical conductivity to divert more current in the stabilizer to heat it more.

This poor diffusivity of Hastelloy® stabilizer hinders from increasing the corrugation height above typically 700 μm . This low Hastelloy® diffusivity also prevents from increasing too much the stabilizer width compared to the tape one.

To take into account the thermal diffusion within the section, 2D finite element simulations have been carried out using COMSOL® software. They are based on following hypothesis:

- Perfect thermal contact between the different areas.
- Adiabatic conditions.
- The superconducting tape under T_c is modeled by two branches in parallel; one is the entire tape with the superconducting layer in the normal state. The other branch represents the superconducting layer considering the power load for the electric field versus current to deduce an equivalent resistance.

Both edges of the conductor are an electrical equipotential. The conductor is inserted in an electrical circuit operating in voltage mode (limitation regime) or current mode (hot spot regime). For the hot spot regime, the I_c is lower (40 % reduction) in the center (spot 100 μm long).

The conductor is made by 5 layers:

- Hastelloy® (substrate, 100 μm).
- Superconductor (3 μm).
- Silver (2 μm).
- Tin (solder) (5 μm).
- Hastelloy® corrugated stabilizer.

The data ($c_p(T)$...) comes from handbook and from [23] for Hastelloy.

Fig. 14 shows the simulated temperature distributions 50 ms after having overstepped T_c in limitation conditions for different widths of the stabilizer (12 mm, 14 mm and 16 mm (tape width: 12 mm)) and for $L_{\text{stabilizer}}/L_{\text{tape}} = 2$ (it influences the current then dissipation distributions). The stabilizer section has been kept constant. The temperature distributions are similar in hot spot condition.

If the temperature remains very homogeneous across the whole conductor when the widths are the same, gradients appear when the stabilizer is wider than the tape. It even introduces an unfavorable temperature gradient in the tape width itself. We can conclude that the stabilizer cannot be larger than the tape by 1 mm (12 mm wide tape) and that a same width is better.

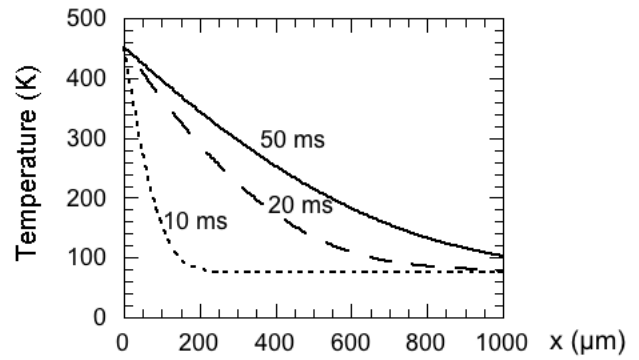


Fig. 13. Temperature distribution in a semi infinite Hastelloy® plan submitted to a temperature step at $t = 0$.

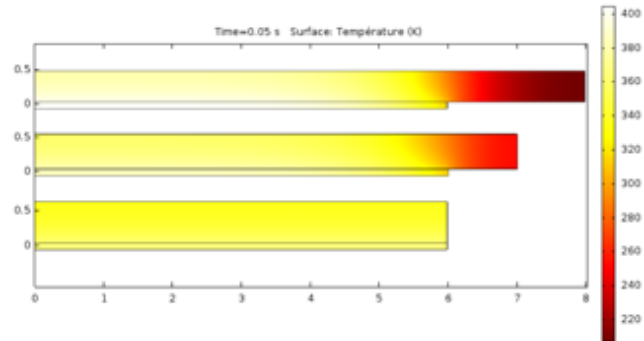


Fig. 14. Simulations of temperature distribution for different widths of stabilizer 50 ms after a quench.

But temperature diffuses also very hardly along the tape. Between two ribs the maximum temperature difference (Fig. 15) reaches (steady state, full conduction):

$$\Delta T = T_{max} - T_o = \frac{E_{lim}^2 L^2}{8} \frac{\frac{e_{Ag} + e_{Hast}}{\rho_{Ag} + \rho_{Hast}}}{\lambda_{Ag} e_{Ag} + \lambda_{Hast} e_{Hast}} \quad (17)$$

The second term depends little (within 30 %) on the silver/metallization thicknesses. So the only free parameter to limit the maximum temperature is L , distance between two ribs. If we want a limitation field of 300 V/m the distance L should be lower than 200 μm to keep the temperature difference under 50 K. A lower L favorably increases the ratio $L_{\text{stabilizer}}/L_{\text{tape}}$:

$$\frac{L_{\text{stab}}}{L_{\text{tape}}} = \frac{L + h_{tot}}{L + e_{\text{stab}}} \quad (18)$$

Thermal considerations then give the limits for the dimensions of the stabilizer:

- height (h_{tot}) lower than 700 μm
- distance between two ribs (L) lower than 200 μm .

The increase of the tape thickness (substrate) or electrical conductivity decreases the stabilizer thickness but lowers the electric field under limitation. It favorably forces more current in the stabilizer in normal state which then contributes more to the temperature rise limitation.

But the increase of the stabilizer length compared to the tape one reduces the amount of current flowing in the stabilizer.

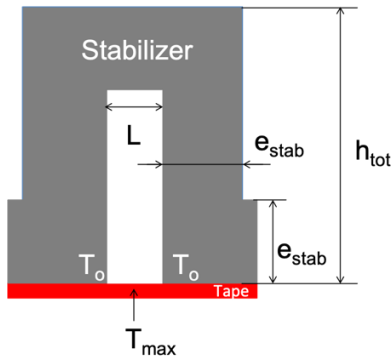


Fig. 15. Tape (in red) bonded to a corrugated stabilizer (in grey), location of the maximum temperature between two ribs.

Fig. 16 shows a possible conductor with two corrugated Hastelloy® stabilizers on both sides of the tape. The limitation of the stabilizer height leads to this configuration. In addition, two stabilizers protect mechanically the tape and makes it possible to have the SC layer on the neutral fiber to avoid mechanical stresses when wound. The positions of the two stabilizers may be shifted like in Fig. 16. The stabilizer has the same width compared to the tape to reduce the temperature gradients in the conductor section. The tape has a Hastelloy® substrate of $100\ \mu\text{m}$, a standard silver metallization layer of $2\ \mu\text{m}$. The total height of the conductor is about $1.5\ \text{mm}$ ($h_{\text{tot}} = 700\ \mu\text{m}$). The distance between two ribs (L) is $100\ \mu\text{m}$ and the stabilizer thickness $300\ \mu\text{m}$ (e_{stab}).

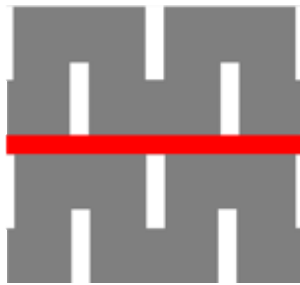


Fig. 16. Possible corrugated stabilizer conductor with top and bottom stabilizer offset.

Such a conductor should withstand an electric field of $200\ \text{V/m}$ (Fig. 17) and be safe in hot spot condition (Fig. 18). The temperature difference between the tape and the extremity of the stabilizer remains a little high (about $100\ \text{K}$) and we have nearly the same thermal conditions for limitation and hot spot regimes as designed.

Enhanced performances are possible using a metallization layer with reduced thickness and electrical conductivity. Optimizations should be carried out and above all experimental validations.

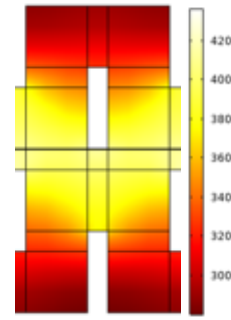


Fig. 17. Temperature distribution at the clearing time in limitation regime ($200\ \text{V/m}$) ($h_{\text{tot}} = 700\ \mu\text{m}$, $L = 100\ \mu\text{m}$, $e_{\text{stab}} = 300\ \mu\text{m}$).

Nevertheless, further work is needed to develop low cost and long length practical realization of such corrugated stabilizer, which is made very challenging by the small dimensions. The distance between the corrugations is tiny. Its filling by the solder must be avoided for example. The industrial implementation will require a lot of developments.

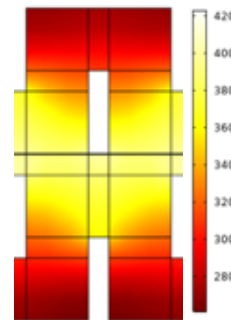


Fig. 18. Temperature distribution at the clearing time in hot spot regime ($I = I_c$) ($h_{\text{tot}} = 700\ \mu\text{m}$, $L = 100\ \mu\text{m}$, $e_{\text{stab}} = 300\ \mu\text{m}$).

IV. STABILIZER COMPARISON

The previous studies enable to make a very preliminary comparison between the corrugated stabilizer and dielectric stabilizer. Still a lot of works are required for both solutions.

TABLE
CORRUGATED AND DIELECTRIC STABILIZER COMPARISON

| | Corrugated stabilizer | Dielectric stabilizer |
|--|------------------------------------|--|
| <i>Implementation</i> | Challenging | Difficult |
| <i>Theoretical electric field under limitation</i> | High ($200\ \text{V/m}$) | Ultimate higher ($440\ \text{V/m}$) |
| <i>Issues</i> | Stabilizer realization at low cost | Dielectric material with good thermal conductivity and suitable elongation |

V. CONCLUSION

Stabilizer design is a key element for optimizing REBCO conductors for SFCL while keeping bare standard REBCO tape as a basis. We show that a dielectric stabilizer may be an attractive solution but a lot of issues have to be solved. This is due in particular to the thermal diffusivity within the stabilizer. Implementation is also a concern. We then concentrated on corrugated metallic (Hastelloy®) stabilizer on both sides of the tape. First investigations have showed that electric fields of 200 V/m are possible. Still higher values are certainly possible using further optimizations. In addition to these theoretical works corrugated stabilizer conductors must be realized and tested to verify and qualify this solution, as well as assess its feasibility as a cost-effective industrialized solution.

REFERENCES

- [1] B.G. Marchionini, Y. Yamada, L. Martini and H. Ohsaki, "High-Temperature Superconductivity: A Roadmap for Electric Power Sector Applications, 2015-2030", *IEEE Trans. on Applied Supercond.*, vol. 27, 0500907, 2017.
- [2] M. Moyzykh, D. Gorbunova, P. Ustyuzhanin, D. Sotnikov, K. Baburin, A. Maklakov, E. Magommedov, A. Shumkov, A. Telnova, V. Shcherbakov, D. Kumarov, L. Sabirov, M. Medovik, A. Kadyrbaev, S. Alexandrov, I. Mikoyan, S. Samoilnikov and A. Vasilov, "First Russian 220 kV superconducting fault current limiter (SFCL) for application in city grid", *Trans. on Applied Supercond.*, vol. 31, 5601707, 2021.
- [3] P. Tixador, M. Bauer, C.E. Bruzek, A. Calleja, G. Deutscher, B. Dutoit, F. Gomory, L. Martini, M. Noe, X. Obradors, M. Pekarčikova, F. Sirois, "Status of the European Project FASTGRID", *IEEE Trans on Applied Supercond.*, vol. 29, 5603305, 2019.
- [4] M. Noe, A. Hobl, P. Tixador, L. Martini, B. Dutoit, "Conceptual Design of a 24 kV, 1 kA Resistive Superconducting Fault Current Limiter", *IEEE Trans. on Applied Supercond.*, vol. 22, 5600304, 2012.
- [5] P. Tixador et A. Badel, "Superconducting Fault Current Limiter optimized design", *Physica C*, vol. 518, pp. 130-133, 2015.
- [6] A. Badel, G. Escamez and P. Tixador, "REBCO FCL Modelling: Influence of Local Critical Current Non-Uniformities on Overall Behavior for Various Tape Architectures", *IEEE Trans. on Applied Supercond.*, vol. 25, Art. N°5600504, 2015.
- [7] G. Deutscher, "High voltage superconducting fault current limiters based on high diffusivity substrates", *Journal of Superconductivity and Novel Magnetism*, vol. 31, p. 1961, 2018.
- [8] F. Irie, Y. Tsujioka and T. Chiba, "Characteristics of Critical Current Distribution for Oxide Superconductor Estimated from V-I Characteristics Using Weibull Function", *Superconductor Science and Technology*, vol. 5, S379-382, 1992.
- [9] J. Giguère, C. Lacroix, F. Dupuis-Desloges, J.H. Fournier-Lupien and F. Sirois, "High normal zone propagation velocity in copper-stabilized 2G HTS coated conductors", *Superconductor Science and Technology*, vol. 34, Art. no 045010, 2021.
- [10] C. Lacroix, F. Sirois and J.H. Fournier Lupien, "Engineering of second generation HTS coated conductor architecture to enhance the normal zone propagation velocity in various operating conditions", *Superconductor Science and Technology*, vol. 30, 064004, 2017.
- [11] A. Zampa, P. Tixador and A. Badel, "Experimental observations of the hot-spot regime on 2G HTS coated conductors", *Trans. on Applied Supercond.*, vol. 31, Art. 5601005, 2021.
- [12] THEVA, <https://www.theva.com/products/>
- [13] A. Zampa, "Effect of the Conductor Length on the Hot-Spot Regime for Resistive-Type Superconducting Fault Current Limiter", *IEEE Trans. on Applied Supercond.*, vol. 31, Art. N°3078818, 2021.
- [14] A. Kudymow, S. Elschner, S. Frink, W. Goldacker, A. Hobl, J. Schramm, and J. Brand, "2G HTS material selection, insulation, optimization, and the resulting component design of the Eccofow resistive fault current limiter", *presented at ASC'12*, 2012
- [15] F. Liang, W. Yuan, M. Zhang, Z. Zhang, S. Venuturumilli, and J. Patel, "The Impact of Critical Current Inhomogeneity in HTS Coated Conductors on the Quench Process for SFCL application", *IEEE Trans. on Applied Supercond.*, vol. 26, Art. N°5600605, 2016.
- [16] D. Colangelo, B. Dutoit, "Inhomogeneity effects in HTS coated conductors used as resistive FCLs in medium voltage grids", *Superconductor Science and Technology*, vol. 25, 095005, 2012.
- [17] P. Tixador, Y. Cointe, N. T. Nguyen, C. Villard, "Electrothermal phenomena about current limitation with Coated Conductor", *IEEE Trans. on Applied Superconductivity*, vol. 19, 2009, pp. 2305-2308.
- [18] C. Creusot, SuperGrid Institute, private communication.
- [19] S. Jeong and D. Kim, "Transient Heat transfer Experiment in Subcooled Liquid Nitrogen", *34th Intersociety Energy Conversion Engineering Conference*, August 2-5, Vancouver, Canada, 1999.
- [20] N.T. Nguyen and P. Tixador, "Influence of Architecture coated conductor YBCO to fault current limiter-visualisation analyse", *Superconductor Science and Technology*, vol. 23, 025008, 2010.
- [21] M. Pekarčiková, J. Mišík, M. Drienovský, J. Krajčovič, M. Vojenčiak, M. Búran, M. Moša, T. Húlan, M. Skarba, E. Cuninková, F. Gömöry, "Composite Heat Sink Material for Superconducting Tape in Fault Current Limiter Applications", *Materials*, vol. 13, 1832, 2020.
- [22] M. Pekarčiková, M. Drienovský, J. Krajčovič, J. Mišík, E. Cuninková, T. Húlan, M. Bošák, M. Vojenčiak, "Analysis of thermo-physical properties of materials suitable for thermal stabilization of superconducting tapes for high-voltage superconducting fault current limiters", *Journal of Thermal Analysis and Calorimetry*, vol. 138, pp. 4375-4383, 2019.
- [23] J. Lu, E.S. Choi, D. Zhou, "Physical properties of Hastelloy® C+276TM at cryogenic temperatures", *Journal of Applied Physics*, vol. 103, art. 064908, 2008.



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