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Antoine Sabrié, Alexandre Battiston, Fabien Vidal-Naquet, Jean-Yves Gauthier, Xuefang Lin-Shi. Analytical Derivation of Output Distortions Harmonics Caused by Voltage Source Inverter Non-Linearities in PMSM Drives. 25th Conference on Power Electronics and Applications (and Exhibition) (EPE 2023 ECCE Europe), Sep 2023, Aalborg, Denmark. 10.23919/EPE23ECCEurope58414.2023.10264340 . hal-04308904

HAL Id: hal-04308904

<https://hal.science/hal-04308904>

Submitted on 27 Nov 2023

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Analytical Derivation of Output Distortions Harmonics Caused by Voltage Source Inverter Non-Linearities in PMSM Drives

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Index Terms—Voltage Source Inverter (VSI), Harmonics, Dead-time, Parasitic elements, Wide bandgap

Abstract—This paper presents a new direct analytical derivation of low frequency harmonics introduced by voltage source inverters non-linearities in PMSM drives. The proposed voltage drops model is robust and requires fewer calculations than time-based models, and has proven to accurately estimate the experimental voltage drops for SiC based inverter output waveforms. Furthermore, it has been extensively validated experimentally and offers an analytical tool to precisely estimate the voltage drops introduced by the inverter non-linearities.

I. INTRODUCTION

Voltage source inverter fed Permanent Magnet Synchronous Machine (PMSM) coupled with an adequate Pulse-width modulation (PWM) has proven to be a very efficient solution. This is due to its high efficiency and passive filtering of high order harmonics inducing low Total Harmonic Distorsion (THD) in the output waveforms. However, the inverter is not ideal and can introduce a certain number of voltage drops causing undesired non-linear behavior. Such as the voltage drops of the switches and diodes, the required dead-times, or the turn-on and turn-off delays of the semiconductors. These added non-linearities introduce low frequency harmonics which are difficult to filter out and are at the origin of low frequency current ripple in the machine if they are not compensated by the controller. This induces in turns undesired torque ripple and impacts efficiency.

Numerous work in the literature aims at compensating these undesired effects in the PMSM drives [1]. The compensation techniques can be based on instantaneous

average voltage compensation, as proposed in [2], [3]. One of the main drawback is that the compensation scheme is dependent on the polarity of the current. Thus very difficult to accurately compensate in near-zero current operation. In [4] the authors proposed an analysis and compensation scheme based on look-up tables to improve performances in zero crossings regions. Furthermore, a model-based compensation will never truly mitigate all voltage drops due to parameters identification. An on-line estimator based on the voltage drops is proposed in [5] but suffers from the same drawbacks as the average value compensation. Advanced algorithms based on observers aims at compensating the given 6th order harmonics in the dq rotary reference frame [6], [7]. These methods achieve good compensation in steady state but exhibit poor performances in dynamic responses. As proposed in [8], in which a model-based is coupled with a current observer to compensate voltage drops in both steady state and dynamic responses. But the study does not considerate the parasitic capacitance, which can have a huge impact on voltage drops [9]. Methods based on models alone cannot truly compensate the voltage drops. In the other hand, advanced disturbance observer, or repetitive control which are not based on models can accurately compensate in the steady-state but not in dynamic responses.

In this paper a simple analytical model of the voltage drop is proposed based on a frequency analysis of the voltage drops and undesired non-linear behavior. To the author's knowledge, direct harmonics calculation is complex and requires high computational resources, as can be described for the switching frequency current har-

monics derived in [10]. In order to improve the dynamic response of such complex compensation algorithm, this paper aims at proposing a simple analytical derivation of the low frequency harmonics of the voltage drops. Furthermore, in the litterture only partial validation of the models and compensation scheme are done on specific operating points. In this paper, a thorough validation in all accessible operating point is done to remove any bias.

The paper is structured as follows : In section II a more complete voltage drop model based on various previous works is presented, then in section III the analytical derivation of the low-order harmonics will be done. Finally, simulations and experiments to validate the robustness of the proposed model are presented in section IV and, section V respectively.

II. NON-LINEARITIES MODELLING IN VSI

This section focuses on the development of the voltage drop average model over a swiyching period T_{sw} . It will be done considering an equivalent half bridge as presented in figure Fig. 1. The pole voltage V_{ao} can be expressed by the switched drain-source voltage across the low side MOSFET of the half bridge. The ideal perfect pole voltage V_{ao} in this condition is defined by equation (1). Where V_{DC} is the DC bus voltage and $C_a(t)$ is the gating signals of the MOSFET.

$$V_{ao}^{ideal} = V_{DC} \cdot C_a(t) \quad (1)$$

The Fig. 2 summarizes all the considered the voltage drops sources introduced referenced to the ideal voltage. In comparison, the Fig. 3 presents the voltage $\Delta V_{ao} = V_{ao} - V_{ao}^{ideal}$ obtained at the output of the half bridge when all presented non-linearities are taken into account.

A. Voltage drops due to dead-times and switching delays

Dead-times are added between the gating signals of the two MOSFETs of the half bridge to prevent any short-circuit of the DC bus voltage. The error introduced in the phase voltage is presented in Fig. 2 in the fourth sub-graph. The dead-times will induce a delay of the establishment of the pole voltage. Since the ideal voltage is the switched voltage corresponding to the DC bus voltage, the error introduced has an amplitude of V_{DC} during the dead time. Due to the way of generating the dead-times, the error will change sign depending on the current polarity. The voltage drop introduced by dead-times is thus expressed as (2).

$$\Delta V_{ao}^{DT} = \frac{T_{dead}}{T_{sw}} \cdot V_{DC} \cdot \text{sign}(i_a) \quad (2)$$

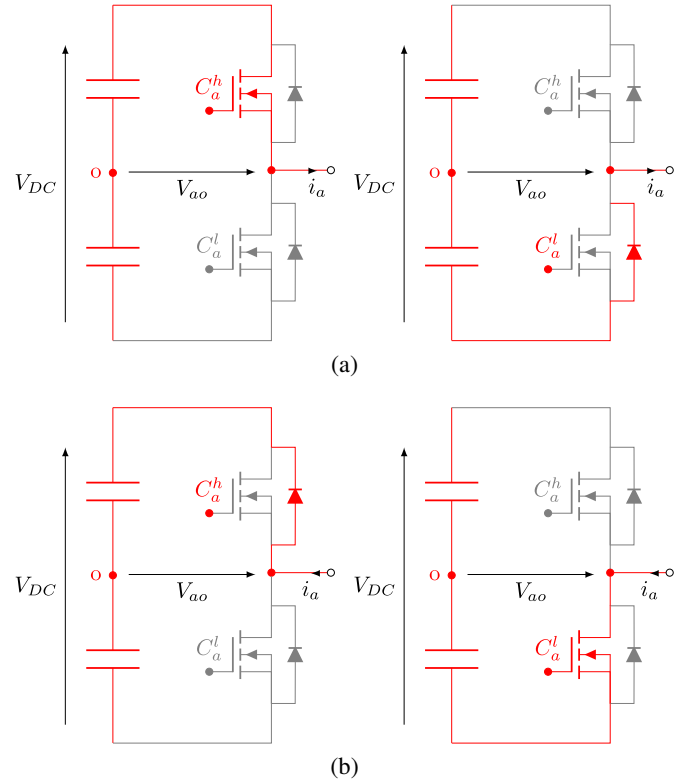


Fig. 1: Four principle conduction cases depending on current polarity and gating signals: (a) - for positive current polarity, (b) - for negative current polarity

Another non-linearity introduced is due to the switching delays at turn-on and turn-off, as presented in Fig. 2 on the third sub-graph. Normally it should vary with different parameters such as the peak phase current I_{peak} , V_{DC} or the temperature, but it would complicate the model and has a lesser impact than the dead-times. It is possible to calculate the error induced by turn-on and turn-off delays as expressed in (3).

$$\Delta V_{ao}^{sw} = \frac{t_{on} - t_{off}}{T_{sw}} \cdot V_{DC} \cdot \text{sign}(i_a) \quad (3)$$

Due to the very close similarity with the dead-time, it is easier to express all of them in the same equation as proposed in (4).

$$\Delta V_{ao}^{DT+sw} = \frac{T_{dead} + t_{on} - t_{off}}{T_{sw}} \cdot V_{DC} \cdot \text{sign}(i_a) \quad (4)$$

B. Voltage drops due to conduction

The figure Fig. 1 presents the active component in which the current is flowing. As it can be seen it depends on the polarity of the current, the gating signal $C_a(t)$, and if takes place during the dead-time. Thus, defining

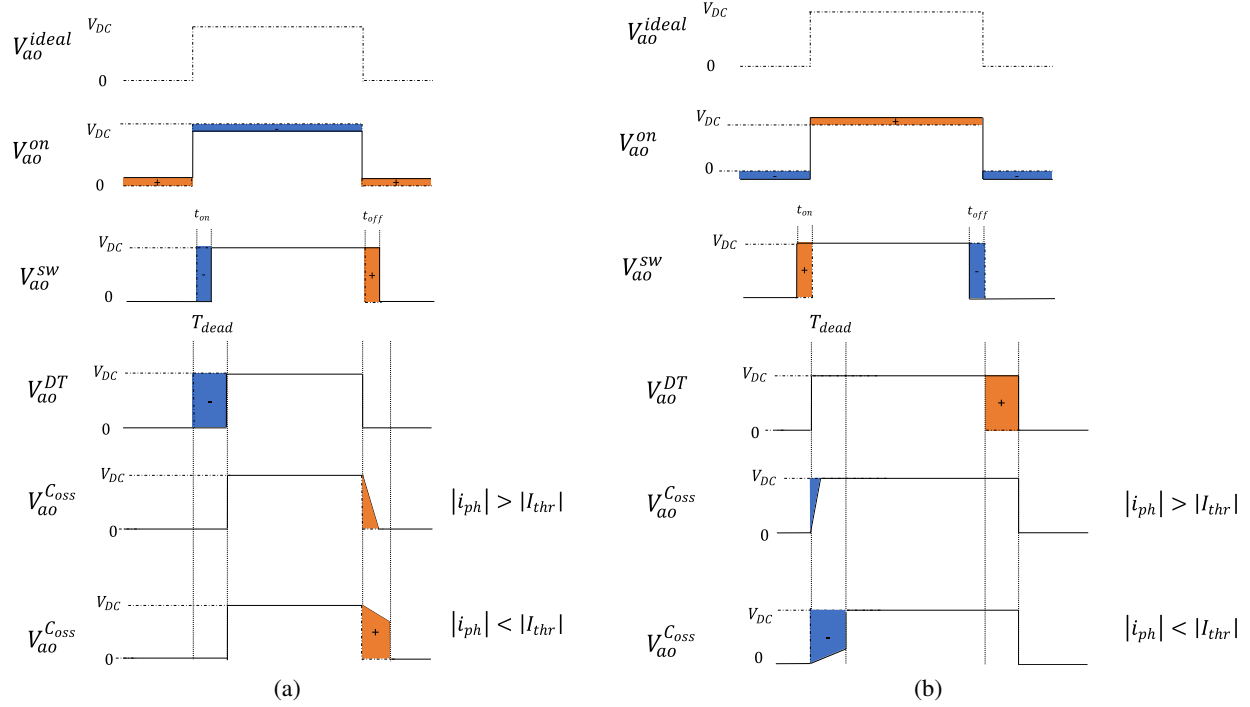


Fig. 2: Contribution of each considered non-linearity, referenced to the ideal phase voltage (a) - for positive current polarity, (b) - for negative current polarity

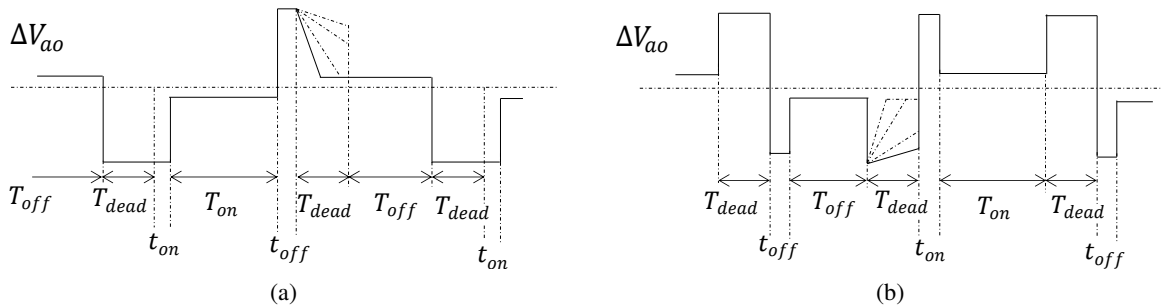


Fig. 3: Total voltage drop considering every non-linearity of the VSI : (a) - for positive current polarity, (b) - for negative current polarity

if the current is flowing through the MOSFET or the diode. Two more cases apart from the one represented in Fig. 1 are taken into account. Those cases corresponds of the voltage drop due to conduction happening during the dead diode where the diode in respect to current polarity is conducting. The sign of the error induced depends on the polarity of the current and on the on state of the MOSFET or diode. A summarized version of those voltage drops can be seen in Fig. 2 on the second subgraph. The voltage drop introduced by the conduction of the semiconductor can be expressed considering, in all six cases, the on-state model of the MOSFET and its

antiparallel diode V_{DS} and V_d expressed in (5).

$$\begin{aligned} V_{DS} &= R_{DS}^{on} \cdot i_a \\ V_d &= V_{do} + r_d \cdot i_a \end{aligned} \quad (5)$$

Where R_{DS}^{on} and r_d are the ON-state resistances. One proposed model in [11] is done by differentiating the actual time when the MOSFET is ON or OFF from the ideal one. Let us define $C_a(t)$ the duration during which the high side MOSFET of phase A is ON during the switching period T_{sw} . By definition, the duty cycle is given by (6).

$$\overline{C}_a(\theta) = \frac{1}{T_{sw}} \int_0^{T_{sw}} C_a(t) dt \quad (6)$$

Where $\theta = \omega t$. If $C_a^*(\theta)$ is the ideal duty cycle that should be applied, then the difference between the real time and the ideal is due to dead-times and the switching delays and can be expressed as (7).

$$\overline{C}_a(\theta) = \overline{C}_a^*(\theta) - (T_{dead} + t_{on} - t_{off}) \cdot \text{sign}(i_a) \quad (7)$$

The voltage drop from the ideal applied voltage can be extensively described in each conduction case by (8)

$$\begin{aligned} \Delta V_{ao}^{on} &= (\overline{C}_a(\theta) R_{DS}^{on} i_a \\ &+ (1 - \overline{C}_a(\theta))(V_{do} + r_d i_a)) \cdot \left(\frac{1 + \text{sign}(i_a)}{2}\right) \\ &+ ((1 - \overline{C}_a(\theta)) R_{DS}^{on} i_a \\ &- \overline{C}_a(\theta)(V_{do} - r_d i_a)) \cdot \left(\frac{1 - \text{sign}(i_a)}{2}\right) \end{aligned} \quad (8)$$

C. Voltage drops due to Parasitic capacitance

The effect of the parasitic capacitance on output voltage distortions has been studied in previous work solely. The parasitic capacitance plays a role in the switching waveforms during dead-time and switching transitions. The model presented was derived from [9]. During a turn-on sequence, for example, the voltage V_{DS} is initially equal to V_{DC} and the parasitic capacitance is charged. If the magnitude of the phase current at the given instant is high enough, the capacitance is very quickly discharged and no effect can be noticed. However, when the magnitude is close enough to zero, the discharge of the parasitic capacitance is much slower and holds its voltage value V_{DC} for a certain amount of time until the end of the dead time when the voltage is clamped to zero. The time needed to discharge the parasitic capacitance is stated in (9), where the factor 2 appears because the current needs to discharge the two parasitic capacitance in series from the high and low side MOSFET. And with the hypothesis that the current is fairly distributed among the two. The two last sub-graphs of Fig. 2 describes the voltage drop associated.

$$\Delta t = 2C_{oss} \cdot \frac{V_{DC}}{i_a} \quad (9)$$

From the defined Δt , we can differentiate if the capacitor has enough time to discharge during the dead-time. This condition is expressed if the magnitude of the

phase current i_a is enough to discharge the capacitor quickly enough. Thus, drawing the expression of the threshold current given in equation (10)

$$I_{thr} = 2C_{oss} \cdot \frac{V_{DC}}{T_{dead}} \quad (10)$$

The voltage error created is actually opposite to the voltage drops due to the dead-time. Meaning, in one switching cycle, A positive voltage error can be created from the dead-time and a negative one from the parasitic capacitance. The actual voltage error can be derived from the difference of the two. In fact, the simple model of the dead-time and switching delays tend to overestimate and by far the true level of voltage drop. The total voltage drop due to the dead-time taking into account the parasitic capacitance are expressed in (11) and (12) depending on the magnitude of the current.

When $i_a \geq I_{thr}$

$$\begin{aligned} \Delta V_{ao}^{DT+C_{oss}} &= \frac{1}{T_{sw}} \left((T_{dead} + t_{on} - t_{off}) \right. \\ &\left. \cdot V_{DC} \cdot \text{sign}(i_a) - \frac{C_{oss} V_{DC}^2}{i_a} \right) \end{aligned} \quad (11)$$

When $i_a \leq I_{thr}$

$$\Delta V_{ao}^{DT+C_{oss}} = \frac{i_a \cdot (T_{dead} + t_{on} - t_{off})^2}{4C_{oss} T_{sw}} \quad (12)$$

The complete averaged model of the voltage loss considering all non-linearities sources is defined in (13) :

$$\Delta V_{ao} = \Delta V_{ao}^{on} + \Delta V_{ao}^{DT+C_{oss}} \quad (13)$$

III. DIRECT ANALYTICAL DERIVATION OF THE LOW FREQUENCY HARMONICS

The complete model above describes the total voltage drops due to the inverter non-linearities. In this section a frequency analysis of the time-based averaged model will be done in steady state. Thus an analytical way of calculating the harmonics introduced by the voltage drops will be done. Since the harmonics to compensate can be known in advance a quick analytical derivation of such harmonics could be done.

A. Voltage drops due to conduction

For this purpose, the voltage error ΔV_{ao} needs to be described in the frequency domain based on the knowledge known on the time-based one. The objective is to define from the complete time varying model

equation as ΔV_{ao} stated in (13). The proposed method in this paper is to replace the instantaneous values by their Fourier coefficient regarding the desired harmonic. For simplicity and due to the experimental setup, most of the work presented in the following are for the fundamental harmonic. Nevertheless, the procedure is the same for low voltage harmonics like the 5th, the 7th, 11th or 13th. The harmonic of higher ranks will not be considered, since their amplitude will be very low and their impact negligible. The switching harmonics will also not be derived and would require a lot more complexity in the model and since there are naturally filtered by the load, they have a lesser impact on the torque ripple.

The ideal phase currents references are supposed perfectly sinusoidal and are described in (14).

$$i_a(\theta, \phi) = I_{peak} \cdot \sin(\theta - \phi) \quad (14)$$

The polarity of the current is a term that appears also in the model. Since it is a square wave of amplitude one, its Fourier series is given in (15).

$$\mathcal{F}(\text{sign}(i_a(\theta, \phi))) = \frac{4}{\pi} \sum_{k=1,3,5,7,9,11,13} \frac{1}{k} \sin(k\theta) \quad (15)$$

The duty cycle in the case of a Space Vector Pulse Width Modulation (SVPWM) for half the fundamental period is described as follows (16)

$$\overline{C}_a(\theta) = \begin{cases} \frac{1}{2}(1 + m \cos(\theta - \frac{\pi}{6})), & \theta \in [0; \frac{\pi}{3}] \\ \frac{1}{2}(1 + m\sqrt{3} \cos(\theta)), & \theta \in [\frac{\pi}{3}; \frac{2\pi}{3}] \\ \frac{1}{2}(1 + m \cos(\theta + \frac{\pi}{6})), & \theta \in [\frac{2\pi}{3}; \pi] \end{cases} \quad (16)$$

The Fourier series of this signal is given in (17).

$$\overline{C}_a(\theta) = \frac{1}{2} + \frac{m}{\sqrt{3}} \sin(\theta) + \frac{m}{\pi^2} \sum_{k=3,5,7,\dots}^{\infty} \frac{1}{k^2} \sin(3k\theta) \quad (17)$$

From (8) a quick analysis of the developpement is made. Then retaining only the terms that have an impact on the fundamental harmonic in (8), the fundamental harmonics of the voltage drop due to conduction can be expression as (18):

$$\Delta V_{ao}^{on}(\theta) = \frac{R_{DS}^{on} + r_d}{2} i_a + \frac{R_{DS}^{on} + r_d}{2} i_a \text{sign}(i_a) + V_d \frac{1 + \text{sign}(i_a)}{2} + (R_{DS}^{on} - r_d) C_a(\theta) \cdot i_a \cdot \text{sign}(i_a) - C_a(\theta) \cdot V_{do} \quad (18)$$

Considering all the derived harmonic contribution of each terms, the fundamental voltage drop harmonics can be derived. The cross product $C_a(\theta) \cdot i_a \cdot \text{sign}(i_a)$ can be derived using the classical description of the Fourier series given in (19)-(21).

$$f(\theta) = a_0 + \sum_n a_n \cos(\frac{n\pi\theta}{T}) + \sum_n b_n \sin(\frac{n\pi\theta}{T}) \quad (19)$$

$$a_n = \frac{1}{T} \int_{-T}^T f(\theta) \cos(\frac{n\pi\theta}{T}) d\theta \quad (20)$$

$$b_n = \frac{1}{T} \int_{-T}^T f(\theta) \sin(\frac{n\pi\theta}{T}) d\theta \quad (21)$$

Finally, considering the phase of each term, neglecting the dead-time effect on conduction which is in the considered case negligible, a simple analytical description of the fundamental harmonic of the voltage drop introduced by the conduction of semiconductors is given by (22).

$$\mathcal{F}^1(\Delta V_{ao}^{on}) = \frac{R_{DS}^{on} + r_d}{2} I_{peak} + \frac{4}{\pi} \frac{V_d}{2} - \frac{m}{\sqrt{3}} \cdot \sin(\phi) \cdot V_{do} + (R_{DS}^{on} - r_d) \frac{2}{3\pi} \sqrt{I_{peak}^2 m^2 (3 \sin^2 \phi + 1)} \quad (22)$$

B. Voltage drops due to dead-times considering parasitic capacitance and switching delays

Regarding the voltage drops due to the dead time considering the parasitic capacitance effect, the instantaneous function given in (11) and (12) contains conditions. Thus, a symbolic calculation of the Fourier coefficient on the different piecewise description has been done. The function being uneven, only the b_n coefficient requires calculation and is done from (21). The result of the symbolic integration of the fundamental harmonic is given in (23). Thus, an equation for the direct analytical derivation of the fundamental component is proposed.

$$\begin{aligned}
\mathcal{F}^{b1}(\Delta V_{ao}^{DT+C_{oss}}) = & \\
& \frac{I_{peak}T_{dead}^2}{4C_{oss}T_{sw}} + \frac{3V_{DC}\sqrt{I_{peak}^2T_{dead}^2 - 4C_{oss}^2V_{DC}^2}}{I_{peak}T_{sw}\pi} + \frac{I_{peak}T_{dead}^2 a \sin\left(\frac{2C_{oss}V_{DC}}{I_{peak}T_{dead}}\right)}{2C_{oss}T_{sw}\pi} \\
& + \frac{4C_{oss}V_{DC}^2 a \sin\left(\frac{2C_{oss}V_{DC}}{I_{peak}T_{dead}}\right)}{I_{peak}T_{sw}\pi} - \frac{\pi I_{peak}T_{dead}^2}{4C_{oss}T_{sw}\pi} - \frac{2\pi C_{oss}V_{DC}^2}{I_{peak}T_{sw}\pi} - \frac{I_{peak}T_{dead}^2 \cos(\pi) \sin(\pi)}{4C_{oss}T_{sw}\pi} \quad (23)
\end{aligned}$$

TABLE I: Simulated and experimental setup parameters

Parameter	Symbol	Value
DC bus Voltage	V_{DC}	350 V
Switching frequency	f_{sw}	10kHz
Dead time	T_{dead}	700 ns
Turn-on delay	t_{on}	120 ns
Turn-off delay	t_{off}	100 ns
MOSFET On resistance	R_{DS}^{on}	3.2 m Ω
Diode forward voltage	V_{d0}	0.8
Diode on resistance	r_d	2.3 m Ω
Intrinsic parasitic capacitance	C_{oss}	25 nF
Number of pole pairs	p	4
Motor Inductances	L_d	460 μ H
	L_q	430 μ H
Motor Resistance	R_s	39m Ω
Flux linkage	ϕ_f	0.131 Wb
Speed reference	Ω^*	1000 rpm
Maximal load Torque	Γ_{ch}	410 Nm

IV. SIMULATION RESULTS

A simulation of a PMSM fed by a three-phase inverter has been carried out in MATLAB Simulink and the SymPowerSystem library. The machine is a traction machine for drives application. The parameters are the one used experimentally and are given in Tab. I. In order to validate the robustness of the approach, the analysis has been done not only on the optimal point or trajectory usually used but on the entire accessible operating point of the machine, even non-optimal ones. For this purpose, a mapping of all couple Direct and Quadratic current i_d and i_q have been done. The machine is connected in a back to back configuration and sees its mechanical shaft speed imposed at $\Omega = 1000rpm$. The implemented control scheme for the simulation is presented in Fig. 4. The two references of i_d^* and i_q^* are thus given by (24).

$$\begin{aligned}
i_d^* &= I_{peak} \sin(\delta) \\
i_q^* &= I_{peak} \cos(\delta) \quad (24)
\end{aligned}$$

In order to validate the proposed analytical and direct derivation of the harmonics, a comparison is carried

out between the simulation estimated voltage drop referenced to V_{ao}^{ideal} and the on-line calculation of the fundamental component. The time-based voltage drops estimated by the simulation needs to be post processed to obtain the first harmonic. The difference in voltage drop ΔV_{ao} first harmonic between the voltage drop obtained in simulation and the simplified under hypothesis proposed first harmonic calculation is presented in Fig. 5. It can be seen that the derived harmonic calculation is very close to the harmonic obtained with the FFT of the voltage drop obtained in simulation, with less than at most 0.4V of error in the estimation of ΔV_{ao} under worst case scenario in near zero currents and abrupt change in polarity. Thus, simplified direct fundamental analytical derivation under hypothesis engenders small errors. This proves that a simpler derivation of the fundamental harmonics of the voltage drop can be accurately estimated, knowing only basic datasheet parameters of the inverter and simple measurements of the current on any operating point.

V. EXPERIMENTAL RESULTS

In order to validate the results experimentally, the protocol carried was as follows. The output of the PI controllers, meaning the references voltages, V_d^* and V_q^* were measured. Furthermore, the three-phase currents I_{abc} and well as all line-to-line voltages U_{ab} , U_{bc} and U_{ca} were measured with a wattmeter giving their respective RMS and mean values. Since the real V_d and V_q as well as the real i_d and i_q applied to the machine are needed for the controlled, were also measured and saved. Thus, a database has been created with all needed mean values applied experimentally. The same protocol described in the section IV was carried out for all operating points. Meaning, a mapping of i_{dq} have been done experimentally. Since the experimental result have been done in closed-loop control, the reference values of V_d^* and V_q^* will be higher than the real applied V_d V_q to attain the given reference steady-point. This means that the control will mitigate at least in mean values the voltage drops.

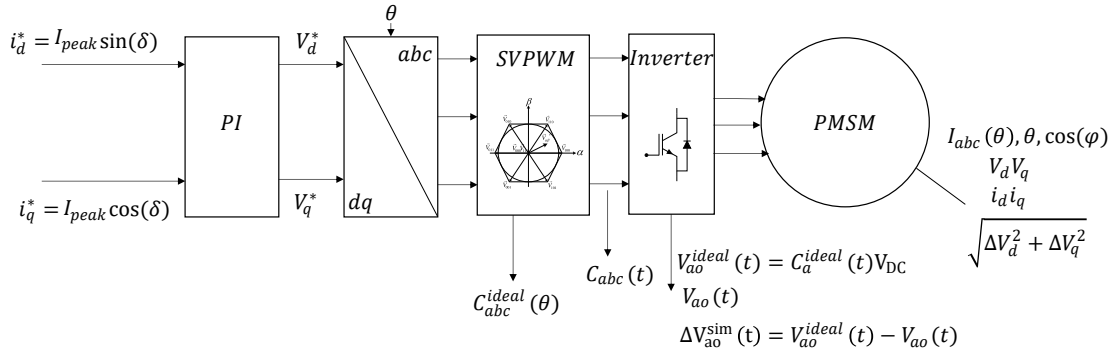


Fig. 4: Control scheme setup for both simulation validation

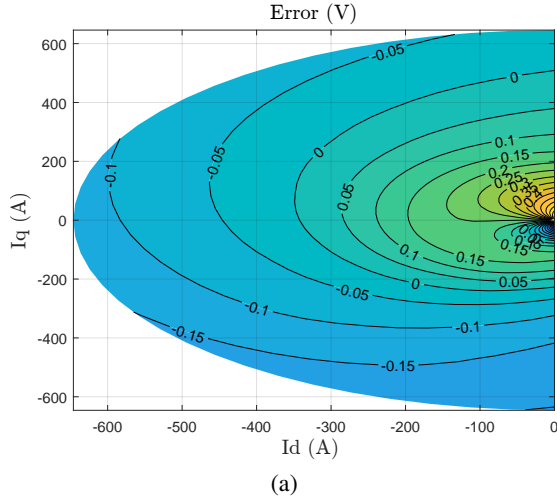


Fig. 5: Error of calculated voltage drop between simulation model and direct analytical model calculated on-line

In steady-state operation, it is possible to define the real applied $V_d V_q$ and the references V_d^* and V_q^* . Thus, the difference of the control signals references V_d^* and V_q^* and the real V_d and V_q can be used to estimate experimentally the voltage drops due to the inverter nonlinearities as expressed in (25). Finally, to estimate the voltage drop, the norm $\sqrt{\Delta V_d^2 + \Delta V_q^2}$ is calculated.

$$\begin{aligned} V_d^* - V_d &= \Delta V_d \\ V_q^* - V_q &= \Delta V_q \end{aligned} \quad (25)$$

The obtained mapping, in the i_{dq} plane, of the estimated voltage drops $\sqrt{\Delta V_d^2 + \Delta V_q^2}$ experimentally, the simulation and the analytical derivation are presented in Fig. 6 and shows the absolute level of voltage drop estimated. In order to validate the proposed analytical derivation, the contour of error between the experimental voltage drop and the proposed fundamental derivation is

plotted in Fig. 7. It can be seen that the derived direct harmonic calculation presents good performances of estimation of the actual experimental voltage drop with less than 0.4V in difference for the majority of operating points in the $i_d i_q$ map except in near zero currents region. This is due to the loss of precision of the current polarity detection as well as the zero current clamping phenomenon due to the dead time. Furthermore, the intrinsic parameters extracted from the datasheet can not be perfectly estimated and presents variation in real application. The temperature dependency for instance is partially taken into account. This is one limit of the model. However, although not shown here, the added parasitic capacitance effect make the estimation far more precise compared to models that do not take it into account. Furthermore, the error between the models and the experimental could be explained by other factors such as the parametric error that could be also compensated by the control. Meaning that the method to derive the voltage loss experimentally can be improved. But the presented protocol can be achieved with any motor easily without added measurements. Nevertheless, the experimental results show that the analytical derivation of the fundamental component of the voltage drop can approximate the real voltage drop with a difference less than a volt.

One of the advantages of such analytical voltage drops model is that it can be used to study the impact of each parameters on the voltage drops. For demonstration purposed, the purple map plotted in Fig. 6 represents the same voltage drop model without considering the intrinsic capacitance, as is done in most dead-time averaged models. This illustrates the importance of taking it into account, otherwise the compensated voltage drop will be largely overestimated. It also concord with the observation made in [9], that the intrinsic capacitance tends to naturally attenuates the voltage drop introduce

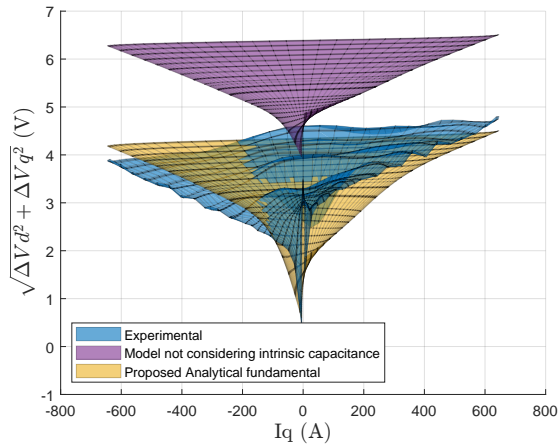


Fig. 6: Map in the i_{dq} plane of the estimated voltage drops (V). Comparison between the experimental points, the simulation and the proposed direct analytical derivation

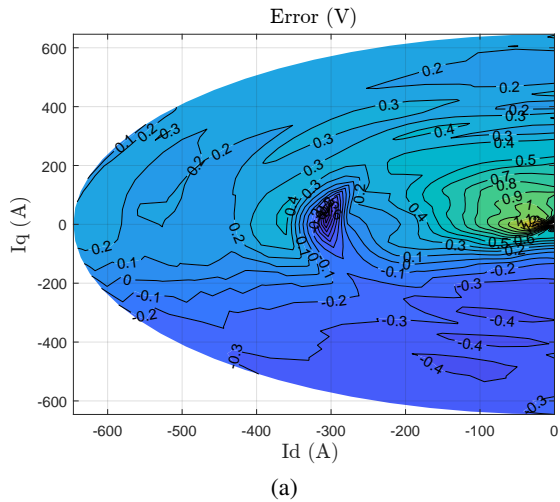


Fig. 7: Contour of error (V) between the estimated experimental voltage drop ΔV_{ao} and the direct harmonic derivation of the voltage drop with the known experimental parameters.

by dead-times. This also shows that the model can be easily used as a tool to evaluate the individual impacts of each parameters.

VI. CONCLUSION

In this paper, an extensive instantaneous model time-based models based on previous literature work have been proposed. Based on this model, this paper proposes an analytical derivation of the low frequency harmonics that are the harder to filter out and impact the most in the load with current and torque ripple. This paper has made the statement that only the amplitude of the harmonics

of the voltage drops are truly necessary to describe the non-linearities introduced by the VSI instead of time based version previously proposed in the literature. The analytical direct derivation of the fundamental harmonic show very good concordance with the time-based model harmonics as well as the one obtained by simulation model of the inverter non-linearities, thus showing the robustness of the approach. Then the analytical harmonics are used to estimate the voltage drops of introduce by a VSI experimentally on all accessible operating points at given speed and DC bus voltage. The results show that the model offers good performance and can accurately estimate the true voltage experimental voltage drop. Errors in the approach are nonetheless engendered, but are due to parametric estimation of the intrinsic parameters that are still needed, as well as the well-known difficulties of precise current polarity detection and measurement. The proposed work offers a complete voltage drops model that is quite accurate with reduced computation time. Furthermore, the analytical computations can offer a pre-study of the voltage drops for any given inverter. Since the model has been extensively validated both by simulation and experimentally. In order to make the most of this model, it could be paired with advanced disturbance observers to improve dynamic performance of such proposed advance compensation techniques.

REFERENCES

- [1] Y. Ji, Y. Yang, J. Zhou, H. Ding, X. Guo, and S. Padmanaban, "Control strategies of mitigating dead-time effect on power converters: An overview," *Electronics*, vol. 8, no. 2, p. 196, 2019.
- [2] D.-H. Lee and J.-W. Ahn, "A simple and direct dead-time effect compensation scheme in pwm-vsi," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3017–3025, 2014.
- [3] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 3179–3187, 2014.
- [4] S. M. Seyyedzadeh and A. Shoulaie, "Accurate modeling of the nonlinear characteristic of a voltage source inverter for better performance in near zero currents," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 71–78, 2019.
- [5] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "An adaptive dead-time compensation strategy for voltage source inverter fed motor drives," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1150–1160, 2005.
- [6] D.-M. Park and K.-H. Kim, "Parameter-independent online compensation scheme for dead time and inverter nonlinearity in ipmsm drive through waveform analysis," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 701–707, 2014.

- [7] X. Hao and Y. Luo, "An smc-eso-based distortion voltage compensation strategy for pwm vsf of pmsm," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 5, pp. 5686–5697, 2022.
- [8] Y. Wang, W. Xie, X. Wang, and D. Gerling, "A precise voltage distortion compensation strategy for voltage source inverters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 59–66, 2018.
- [9] D. Wang, P. Zhang, Y. Jin, M. Wang, G. Liu, and M. Wang, "Influences on output distortion in voltage source inverter caused by power devices' parasitic capacitance," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4261–4273, 2018.
- [10] W. Liang, J. Wang, P. C.-K. Luk, W. Fang, and W. Fei, "Analytical modeling of current harmonic components in pmsm drive with voltage-source inverter by svpwm technique," *IEEE Transactions on Energy Conversion*, vol. 29, no. 3, pp. 673–680, 2014.
- [11] H. Zhao, Q. Wu, and A. Kawamura, "An accurate approach of nonlinearity compensation for vsf inverter output voltage," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 1029–1035, 2004.