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Simplified Assembly of through silicon via Integrated Ion Traps

Peng Zhao, *Student Member, IEEE*, Hong Yu Li, Theo Henner, Jean-Pierre Likforman, Yu Dian Lim, Liang Xing Hu, Wen Wei Seit, Guidoni Luca, and Chuan Seng Tan, *Fellow, IEEE*

Abstract—The scalability of surface electrode ion traps has been progressively improved with the on-chip integration of conventional bulk components. Based on the development of through silicon via (TSV) integrated ion trap, in this work, we further simplify the back-end assembly process by patterning a redistribution layer (RDL) onto customized ceramic pin grid array (CPGA) package. This RDL has internal connection with CPGA pin on the back side, rerouting the electrical signal and facilitating the direct bonding of TSV trap and CPGA. The patterned neighboring RDL has an averaged resistance of 4.5×10^{12} ohm, three orders of magnitude higher than that of TSV trap itself. As compared to the previous assembly (glass interposer wire bonded to a conventional CPGA), a small parasitic capacitance increase of 0.1 pF of the customized CPGA is observed. Radio frequency (RF) electrical tests indicate that the trap on customized CPGA will not induce additional power loss. Meanwhile, due to the high thermal conductivity of ceramic materials, the heat dissipation capability of the customized CPGA is boosted. The functionality of TSV trap on customized CPGA is also demonstrated by trapping and laser-cooling $^{88}\text{Sr}^+$ ions. The measured heating rate (310 ± 60 mK/s) and lifetime (30 minutes) are comparable with the trap assembled in previous approach. This indicates that the CPGA with built-in RDL is fully compatible with ion trapping applications, providing a new approach towards compact, flexible, and robust ion trap assembly.

Index Terms—Ceramic Pin Grid Array, Redistribution Layer, Surface Electrode Ion Trap, TSV

I. INTRODUCTION

QUANTUM computing, bearing the potential to solve intractable problems by classical computing, has been under extensive developments over the past several decades, from theory to experiment and from algorithm to hardware [1]. Various physical implementation platforms have been proposed and demonstrated, including superconducting circuit, trapped ion, photon, quantum dot, with their specific potentials and limitations [2, 3]. Amid these platforms, trapped ions have become one of the most popular candidate, due to its robust lifetime, long coherence times, high gate fidelity and exclusive reconfigurability [4]. Meanwhile, the development of surface electrode traps in 2005 constituted a trap architecture that is compatible with advanced fabrication processes (MEMS and CMOS), making it suitable for a large scale implementation [5, 6].

Typically, trapped ions are dynamically confined by a RF electric field in an ultra-high vacuum (UHV) chamber. This enables an excellent isolation from a noisy environment. Besides RF fields, non oscillating fields are also required for axial movement control. Quantum information (qubit) in trapped ions is encoded in two internal states of the atom. Laser beams are used for qubit manipulations and also for ionization, readout and cooling. The two-qubit gates are achieved using the shared motional mode together with single qubit rotations.

Owing to the advanced process compatibility of surface electrode traps, various originally bulk modules have been continuously integrated onto the trap substrate [7]. In year 2021, our group developed a through silicon via (TSV) integrated ion trap [8, 9], in which 3D interconnect TSV were integrated underneath surface electrodes, in place of conventional wire bonding. A corresponding glass interposer with a redistribution layer (RDL) was also designed and fabricated, where TSV integrated trap could be bonded on its top. To facilitate robust and flexible electrical feedthrough from a motherboard socket, the bonded trap was further assembled into a conventional ceramic pin package array (CPGA) carrier (Fig. 1(a)). The assembly process is relatively

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intricate, in which the bonded trap (i.e., trap on interposer) was first required to be pasted onto a glass spacer (thickness ~ 750 μm). This was to raise the trap surface and make it higher than the CPGA, since the CPGA has a sunken cavity with a depth of ~ 1400 μm . The paste used should also be UHV compatible. Subsequently, to connect the RDL on glass interposer and lead frame on CPGA, extra wire bonding was still essential, though it was not directly on the surface electrode. A long electrical signal transmission path from CPGA pin to surface electrode was formed, via CPGA lead frame, wire bonding, RDL on glass interposer, microbump and TSV.

To simplify the assembly process between trap and socket, we explore the elimination of the glass interposer and wire bondings. By patterning an RDL layer onto the CPGA and building internal connections from this RDL to the CPGA pin, the direct bonding of TSV trap and CPGA can be achieved (Fig. 1(b)). The abovementioned electrical signal transmission path is consequently shortened. In this simplified design, the CPGA is not only a packaging apparatus, but also an essential part of the ion trap, determining the delicate rerouting of the electric signal. Indeed, pin grid arrays (PGA) have been widely used for decades to bridge the silicon die and organic motherboard, due to its high I/O density, fan-out circuitry and demountable capability [10]. CPGA is one of the most popular candidates amid various PGA products, in view of the low dielectric constant, high thermal conductivity and cost-effective manufacturing of ceramic materials (e.g., alumina, aluminum nitride, etc.). It is also expected that the direct bonding onto CPGA will promote the heat dissipation from RF traps. In brief, locating a TSV integrated ion trap on a CPGA with built-in RDL facilitates a flexible, robust, and ultra-compact trap-package architecture. On top of that, this architecture provides a possible route towards the goal to build a compact UHV ion trapping system to simultaneously maximize the system flexibility and the mechanical stability [11, 12].

The pioneering customization of array packages was reported in 2001, where a pin grid array package and a ball grid array package were designed for the application of microwave and millimeter waves [13]. Similarly, in year 2004, a dielectric chip antenna was seamlessly integrated in a ceramic ball grid array package [14]. The obtained bandwidth, gain and radiation efficiency of the integrated antenna suggested that the antenna-package codesign introduced negligible effects to the antenna performance. In the context of ion trap applications, in year 2013, a conventional ceramic leadless chip carrier (LCC) was cut using water-jet-laser to create an orifice for vertically optical access and vacuum conductivity [11]. Besides, in the work reported by Sandia National Laboratories in 2020, a bowtie shape CPGA was customized to preserve the optical access to the trap isthmus region. However, no direct metal layer patterning was made onto the package and wire bonding was still heavily used [15].

In Section I, we first introduce the fundamental principles of surface ion traps. We also highlight the motivation and necessity of the trap assembly process simplification. The customized CPGA design is given in Section II. The design rules and considerations are discussed. Section III provides the electrical characterization results and analysis of the customized CPGA before and after it is bonded to the TSV integrated trap. In Section IV the ion trapping related setup and the performance of TSV trap on this customized CPGA is given in more details. The key findings and conclusions are highlighted in Section V.

II. CUSTOMIZED CPGA DESIGN

The first concern about the customized CPGA carrier is the form factor limitation. Since the trap will be directly located on a CPGA (i.e., in the absence of a smaller glass interposer), the focused Gaussian beams are more likely to collide with the CPGA surface along the propagation path (especially for those of small beam waist), when the carrier dimension is enlarged. Therefore, in the new design, the sunken cavity in conventional CPGA is removed, and the RDL is at the same height as CPGA surface (Fig. 2 (a) and (b)). In this case, the laser beam properties (i.e., wavelength λ and beam waist w_0) together with ion height (w) will determine the maximum allowable carrier dimension (z): $w^2(z) = w_0^2 \left(1 + \left(\frac{z}{z_0} \right)^2 \right)$, where z_0 ($z_0 = \frac{\pi \omega_0^2}{\lambda}$) is the Raleigh length. Note w is the sum of height from trapped ion to surface electrode (~ 76 μm) and height from surface electrode to CPGA surface (~ 125 μm).

In our ion trapping experiment, five lasers with different wavelengths and beam waists are used, as shown in Table I. Their specific functions are also listed accordingly. The incident directions of laser beams are marked in Fig. 2 (b). Table I shows that the maximum substrate dimension is 65.8×65.8 mm (assuming a square substrate shape), which is determined by the laser beam of 1092 nm wavelength. Based on that, the dimension of customized CPGA is set as 14×14 mm, leaving a sufficiently large threshold to prevent laser collision issues. Meanwhile, the minimum allowable beam waist with this substrate dimension (14×14 mm) is also calculated. The obtained 12 μm beam waist is compatible with general inter-ion distance when individual addressing is needed in a long ion string. Since the inter-pin distance of CPGA should be kept at 0.1 inch, the further CPGA size reduction can only be achieved by sacrificing the pin number of CPGA backside.

The RDL on CPGA has a similar geometry design as the ion trap electrodes (Fig. 2 (c)). 12 metal pads are specifically defined to locate microbumps, building connections with corresponding surface electrodes on the top. Each pad has a small tail, for the internal connection to the routing circuit inside the CPGA, and finally to the pin at CPGA backside. This tail can also be used for

wire bonding connections if needed. In total, 25 pins (5×5 pin array) are built, enabling a fan-out circuitry for up to 25 RDL pads (ignoring the possible signal multiplex for DC electrodes). In the application of current TSV trap, 9 of 25 CPGA pins are respectively connected to 9 of 12 RDL pads. It should be noted that the remaining 3 RDL pads are kept floating (i.e., not connected with pin, C-DC-1, RF1-2 and RF2-2 in Fig. 2 (c)). This is because the signal feedthrough for the central three electrodes from one end is sufficient. In addition, two CPGA pins are reserved for the surface grounding plane connections. The unoccupied 14 pins are floating.

To locate the microbumps with a diameter of $30 \mu\text{m}$, the width of the RDL pads for the central three electrodes is set as $80/50/80 \mu\text{m}$. The gap width in between is $50 \mu\text{m}$. These dimensions are close to the fabrication limits offered by Kyocera. The alignment markers on customized CPGA (for subsequent trap-to-CPGA bonding process) are also simplified to hollow squares with a diameter of $150 \mu\text{m}$ (insight of Fig. 2 (b)). These markers can be matched with those on the backside of the TSV trap.

We illustrate the fundamental fabrication steps of a customized CPGA, and more details can be found in [10]. First, the ceramic green sheet is formed by casting the ceramic slurry (A440, Kyocera). After cut into square shape, it is mechanically punched to create vias. The vias are subsequently filled by tungsten paste. Next, the routing circuit is patterned using screen printing. Following that, multiple green sheets are stacked, laminated, and shaped. The chip carriers are then co-fired to form the electrical and mechanical integrity. After inserting CPGA pins (Fe-Ni-Co alloy), the last step is the electroplating process of $\sim 2 \mu\text{m}$ Ni and $\sim 2 \mu\text{m}$ Au, in which the patterned RDL pads and the grounding plane are defined. The measured root-mean-square roughness (R_q) of RDL is $\sim 80 \text{ nm}$. We note that the CPGA fabrication is provided by Kyocera.

III. ELECTRICAL CHARACTERIZATION AND DISCUSSION

A. Electrical Tests before Trap Bonding

The following tests are carried out on a bare customized CPGA, before its bonding to the TSV trap.

First, the internal connection between each RDL pad and its respective CPGA pin is examined and no open circuit is found. Subsequently, to evaluate the insulation resistance between two arbitrary RDL pads, an I - V test is performed using a probe station. Two probes (one signal, one ground) are used to connect with the RDL pads. A voltage sweep from 0 to 10 V with a step of 0.2 V is applied and the leakage current in between is measured. As shown in Fig. 3, the resistance varies from 2 to $7 \times 10^{12} \Omega$, due to the size and distance difference of both RDL pad and internal routing circuit. We note that the resistances of the floating pads (C-DC-1, RF1-2 and RF2-2) are the highest. The averaged resistance value of RDL pad ($4.5 \times 10^{12} \text{ ohm}$) is three orders of magnitude higher than that of TSV trap (in the range of 10^9 ohm). This indicates that the final resistance between electrodes after bonding will be determined by the TSV trap, and that the customized CPGA itself has excellent insulation property.

The capacitance between RF and central DC RDL pads of the customized CPGA is also measured. One probe is contacted with a RF pad (RF1 or RF2) and signal is applied, while the other probe is contacted with central DC pad (C-DC) and set as ground (see Fig. 2 (c)). The applied DC voltage dual sweep is from -5 to 5 V with a step of 0.1 V, while the AC signal has an amplitude of 30 mV and frequency of 100 KHz. The obtained capacitance of customized CPGA is benchmarked to that of previous glass interposer, before and after its wire bonding on conventional CPGA. It should be highlighted that the capacitance is from the single end of central three RDL pads. As shown in Fig. 4 (a), the customized CPGA has a capacitance of $\sim 1 \text{ pF}$, which is higher than that of the glass interposer itself ($\sim 0.4 \text{ pF}$). However, after the interposer is connected to the conventional CPGA by wire bonding, the total capacitance will rise to $\sim 0.9 \text{ pF}$. On the other hand, the obtained high capacitance of the customized CPGA is largely due to the relatively high dielectric constant of A440 alumina (9.8), though the overall signal routing path is shortened. In comparison, the dielectric constant of glass is 3.9. Besides, due to the carrier form factor constraint, the closer routing circuits inside CPGA may also increase the mutual capacitance.

B. Test after Trap Bonding

TSV trap is independently fabricated using a via-first approach with standard CMOS back end of line process. The process details are illustrated in [8, 9]. The cross-sectional SEM image Fig. 5 (a) shows the vertical connection from surface electrode to TSV and finally to backside metal layer and microbump of fabricated TSV trap. The TSV trap is then bonded to the customized CPGA using a flip-chip process. Flux is first dispensed onto the RDL pad surface, which is followed by TSV die placement. The alignment is facilitated by locating the cross markers on the TSV die backside into the hollow squares on RDL pads of CPGA (Fig. 2 (b) and Fig. 5 (c)). Next, the assembled chip is put into a reflow oven (~ 4 mins, with reflow temperature of up to $\sim 240 \text{ }^\circ\text{C}$). X-ray is used to morphologically check the alignment and bonding quality, as shown in Fig. 5 (c). An overall wire bonding-free assembly is achieved for DC and RF signal feedthrough. However, for DC electrodes, bonding wires are still used to connect with thin-film capacitors for RF pick-up filtering. Again, wire bonding end close to the trap is located on the RDL pad tail (Fig. 5 (b)). To avoid degassing issue in the UHV chamber during ion trapping operations, no underfill material is introduced between TSV die and CPGA. As the TSV die is bonded to the RDL pad in the absence of specifically defined under bump metallization (UBM) (see

Fig. 5 (c)), it is necessary to evaluate the resultant bonding strength. A shear test is performed in accordance with MIL-STD-883E method 2019.5 [16]. It is found that the fracture is at the interface of backside metal layer and microbump of TSV die, instead of the interface of microbump and CPGA RDL. The averaged maximum shear force for a single bump is ~ 0.07 N, corresponding to a shear stress of ~ 100 MPa (given the diameter of microbump is $30 \mu\text{m}$). This is sufficiently high and indicates that a robust bonding is achieved [17].

During ion trapping tests, the trap is connected to an external resonant transformer to step up the RF voltage. A resistor-inductor-capacitor (RLC) circuit is formed: the resistor and inductor come from the transformer, whereas the capacitor (between RF electrodes and ground) is largely determined by the packaged trap itself. Therefore, we first evaluate the capacitance of packaged trap after the bonding process, followed by a resonator test emulating the actual setup during ion trap operation.

The capacitance is between one single RF electrode and the ground of CPGA is first measured. The measurement setup is similar to that described in Section III. As shown in Fig. 4 (b), the obtained a trap capacitance on the customized CPGA of ~ 10.8 pF, which is ~ 0.3 pF higher than that of the trap in a conventional CPGA with glass interposer. Next, the two RF electrodes are shortened by a wire bonding. The total RF-GND capacitance is measured again, and a difference of ~ 1 pF is observed.

Next, the packaged traps are respectively connected to a homemade resonator box composed of inductors and resistors. A -10 dBm RF signal sweeping from 10 to 100 MHz from a RF generator is applied to the resonator. A spectrum analyzer is used to monitor the output signal from the ion trap. The overlapped resonance curves of different traps are shown in Fig. 6, indicating that TSV trap on customized CPGA and conventional CPGA with glass interposer have similar RF performance. Both have a Q factor of ~ 30 . The small deviation of resonance frequency (51.9 and 52.3 MHz) is also consistent with the RF-GND capacitance difference mentioned above ($f = \frac{1}{2\pi\sqrt{LC}}$).

A separate S-parameter test is also performed. Two 3-pin probes are placed at the two ends of the central RF-DC-RF electrodes, establishing a two-port circuit network. Note this test is also performed on traps that are packaged into different CPGA (i.e., ready for ion trapping test). The RF signal sweep is from 10 to 200 MHz. As shown in Fig. 7, at a lower frequency range (< 50 MHz), the traps on different CPGA have a similar insertion loss (S_{21}) and reflection loss (S_{11}). However, when the frequency is higher than 100 MHz, the trap performance on the customized CPGA becomes more favorable. Its smooth curves also suggest that a good stability of the components is achieved across the entire frequency range.

Although both traps have similar RF losses, the high thermal conductivity ($14 \text{ W}/(\text{m}\cdot\text{K})$) of ceramic material (alumina A440) is able to facilitate high efficiency heat dissipation, maintaining the trap temperature in an acceptable range. Based on finite element modelling results, it is found that at a given power loss of 0.1 W, the trap on customized CPGA has a temperature increase of ~ 3 K, significantly lower than that of a trap on glass interposer (> 30 K).

IV. ION TRAPPING PERFORMANCE

The trap is tested in a stainless-steel ultra-high vacuum (UHV) chamber with a set of viewports and flanges for photon detection, laser input/output, lateral imaging, pumping and electrical feedthrough. During trap operation the chamber is pumped by an ion pump (IP) and a Titanium sublimator pump (TSP) with a base pressure of 3×10^{-10} mbar. The customized-CPGA holder includes a home-made socket, machined in a Peek plate.

Adjustable DC voltages for the segmented electrodes are generated by a DAC card (Measurement Computing PCI-DAC6703), filtered by an out-of-the-chamber low-pass passive inductor-capacitor-resistor filter and then steered to CPGA socket using screened cables. RF voltage (frequency of 31.1 MHz) is supplied by a digital RF generator, amplified in a 10 W, 50 Ohms amplifier, adapted to the high impedance of the trap by a toroidal resonant transformer (step-up of 9) and steered to the socket with a coaxial cable. The maximum RF voltage amplitude at the trap is around 100 V.

An atomic beam of neutral Sr is generated by sublimation of a Sr dendrite inserted in a tungsten filament. Two-color CW photo-ionisation [18] allows us to create Sr^+ ions in the center of the trap: the loading-time for an ion is typically around 5 seconds.

The $^{88}\text{Sr}^+$ ions are Doppler-cooled addressing the $422 \text{ nm } 5^2\text{S}_{1/2} \rightarrow 5^2\text{P}_{1/2}$ transition with a free-space beam from a GaN extended-cavity laser diode. Two additional free-space lasers beams (“repumpers”) address the $1003 \text{ nm } 4^2\text{D}_{3/2} \rightarrow 5^2\text{P}_{3/2}$ and the $1033 \text{ nm } 4^2\text{D}_{5/2} \rightarrow 5^2\text{P}_{3/2}$ transition to avoid optical pumping. All the beams are coupled in single mode optical fibers and then focused at the ion position with typical spot sizes reported in table 1.

The photons scattered by the ion during the cooling process are collected by an objective (numerical aperture of 0.4), spatially filtered in a $150 \mu\text{m}$ diameter pinhole, spectrally filtered by an interference filter and detected by a photomultiplier in photon-counting mode. The overall photon collection efficiency [19] is $2.20 \pm 0.05 \times 10^{-3}$.

We observe stable trapping of ions (lifetime of the order of 30 minutes) in a range of RF voltage amplitudes between 35 and 65 V. Amplitudes exceeding 60 V result in a base pressure increase in the vacuum cell (pressure increase of 2.5×10^{-11} mbar for a RF amplitude of 75 V) probably induced by residual device heating induced by RF dissipation.

We measured the motional frequencies corresponding to trapping voltage amplitudes using a “tickle” technique coupled to a sequential fluorescence acquisition. The agreement between the measured and the calculated frequencies (according to an analytical gap-less model [20]) is within 12%, as usual in surface traps of this size. The heating rate of the trap has been characterised using the Doppler re-cooling method [21]. For this purpose we operate the trap with an axial frequency of 300 kHz and radial frequencies around 2.3 MHz. We expect the re-cooling dynamics to be dominated by the temperature of the lower frequency axial mode. Incoherent repumping allows us to operate in the two-level-atom approximation needed for the analysis of the acquired data [21]. From the analysis of several experimental sets, the heating rate of the trap is evaluated at 310 ± 60 mK/s that corresponds to 21 axial quanta per millisecond. This result corresponds to a normalized electric-field spectral noise density, $\omega_z * S_E(\omega_z)$, of 1.9×10^{-4} (V/m)², similar to what we obtained in a TSV trap with glass interposer [8].

V. DISCUSSION AND CONCLUSION

A. Further Improvement

First, to further boost the thermal dissipation capability of the package, a ceramic material with even higher thermal conductivity (e.g., aluminum nitride, 150 W/(m·K)) can be selected. Meanwhile, with current CPGA manufacturing technologies, the feature size and pitch of CPGA RDL are hard to be reduced to less than 50 μ m. Mismatch between microbumps and CPGA RDL will be induced when TSVs/microbumps are of high density. This poses a challenge to the metal layer routing on the TSV trap backside, which bridges the via and microbump. Delicate routing shall be implemented to guarantee the precise connection between bump and RDL, without sacrificing the TSV density. In addition, the CPGA size/the backside pin number limitation considering the laser beam propagation can be fundamentally solved once silicon photonics devices are integrated on-chip allowing laser light to be locally routed and emitted [22, 23]. Therefore, a complex ion trap design with a high number of electrodes can be achieved. Finally, a flexible CPGA socket is in need, to facilitate frequent CPGA size and CPGA pin arrangement adjustments.

B. Conclusion

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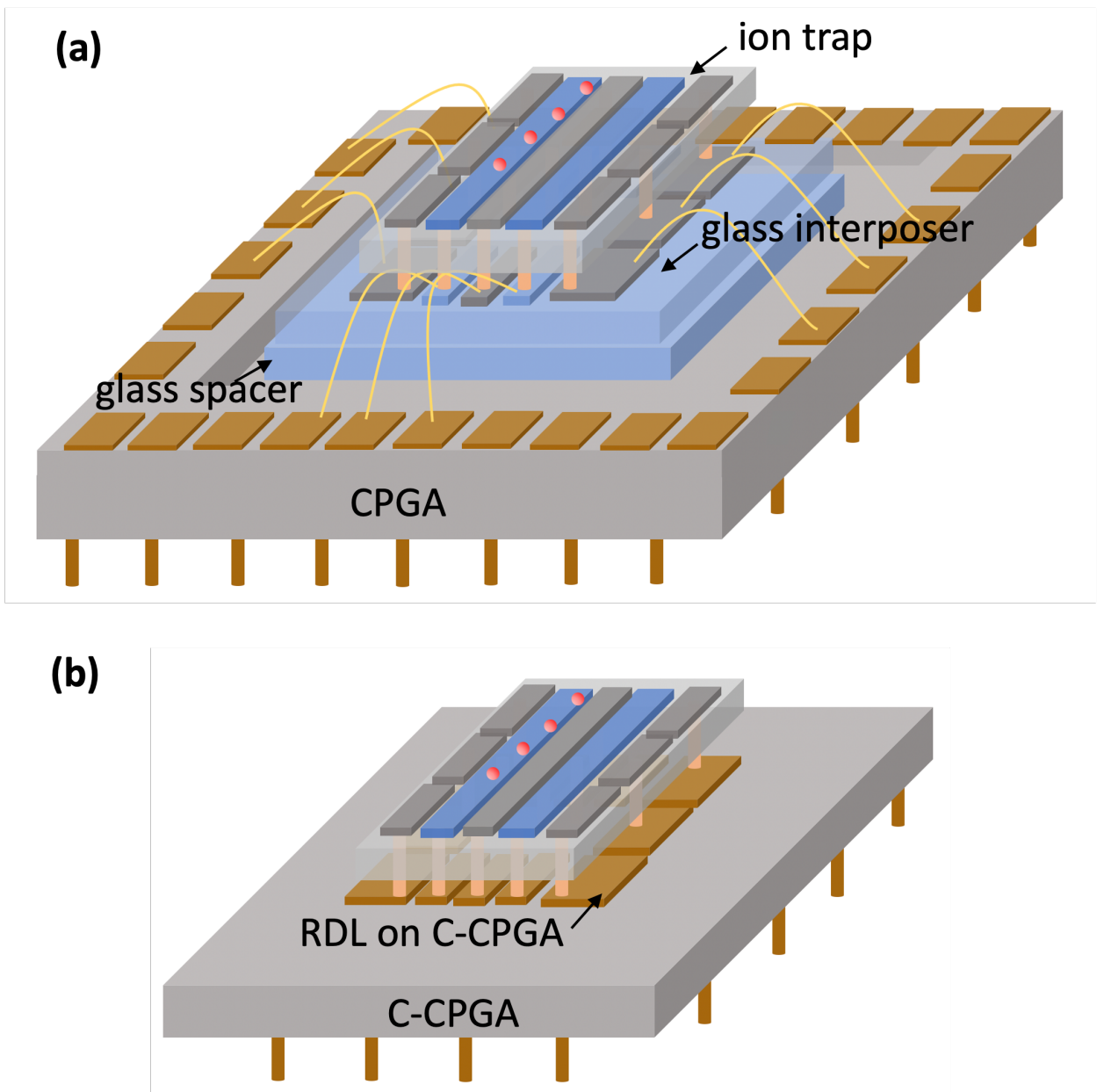


Fig. 1. The development of TSV integrated ion trap assembly method. (a) Conventional method: TSV trap + glass interposer + glass spacer + CPGA. (b) New method: TSV trap + customized CPGA with patterned RDL. Capacitors for RF filtering are not included in the schematic.

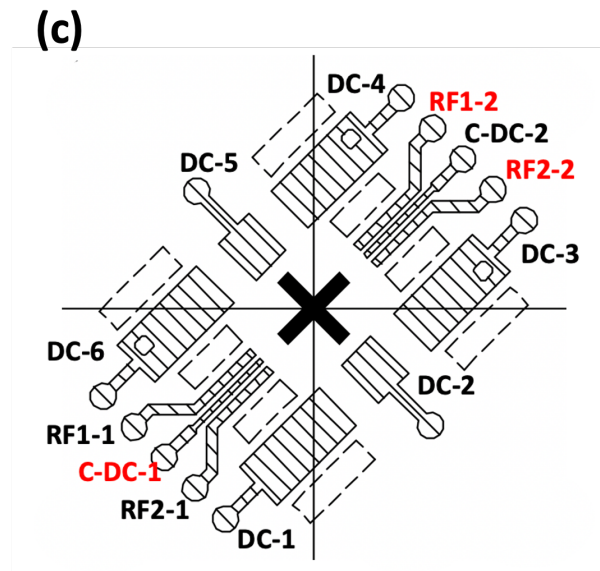
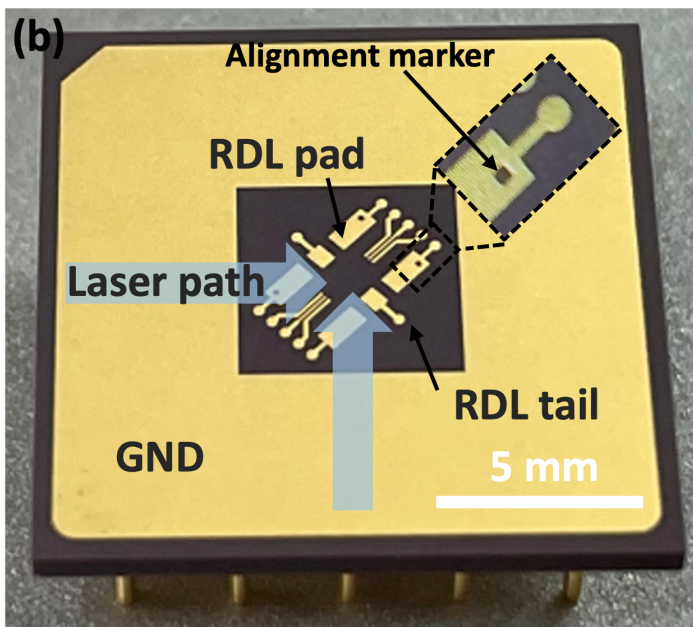
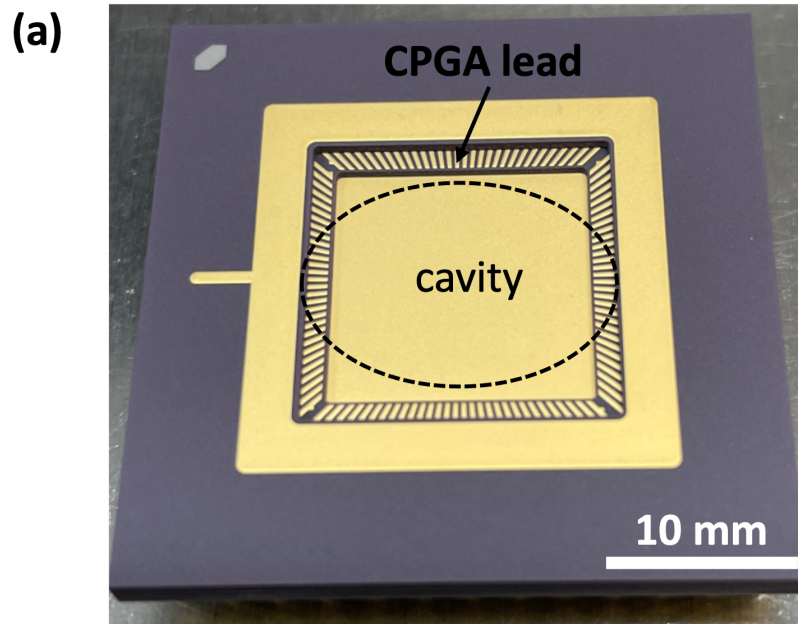


Fig. 2. (a) Conventional CPGA that has lead frame and a sunken cavity. (b) Customized CPGA where patterned RDL pads are on the substrate surface. (c) Schematic of patterned RDL pads, where functions are labelled.

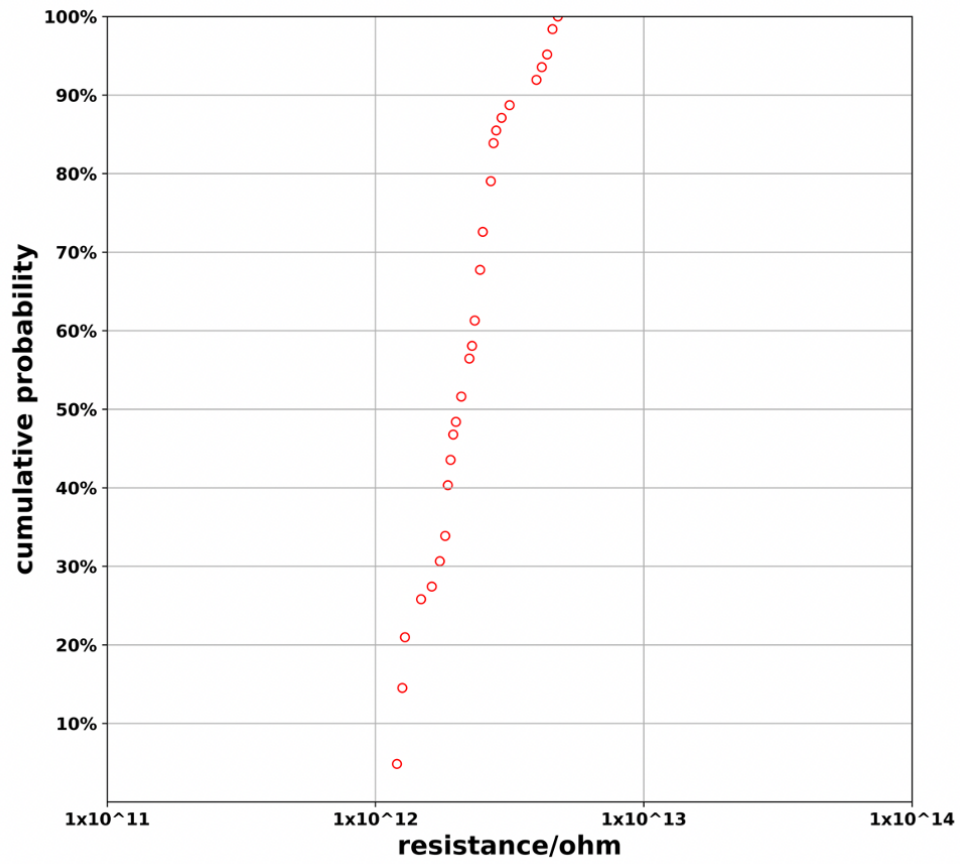


Fig. 3. Cumulative probability of measured resistance between arbitrary RDL pads of customized CPGA.

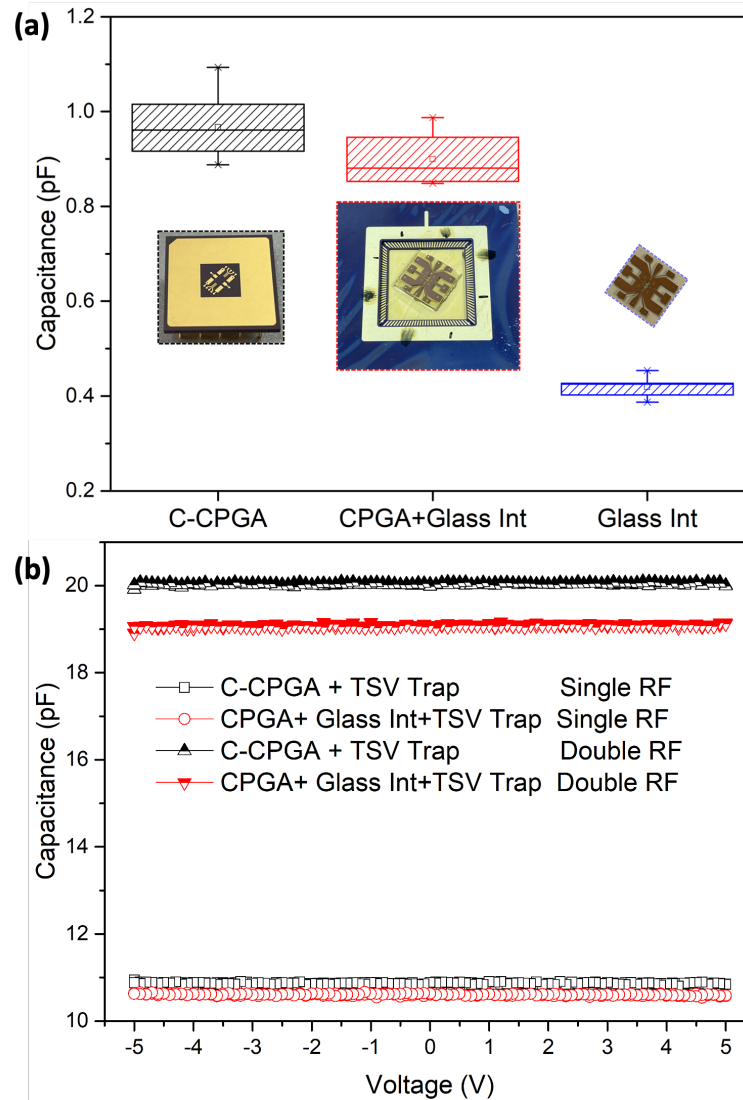


Fig. 4. (a) The RF-central DC capacitance comparison among customized CPGA, glass interposer assembled on conventional CPGA, and glass interposer only. The images of these three candidates are shown as insets. (b) RF-GND capacitance of trap on customized CPGA and trap on conventional CPGA with glass interposer.

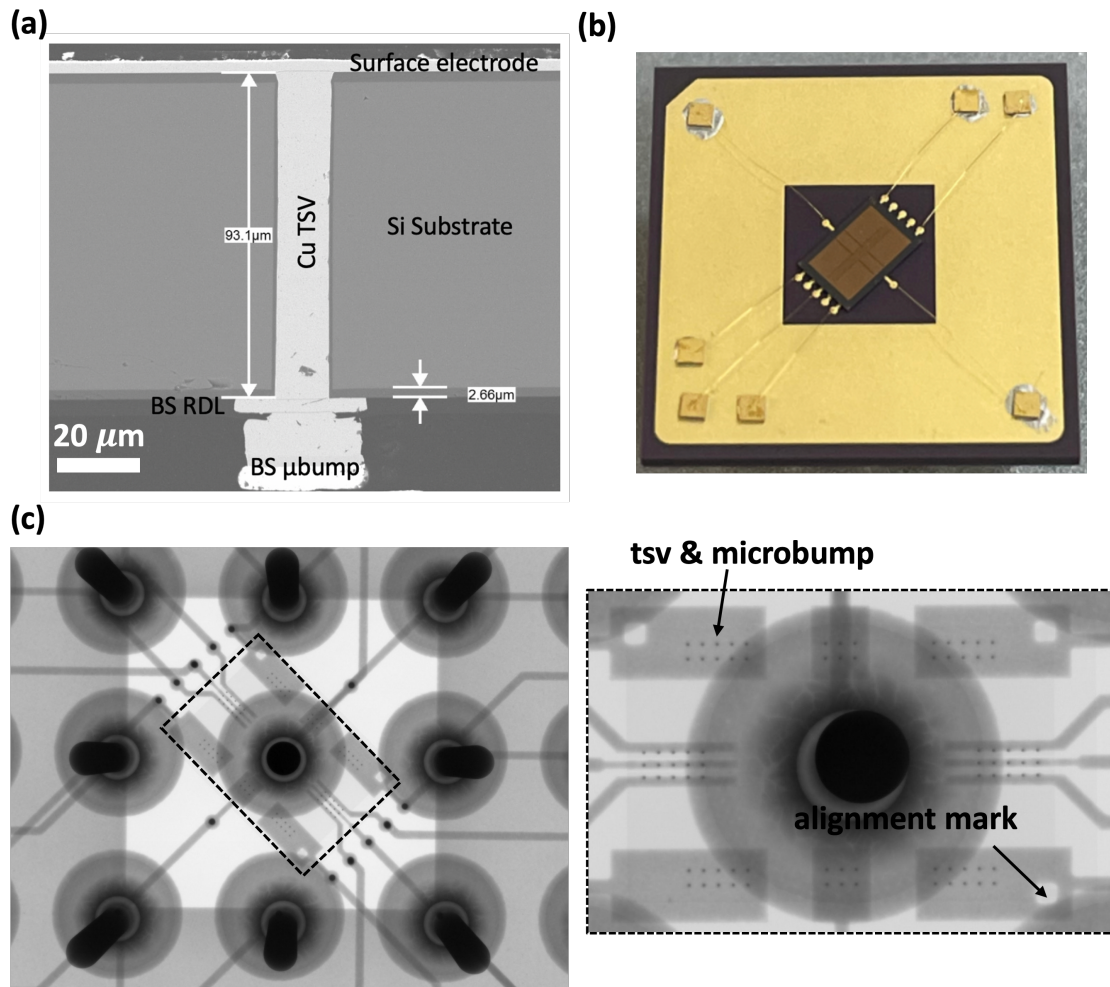


Fig. 5. (a) Cross-sectional SEM of fabricated TSV trap, before its bonding onto CPGA. (b) TSV trap bonded onto customized CPGA. (c) X-ray image of TSV trap bonded on customized CPGA (view from backside). A zoom-in X-ray image showing the connections between TSVs and RDLs is on the right.

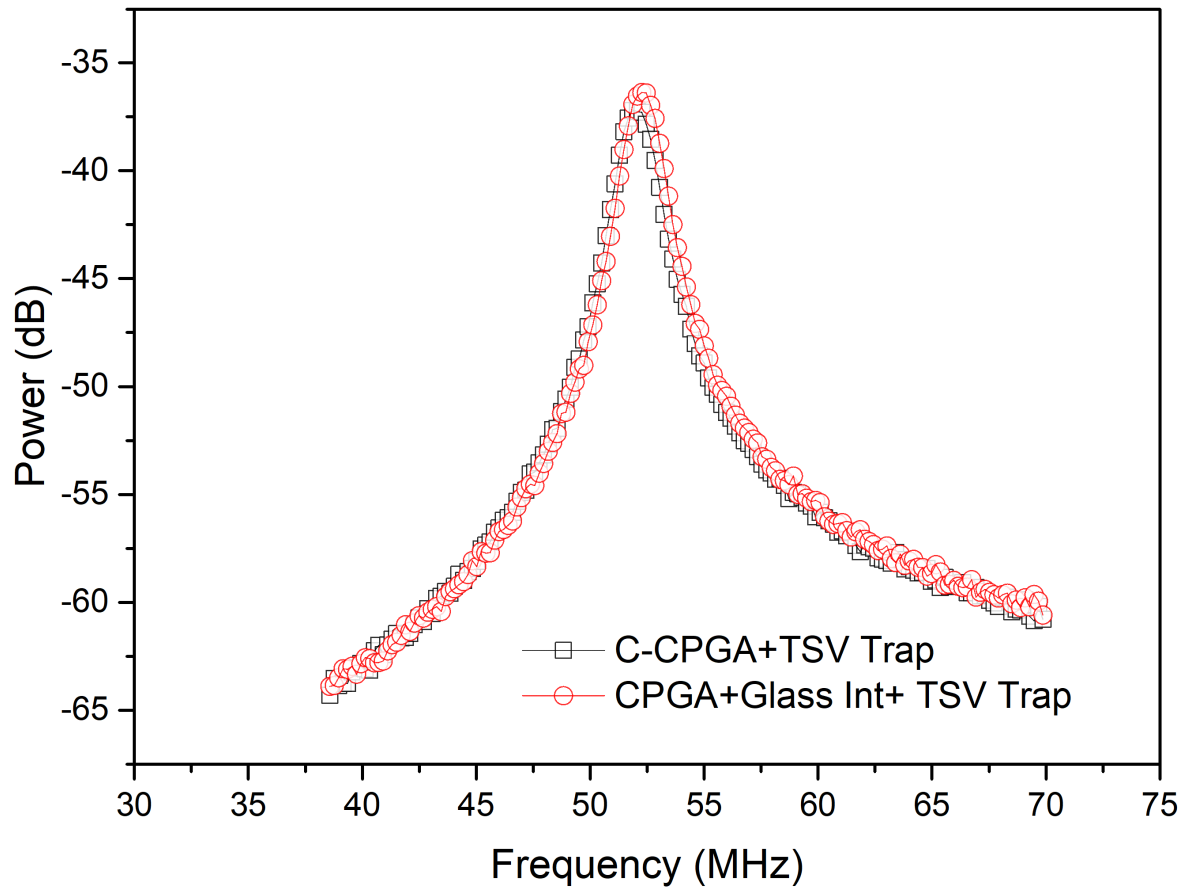


Fig. 6. The resonance curve of TSV trap on customized CPGA, with a reference curve of TSV trap with glass interposer wire bonded with conventional CPGA. The curve of TSV trap on customized CPGA has higher peak and smaller 3 dB bandwidth.

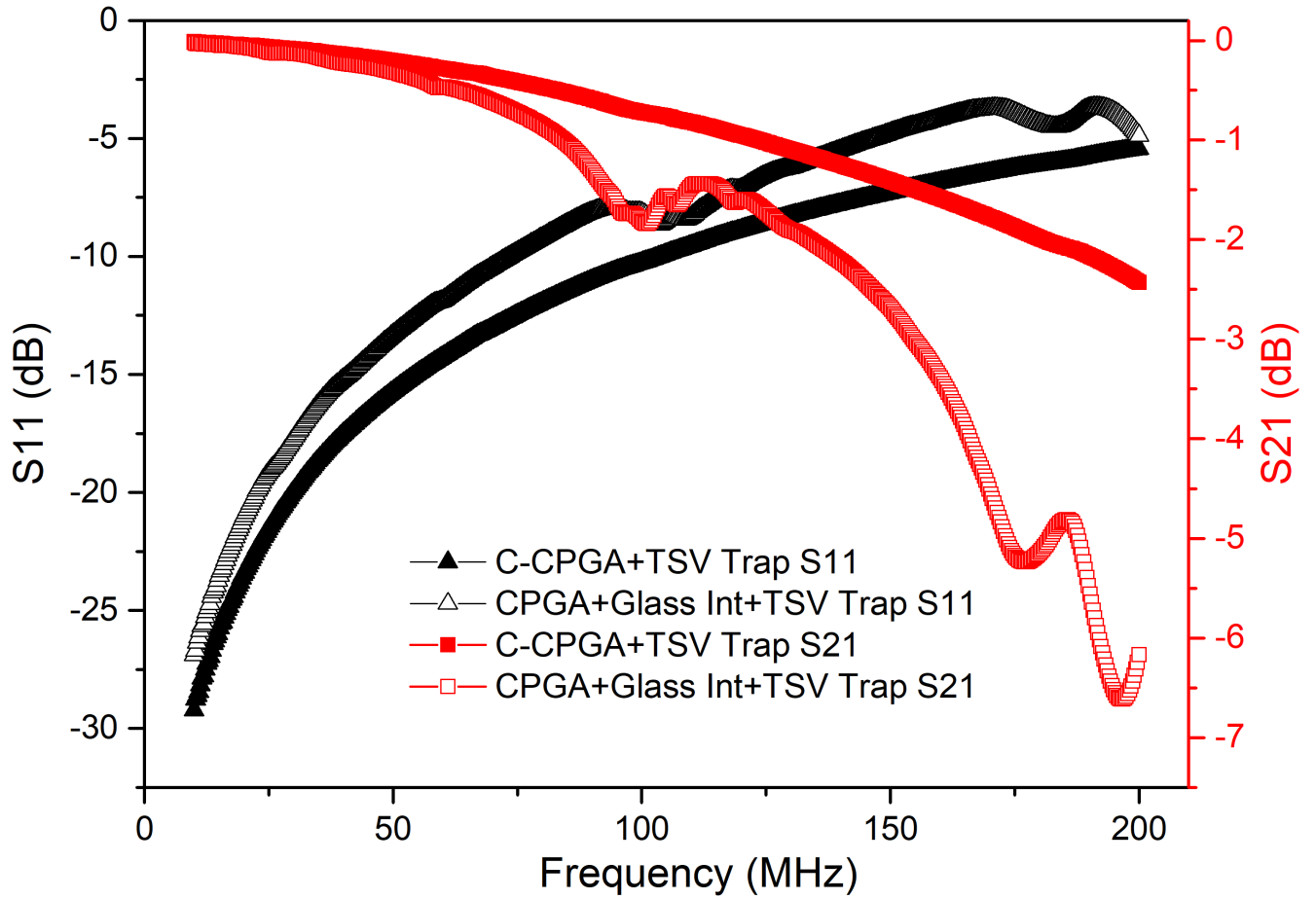


Fig. 7. The insertion loss (S21) and reflection loss (S11) comparison of TSV traps respectively packaged on customized CPGA and on conventional CPGA with glass interposer.

TABLE I
BEAM PARAMETERS AND MAXIMUM ALLOWABLE SUBSTRATE DIMENSION

Lasers Wavelength (nm)	Function	Beam Waist (μm)	Rayleigh Range (mm)	Maximum Substrate Dimension R (mm)	Minimum Beam Waist @ R=14mm (mm)
1092	Detection	60	9.1	65.8	12.2
1033	Repumper	60	9.7	69.6	11.5
1003	Repumper	60	9.9	71.7	11.2
461	Ionization	40	18.9	106.8	5.1
422	Cooling	30	16.6	88.3	4.7
405	Ionization	40	21.5	121.5	4.5