Backside Fault Localization and Defect Physical Analysis of Degraded Power HEMT p-GaN Transistors Stressed in DC and AC Switching Modes

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Abstract

This paper describes a backside approach methodology for sample preparation, fault localization and physical defect analysis on p-GaN power HEMT electrically stressed in DC voltage surge and AC switching mode. The paper will show that preparation must be adapted according to the defect position (metallurgy, dielectric layers, epitaxy, etc.) which depends on the type of stress applied. In our life-operation mode amplified electrical stress reliability study, the failure analysis will help us to reveal the weakest parts of the transistor design in relation to the type of applied stress. The failure analysis presented in this paper is composed of electrical characterization, defect localization with PEM and LIT, FIB Slice&View, TEM analysis and frontside conductive AFM after a deep HF.

Introduction

The GaN HEMT power device emerges nowadays as a promising device in high frequency and medium voltage power electronics applications to overcome silicon devices limitations allowing smaller size and higher efficiency power converters. Nevertheless, its reliability and failure modes under maximum voltage and under switching mode near or just above its maximum ratings remains unknown. The physical degradation mechanisms specific to GaN HEMT as well as the associated electrical signatures must now be established and better understood. Very few publications on this type of technology are available in the FA community despite reliability studies of power GaN HEMT were published [1-2]. The applied aging stresses types are detailed in the first part. We will demonstrate that our proposed backside sample preparation methodology must be adapted with the type of stress applied. A FA methodology for DC stress induced defects will be proposed in the second part. In the last part of this paper, we will show that this methodology must be adapted for AC stress induced defect. The backside defect localization will be performed with several techniques such as IR Lock-In Thermography (LIT), Photon Emission Microscopy (PEM) and Raman spectroscopy. The defect physical analysis will be carried out by Focused Ion Beam (FIB) Slice&View cross section, TEM analysis and frontside conductive AFM measurements after deep HF.

Electrical stresses and characterization

Four stressed devices are presented #1-3 and two unstressed will be used for comparison, both have the same part number and are commercially available 100V, 90A, 7mΩ QFN packaged p-GaN gate AlGaN/GaN HEMT (with a Si substrate). The drain voltage V_{DS} of transistor number #1 was increased linearly in DC mode until breakdown voltage (BV). A serial 1kΩ resistor is set to reduce the defect current after breakdown. The I(V) curve measured during the breakdown experiment (obtained with a curve tracer *Keysight* B1505A) is visible in figure 1a. The transistors #2 and #3 were electrically stressed on a no-load half bridge circuit under 120V at 2kHz during 35 hours on AC mode. This very low switching frequency has been chosen to avoid thermal overstress in addition to electrical stress which remains the main focus of the study. This circuit architecture amplifies the switching energies adding a cross-conduction phenomenon at turn on that lasts approximately 20 ns. It consists of a gate control fault that switch-on a transistor with the turn-on of the opposite transistor, resulting in a higher switching energy [3]. The transistor #10 was stressed like transistor #2 and #3 but at 67V and without the cross-conduction phenomenon due to a longer deadtime value (avoid to switch ON one transistor when its complementary transitor in the half bridge is completely switch OFF yet).
Characterization curves of the leakage current $I_{dss} = f(V_{DS})$ are shown in figure 1b at T_0 in blue and post stress at T_{0+35h} in orange. An abrupt current leakage at T_{0+35h} appears over 90V only, the transistor is still functional after the aging despite this current leakage change. Failure analysis was conducted in

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order to determine precisely the localization and nature of the defect induced in static and dynamic mode.

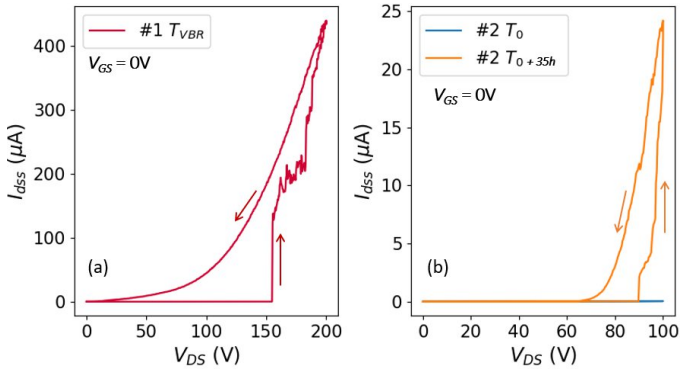

Figure 1: (a) Electrical signature of breakdown voltage of transistor #1, the curves are similar for transistor #3, a steep increase of current I_D between drain and source occurs at 155V. (b) Electrical characterization of the aged transistor #2 of the leakage current I_{dss} under V_{DS} at T_0 in blue and after 35 hours of electrical stress at T_{0+35h} in orange. A high leakage current appears only after 90V. Forward and backward sweeps are performed to take into account a possible hysteresis (arrows close to curves). #3 has similar I_{dss} curve than #2.

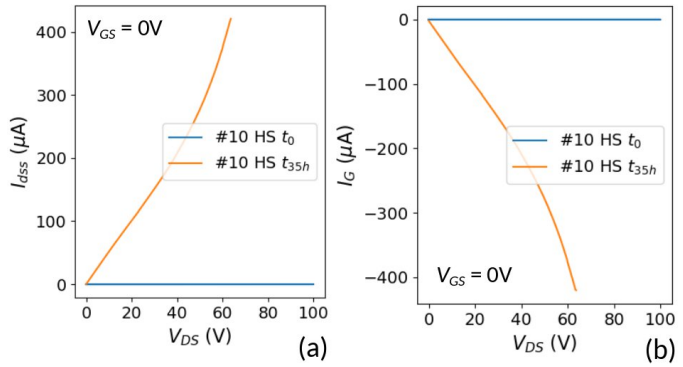

Figure 2: Drain leakage current I_{dss} = $f(V_{DS})$ at V_{GS} = 0V of transistor #10 before stress (at t_0) and after stress at t_{35h} (stress under switched voltage of 67V). (a) Drain current (b) gate current during this characterization measurement. The degradation observed is a leakage current between the drain and the gate of the transistor.

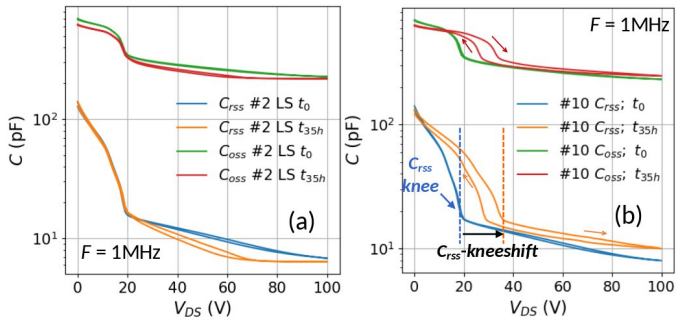

Figure 3: C_{oss} and C_{rss} = $f(V_{DS})$ capacitance measurement with Keysight B1505A before and after stress for (a) transistor #2 (for #3 the curves are similar) (120V) and (b) transistor #10 (67V). The main change for #2 and #3 is observable in the higher voltage values where the capacitance value becomes constant. For transistor #10 the capacitance knee is shifted to higher V_{DS} values and the hysteresis increases.

DC stress defect type FA methodology

The transistor technology has 3 metal levels for Drain, Source and Gate interconnections and one polysilicon gate level. The AlGaN/GaN layers epitaxy is made on a Si substrate. In this configuration, optical fault localization will be more effective through the backside of the device [4-5].

First the sample leadframe and PQFN package was mechanically removed by backside parallel lapping. The silicon substrate was thinned to a thickness of 100 µm for transistor #1. We verified that the active region of the transistor and its electrical characteristics remain unchanged which enables to perform IR Lock-In thermography correlated with PEM analysis. The PQFN configuration with through package metal vias allows the transistor polarization with the use of probe needles at the bottom side of the thinner Si substrate. Images of the chip in Fig.4 are upside-down views of the chip' GaN layers through the remaining silicon substrate. We found a perfect correlation between the LIT hot spot position and the PEM emission spot position. In the same way as for backside FIB editing approach, backside ultimate trenching of the remaining silicon layer above the hot spot / emission spot position is then performed with XeF_2 gas assisted etching on a DCG Systems optiFIB IV. FIB marking around the spot localization is also done in order to position precisely the FIB Slice &View cross section area.

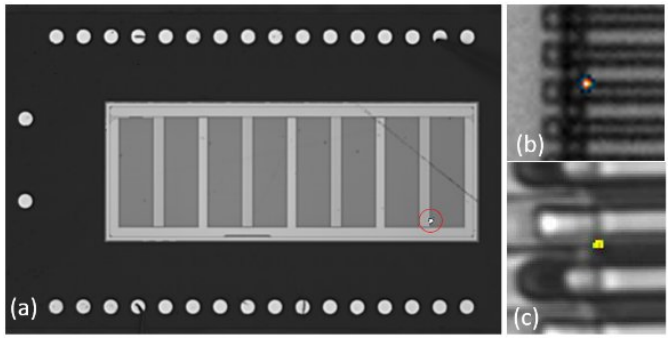

Figure 4: (a) LIT Amplitude signal of the prepared transistor #1 with a 5x magnification (lock-in frequency 25Hz), polarized at 2V with probes landed on the electrical vias. (b) LIT at 10x magnification focused on the hot spot (c) InGaAs camera PEM image with a 71x magnification focused on the emission spot (good correlation with LIT hot spot position)

The FIB Slice&View cross section is positioned 2µm beside the hot spot (figure 5a) and a small pitch (50nm) is needed (figure 5b) regarding the defect size: a filamentary breakdown defect is revealed only on one image of the Slice & View (zoom in figure 5c). As expected, it is situated in the Si_xO_y layer where the electric field is maximal *ie* between the 2D electron gas (2DEG) connected to the drain electrode and the drain-side corner of the field plate (FP) connected to the source. This defect seems to be a metal filament obtained with the localized fusion of the FP metal through Si_xO_y and probably AlGaN to reach the 2DEG. Due to its very small dimensions (a few tenths of nanometers), FIB slice&view cross section resolution is not sufficient and TEM observation is needed to analyze more precisely this defect type.

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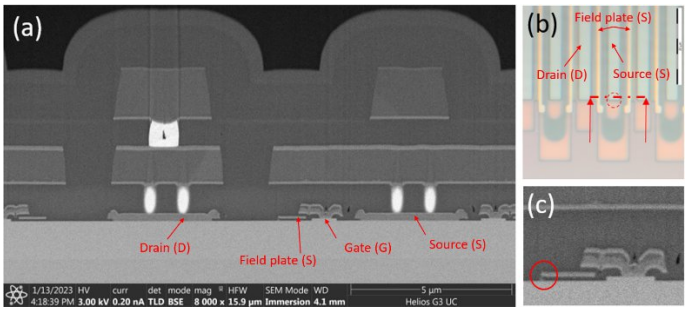

Figure 5: (a) FIB slice&view cross section in the defect zone of #1 transistor, the section axis observed is indicated by the red arrows in (b) the zoom in (c) shows at the corner of the source field plate the leakage path formed at the breakdown voltage in figure 1(a). This zone is where the electrical field is locally the most significant.

In the case of transistors #2 and #3, the defect is suspected to be in the epitaxial layers which is far more challenging for the observation and the analysis approach will be discussed in the next section.

AC switching stress defect type FA methodology:

fault isolation challenge

For the transistor #2, as the transistor is stressed in permanent switching mode on a long duration, more hotspots are visible during the LIT backside analysis (figure 6a) done after backside parallel lapping (silicon substrate was thinned to a thickness of 100 µm as for transistor #1). These hot spots are only visible for an electric polarization above 90V on a stressed transistor and corresponds to the high leakage of figure 1b. There is still a quite good correlation with PEM analysis despite some spots appears more or less intense with one technique or the other. If we apply the same backside ultimate trenching method as for transistor #1 above a selected hot spot, no more spot is detected at this position with LIT and PEM in this zone (figures 6b and 6c).

The hotspots and emission spots localization on transistor #2 are mainly near the drain edge electrode as visible in figure 7b. However some points are visible near the gate region area. The spots in the case of transistor #3 are similar to #2 (#3 will be used for other measurements that will be presented in the end of this paper). For the transistor #10 the hotspots are only located in the gate regions as it can be seen in figure 7a.

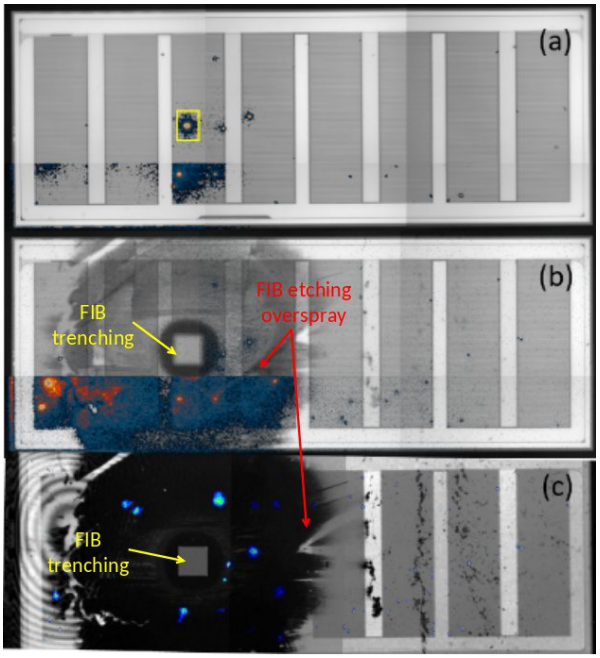

Figure 6: (a) superimposed LIT of #2 with polarization between 75V and 95V, more than 20 hot spots are visible, a brighter hot spot is visible in the yellow square (b) LIT after FIB silicon trenching locally above the brightest hot spot location that has disappeared (c) InGaAs camera PEM image after FIB silicon trenching, emission spot has also disappeared.

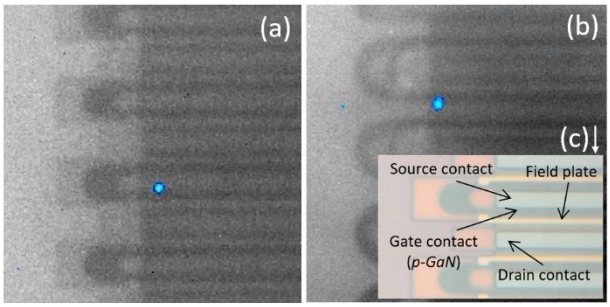

Figure 7: InGaAs camera PEM image of the emission spots. (a) Defect near the gate that might be a GD leakage current through the AlGaN barrier (#10 transistor) (b) defect near the drain metal that is expected to be a DS leakage current through the GaN layer (#2 transistor). (c) optical zoom of the metal structure seen from the backside.

Anyway the complete removal of the silicon allows the use of another analysis technique such as Raman spectroscopy as GaN/AlGaN materials are transparent at 532nm wavelength but the silicon is not. Raman spectroscopy is widely used in research laboratories for epitaxy layers and transistor unit cell characterization (structure, temperature, strains, electric field) [6-7] in a frontside approach but not yet in the field of commercial devices failure analysis and even less with a backside approach.

The variation of the principal peak of the Raman shift in figure 8d was mapped in the silicon trenching area (figure 8a, 8b) without any polarization of the transistor. A darker spot is visible over the luminescence pattern of metal lines (Drain, Source, Field Plate) exactly where the localization of the defect was revealed by LIT and PEM.

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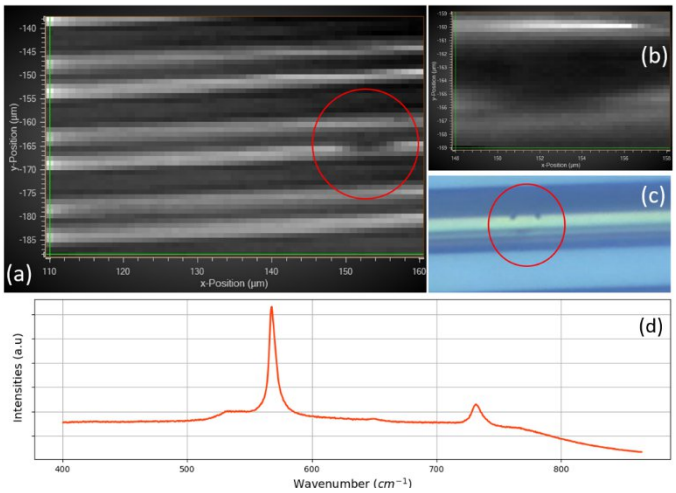

Figure 8: Raman spectroscopy using 532–nm laser beam diameter 300nm. (a) Mapping of the principal Raman peak (1µm scanning step). (b) Higher resolution mapping (300nm scanning step) focused on the defect zone. Optical view of the defect at 100x at the coordinates given by (b). (d) Long exposure Raman spectrum associated with (a,b) acquired for one pixel.

A 100x optical view is shown in figure 8c: dark spots in the GaN layer have now appeared (they were not observed just after FIB trenching). Raman spectroscopy allowed to localize the defect post silicon substrate trenching however this measurement and probably the laser power seems to have aggravated the defect. Indeed, the hotspot that had disappeared after Si trenching is visible once again with LIT and PEM conducted after Raman spectroscopy (figures 9a, 9b).

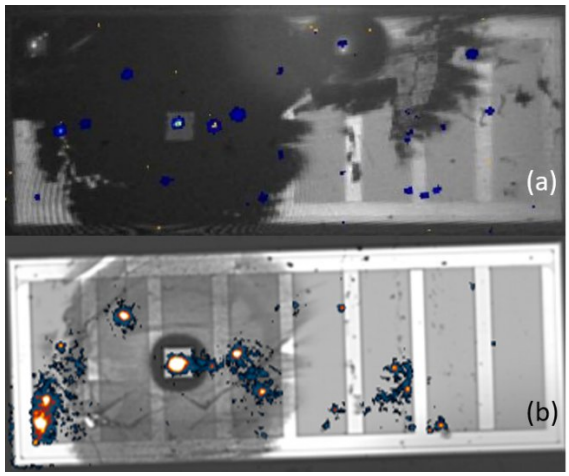

Figure 9: (a) PEM after Raman analysis, the brightest emission spot that disappeared after trenching has now signal. (b) LIT amplitude after Raman analysis, like with PEM, the hot spot reappeared after the Raman analysis.

In order to optimize the FIB trenching depth and marking parameters, other trials were done on the remaining other spots. We found that a 10µm thickness of remaining silicon in the trench preserves the defect localization with both LIT and PEM.
A FIB marking (slight etched lines) is then done in the silicon to position well the TEM lamella extraction preparation as seen on the optiFIB IV ionic image (figure 7a) and in-situ IR camera image (figure 7b).

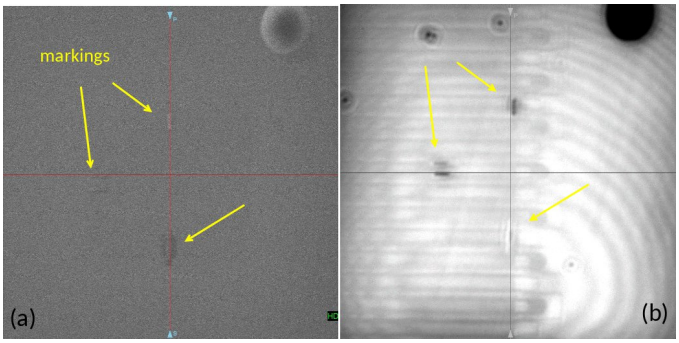

Figure 10: (a) ionic image of the trenching with 10µm of remaining silicon and marking. (b) In-situ IR camera image through the remaining silicon and view of the etched lines marking the hot spot position for TEM lamella extraction.

Localization of the layer/area that contains the defect with electrical characterization measurements.

The characterization measurements are used to know where to look for the defect once the defect region has been revealed by LIT or PEM. As the searched defects/degradations are very small (a few nm) it makes them difficult to detect during the slice&view cross section analysis or preparation of the TEM lamellae. The measurement of the capacitances and leakage currents, especially C_{rss} give information on the degraded region of the transistor. Indeed, the 2DEG depletion behavior at OFF-state depends on the metals around such as the field plates and can be followed with the C_{rss} capacitance measurement. Indeed the measurement of C_{rss} is an image of the depletion of the 2DEG under V_{DS}. As this parameter is affected by the aging, the degraded region can be determined with the change of the capacitance curve.

The change of capacitance of transistor #2 (and for #3 stressed in AC switching mode at 120V) is seen approximately between 70V and 100V Fig.3a which means the depletion stops or is complete at 70V. The zone near the drain electrode is degraded which changes the polarization of the 2DEG in this region. As the leakage current is only visible for a high enough electric field only (ie high V_{DS}) a thick isolating layer can be suspected, in this case the leakage current can be expected to be vertically through the GaN layer.

The transistor AC stressed at 67V shows a capacitance shift to higher V_{DS} voltage values (Fig.3b). The knee observed is caused by the metal field plate which depletes more easily the 2DEG to move away the electric field peak from the gate stack in order to protect it and increase gate reliability. The shift traduces the fact that the 2DEG is depleted under the field plate at higher voltage than at t_0. This shift shows that the field plate effect is less significant which shows that degradations have appeared beneath it. Now as the current leakage is between gate and drain as visible in figure 2 the layer of interest is expected to be the AlGaN barrier. This layer is supposed to electrically isolate the gate and the drain. A defect in the dielectric layer would have create an electrical contact between the 2DEG (the drain) and the source (the field plate) and the

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leakage current would have been only between drain and source.

These results are in accordance with the approximate localization of the emission spots over the metal deposition pattern observed in figure 7a. Regarding the attended very small size of the defect (a few nms), knowing exactly which part of the transistor must be inspected during the defect physical analysis (FIB slice&view and/or TEM cross-section) will increase the chances of success.

TEM lamellae preparation and observation

Now we have all information needed for further analysis, TEM lamellae are prepared to investigate the defect generated by our AC switching stress. Three lamellae are prepared, 2 from transistor #2, one corresponding to a GD current leakage defect (Fig.2 and 7a) and one for a DS current leakage defect (Fig. 1b and 7b). Indeed transistors #2 and #3 have the two current leakage locations (GD and DS) as visible in figure 7, the majority of the spots are DS leakage currents which traduces the fact that the I_{dss} measurement does not show much the GS leakage. However the measurement of the gate leakage current show an increase after stress. One lamella will be extracted from one of our unstressed device that will allow comparison of the TEM lamellae. The lamella was extracted in the same region than the DS one of transistor #2.
As the defect was expected to be under the active region (in the GaN layers of the epitaxy), the substrate silicon layer was partially removed during FIB trenching (as seen before in figure 10) to be able to observe all the substrate/epitaxy layers interfaces during TEM lamellae inspection.

The TEM lamella preparation of device #2 on a drain defect is shown in figure 11. The degraded region delimited by optiFIB markings is first covered by platinum to protect it. FIB boxes are milled on each side of marking. The unthinned lamella is lifted-out with an Omniprobe micromanipulator and attached on a TEM grid (Fig.11) where the final FIB thinning takes place to obtain a sample of thickness no greater than 100 nm (Fig. 13).

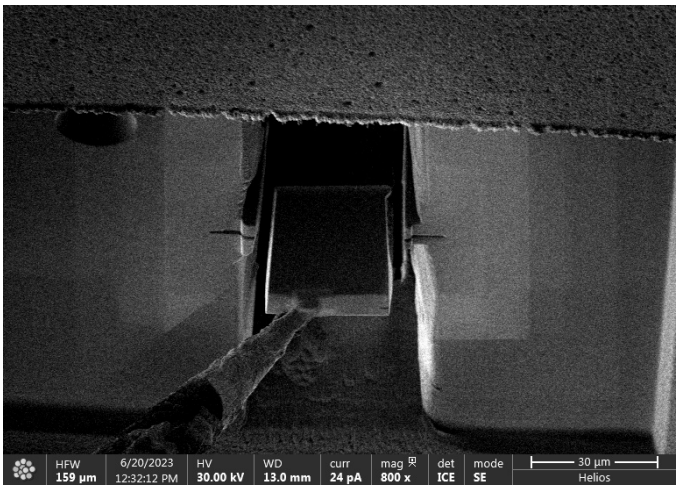

Figure 11: (a) TEM lamella extraction in the area delimited by the optiFIB markings after milling and side cuts.

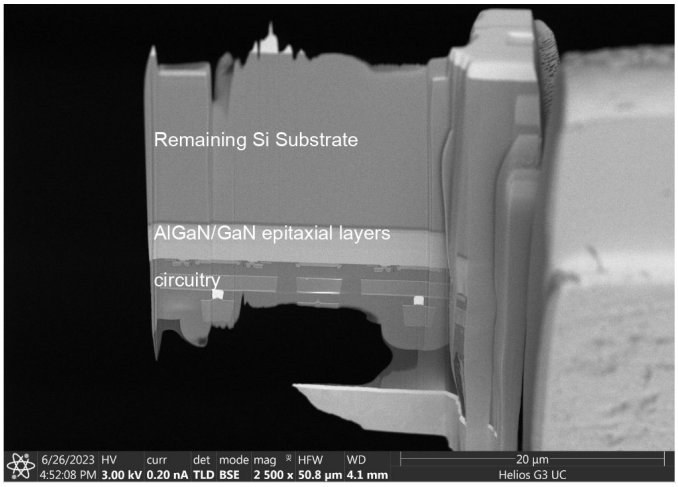

Figure 12: (a) TEM lamella thinned to 100 nm in the defect region before observation.

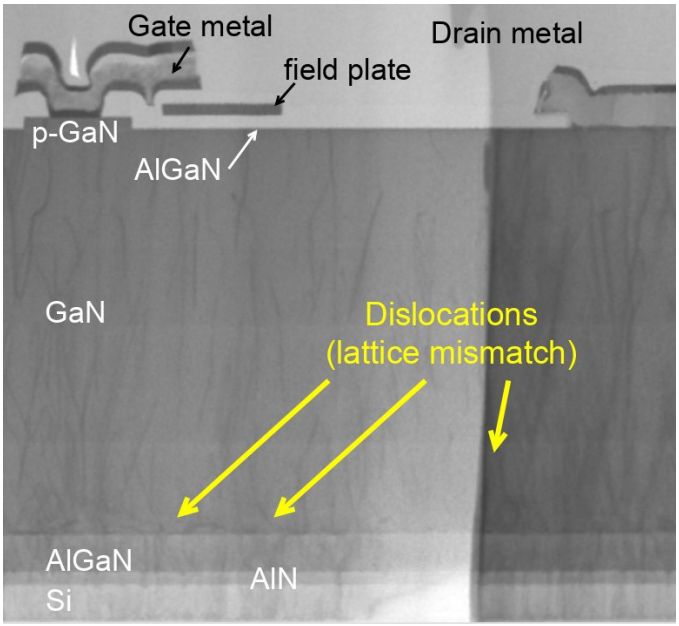

Figure 13: TEM lamella observation of the reference device in the gate-drain region. Dislocation starting from the lower part of the device can be observed. These dislocations can be generated by the lattice mismatch between Si and GaN.

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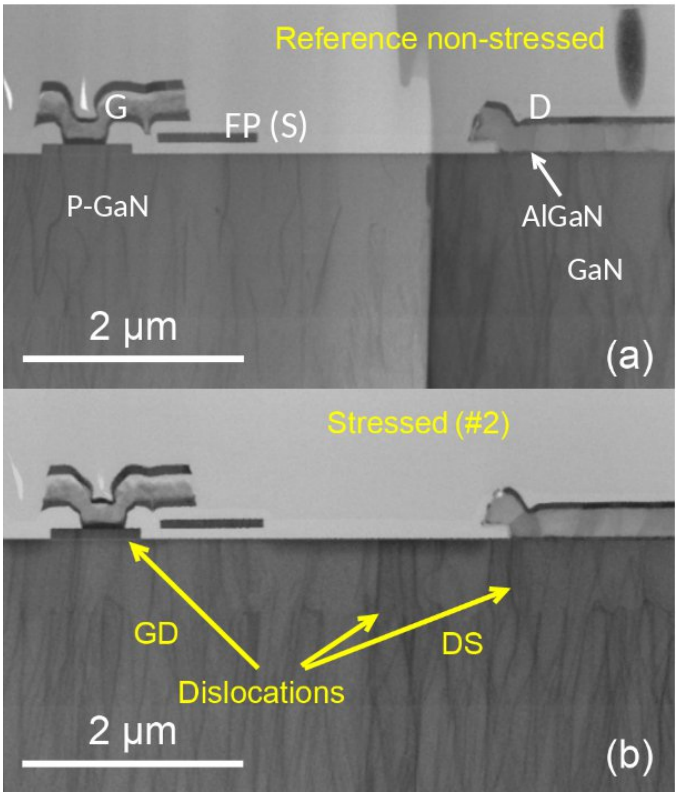

Figure 14: (a) TEM lamella observation of our reference device that was not stressed (b) TEM observation of the GD region of device two #2 (stressed in AC at 120V in cross-conduction switching mode).

The origin of the leakage current and capacitance changes may be from the same physical degradation mechanism. Our hypothesis is that the alteration of the buffer GaN layer quality might result from hot electrons generation in AC switching mode, the energy of these electrons can generate traps through lattice degradations. The dislocations may grow or evolve or new ones could appear due to the piezoelectric effect that makes a mechanical constraint between the layers (in relation to the electric field). Moreover the electric field could also be increased by the hot electrons degradation and traps generated that will change the electric field distribution. As seen on figure 14, the comparison of the TEM images in the same zone between an unstressed reference part (Fig. 14a) and stressed #2 part (Fig. 14b) clearly reveals that the dislocations density increased for the stressed transistors and more particularly in the gate drain region and below the drain metal. The drain voltage amplitude during the applied stress is expected to degrade a specific region as the 2DEG is not depleted the same way depending on the applied V_{DS} voltage. This difference will modify the position of the electric field peak in the structure and then the preferential zone of hot electrons degradations.

For the DS leakage defect case in Figure 14b, the leakage current might go through a parasitic 2DEG at one the AlGaN/GaN interface of epitaxial stack to reach the source [4] or reach a conductive GaN layer (dopped layer) connected to the source electrode. Our hypothesis is that when the silicon is entirely removed by the FIB trenching it could change the overall electrostatic polarization around the leakage path which makes it disappear locally with the same polarization parameters.

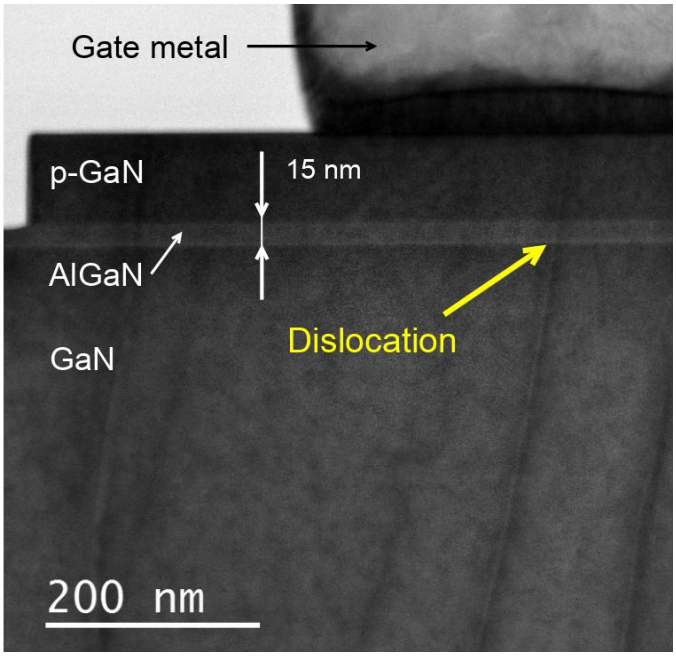

Figure 15: (a) TEM lamella observation in the region illustrated in figure 7a that corresponds with a gate drain leakage such as transistor #10. The leakage is through the AlGaN barrier through one of the dislocations observed such as the one showed by the yellow arrow in the figure.

Our hypothesis is that when V_{DS} reaches a given threshold value, some of these dislocations may become conductive. The GaN layer electric resistivity is then reduced and the leakage current reach the source vertically through the epitaxy. The presence of the leakage current in the conductive dislocations could lead to recombination mechanisms with trapped charges in the buffer (here independently from the stress) and could explain the light emission we observed with PEM at high V_{DS}.

For the GD leakage current case, as the layer (AlGaN) that contains the leakage path is rather thin (15 nm) (Fig15), the conductive path through dislocations can easily conduct the leakage current (fig 2) compared to the dislocations paths in the DS current leakage case through GaN layers (1 to 2 µm) under the drain electrode that need a higher polarization (90V, fig 1b) to be activated.

The current leakage mechanism through dislocations is not yet very well understood, besides some hypothesis are given in this paper on the possible type of dislocations and conduction mechanisms encountered in this study. These threading dislocations are expected to be threading screw dislocations through the AlGaN for GD and through the GaN for DS leakage according to [9, 10]. However the type of conductive dislocation is laborious to establish as it depends on the type of growth used which is still unknown at the moment. Several hypothesis can be made. The nature of the dislocation formed/grown can be different from the ones at t_0 that may be less conductive or only the density of dislocation could explain the difference of leakage current value observed between the unstressed and stressed device. The dislocations formed (or changed) by the stress applied might be more conductive due to maybe the presence of aluminum in the AlGaN barrier that can segregate in the threading dislocations and then form the current leakage path.

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The relaxation after stress might induce this segregation mechanism. For drain source leakage aluminum could segregate too in the threading dislocations. Besides the presence of doping materials such as carbon in the lower part of the GaN layer (but also impurities) could also play a role in the conduction mechanism. As the isolating electric distance in this layer is more important, a sufficient electric polarization is needed to activate the leakage path even if the type of dislocation is similar. We still have to determine if the leakage path is composed of a single dislocation or a group of them in the same location. The nature of the dislocation that create the leakage current path has to be determined.

TEM lamellae alone are not entirely adapted for degraded GaN analysis, more measurements are needed to characterize the conductivity of threading dislocations and their types using AFM in electrical mode / Conductive-AFM [9, 10] in a frontside approach.

Electrical characterization of the dislocation conduction behavior.

In order to characterize the conduction behavior of threading dislocations, two samples were used. One unstressed reference device and one transistor #3 that underwent the same stress than transistor #2. The electric characterization curves of this late transistor are very similar than #2's (Fig.1b and Fig.3a for instance). Similarly this device was thinned by the backside to perform defect localization (PEM, LIT) and several spots were observed as with #2 in Fig. 9. The two device's threading dislocation conduction behavior will be compared with C-AFM analysis.
The comparison is made in a spot region in the case of stressed device #3.

First a deep HF (pure hydrofluoric acid etch) is performed on the two devices in order to proceed to the complete removal of oxide and metals layers on the chip frontside. This sample preparation method is commonly used for microelectronics silicon device to access directly to the active region on the frontside of the chip. In our case the HF acid does not have any effect on AlN/AlGaN/GaN layers [11]. After that, the p-GaN cap steps will be used as visual cues to make the conduction measurement in a degraded zone were leakage is expected and where an emission spot has been observed with PEM.

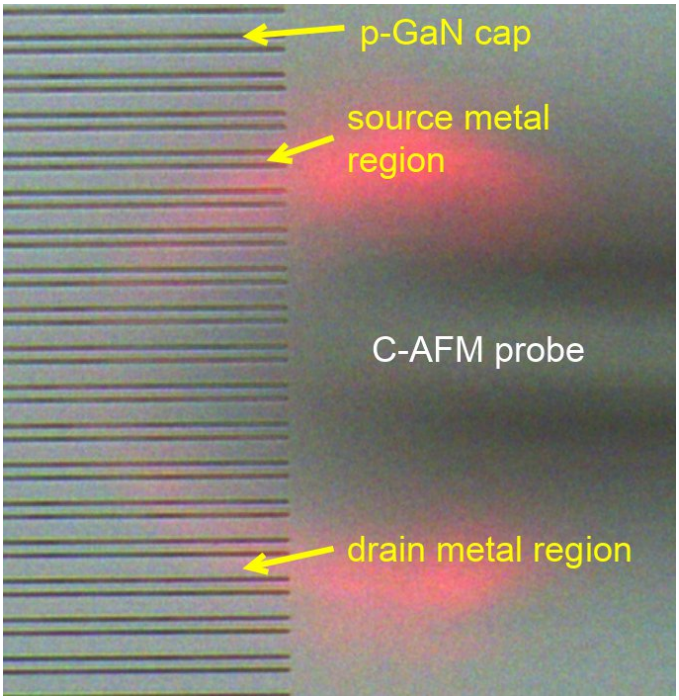

Figure 16: Optical observation of the frontside surface after deep HF, the double lines patterns observed are p-GaN caps, the rest of the observed surface is AlGaN except in the previous source and drain metals the two p-GaN caps and location (see figure 7c and 17) where the surface is the GaN layer.

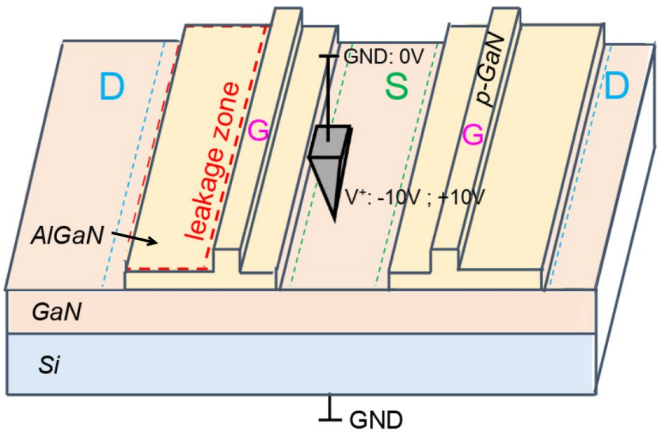

Figure 17: Setup of conductive AFM experiment performed. The probe is electrically polarized between -10V and +10V. The blue squares are the previous drain metal region and the green ones are the previous source metal regions.

The use of AFM in electric mode will allow to polarize a few dislocations on the two devices to evaluate if there are conductive or not. The leakage current goes through the AlGaN barrier and then reaches laterally the source electrode through the 2DEG. The AFM will point the zone near the p-GaN cap to measure the conduction. The zone of interest is between gate and drain previous location which is the expected current leakage zone and the most degraded region for the applied stress (see the red square in figure 17 and 18). The observed dislocations seem to be in both AlGaN and GaN layer.

A 10–µm square spot area is scanned to characterize the conduction behavior under an electric polarization up to 10V (limited by Conductive mode of the *Bruker Dimension Icon XR*

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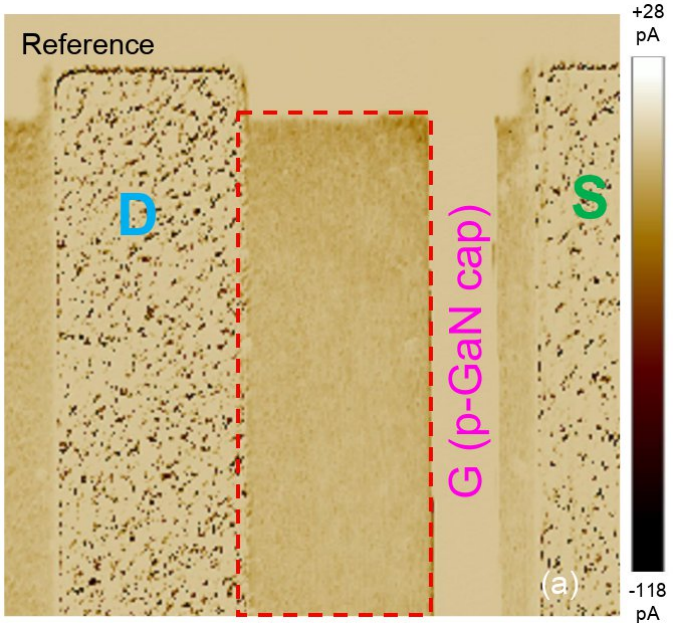
AFM used here). The same measurement is done on the reference device to allow comparison. Only the measured negative currents are considered due to the equivalent Schottky diode contact made by the metal conductive AFM probe on the scanned semiconductor.
The comparison of the leakage current paths observed is visible in figure 18a,b.

The metal regions (GaN surface) are more conductive due to the surface quality and the fact that there is not the AlGaN layer to isolate the 2DEG compared to the region of interest. The higher roughness probably also affects the measurement in electrical mode.
The conductive AFM experiment is not clearly suitable for this study and this type of device regarding the small current measured (pA) and the small polarization that can be applied compared to the threshold voltage value of the leakage degradation of figure 1b (near 90V). The results obtained in [9, 10] are for experimental epitaxial structures and not a commercial device such as ours.

However even if the comparison is hard, an overall comparison of the current leakage mappings (in all scan directions) shows some difference that might be the result of the stress. A first observation is the comparison for a same device of the leakage current in the zone of interest and in the zone between the p-GaN and the source metal (GS region). For the unstressed device the leakage current is very similar in the two regions. Yet for device #3 the zone delimited by the red lines in figure 18b seems to be more conductive than the GS region (not particularly stressed as the 2DEG always lies in this region which reduce locally hot electron effects and the electric field value). Moreover the leakage current for the stressed device (#3) is less uniformly spread over the interest region like the reference device. Indeed the leakage is higher in many precise locations that form black dots in the C-AFM scan of figure 18b. Some of these dots could be the leakage current through the threading dislocations observed in the TEM lamellae.



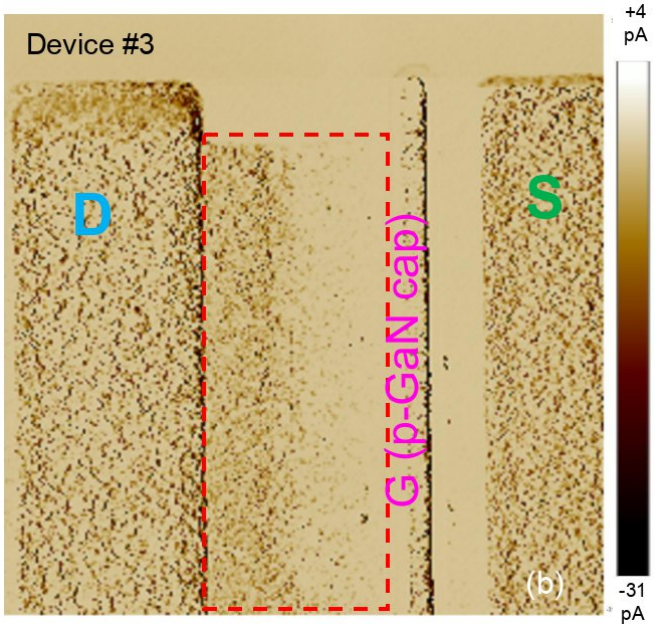


Figure 18: Current leakage mapping obtained with conductive AFM, the black dots are the current leakage paths. The zones were the metal contacts were previously are always more conductive due to their proximity with the 2DEG that facilitates surface leakage currents.

A chemical revelation with pure phosphoric acid could reveal the nature and quantity of the dislocation formed during the stress compared to the reference device as in [10].

In both stress cases, only a degradation is observed and the transistor is still functional despite functioning in a degraded mode. The functional state of the devices make the FA analysis all the more difficult. Our hypothesis is that a complete failure such as a transistor breakdown could be expected to be through the same conductive threading dislocations that could induce, in real application, percolation paths through the respective GaN (DS leakage current case) or AlGaN (GS leakage current case) isolating layers. The experiment will be done on some of the stressed devices (already degraded parts like #2 and #3) in a future experiment to validate this late hypothesis on the failure mode that could follow the degradation mode presented in this paper. The analysis of this degradation gives the ignition of the failure mode which is very important to understand the full degradation/failure mode of the device. This observed degradation would have been very hard to understand as the root cause of a bigger defect in a hardly damaged device.

Conclusions

In this paper, a failure analysis methodology with a backside approach is proposed and applied for commercial PQFN p-GaN HEMT DC and AC switching stress induced defect types. The conducted analysis shows that these physical induced defects can be very tricky to isolate (filamentary like breakdown in DC stress). Backside ultimate FIB trenching of silicon substrate above LIT hot spots / PEM emission spots can be a very effective way to perform the finest defect physical analysis (slice&view/TEM cross view), but it must be specifically adapted depending on the type of electric stress inducing different defect position depth in the transistor layers.

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This paper also demonstrates that the complete removal of silicon by FIB trenching could also enables the use of Raman Spectroscopy as a fault localization tool, but also other powerful techniques such as cathodoluminescence or photoluminescence [8] where a very close access to the direct bandgap semiconductor layers is mandatory. The defect being very small and hard to detect even with many information obtained with several complementary techniques such as electrical characterization in particular capacitance and leakage current measurements and localization like PEM, LIT and even Raman spectroscopy. For the AC stress case, TEM observation allowed to determine the nature of the leakage current for these degraded devices which seems to be an increase of dislocation density. However the high number of threading dislocation in this technology makes the interpretation of the origin of the leakage current very hard. The TEM is still limited for this type of analysis, therefore thanks to the deep HF on GaN devices, the frontside C-AFM measurements can be another complementary option to characterize the conduction behavior of dislocations and complete the TEM observation interpretation. The results obtained in this paper are in accordance with our hypothesis on the degradation due to the real-life like stress applied. The leakage current observed in characterization measurements is suspected to go through dislocation through AlGaN and GaN. These conductive dislocations might come from the mechanical constraints coming from the piezoelectric effect generated by the electric field. The application of the stress on a longer duration to the complete failure of the device will explain the complete aging process of the device from the beginning of the degradation to a not working device.

To conclude, the results obtained with this methodology will give significant information about power GaN HEMT reliability and failure modes in applications-like conditions.

References

[1] R. R. Chaudhuri, V. Joshi, S. D. Gupta and M. Shrivastava, "On the Channel Hot-Electron's Interaction With C-Doped GaN Buffer and Resultant Gate Degradation in AlGaN/GaN HEMTs," in *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 4869-4876, Oct. 2021, doi: 10.1109/TED.2021.3102469.

[2] M. Meneghini *et al*., "Reliability and failure analysis in power GaN-HEMTs: An overview," *2017 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2017, pp. 3B-2.1-3B-2.8, doi: 10.1109/IRPS.2017.7936282.

[3] N. Perera *et al*, "Hard-Switching Losses in Power FETs: The Role of Output Capacitance" in *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 7604-7616, July 2022, doi: 10.1109/TPEL.2021.3130831.

[4] T. Colpaert *et al*, "Fast and Effective Sample Preparation Technique for Backside Fault Isolation on GaN packaged devices" ISTFA2021 doi: 10.31399/asm.cp.istfa2021p079

[5] T. Colpaert *et al*, "A Novel Sample Preparation Method for Frontside Inspection of GaN devices after Backside Analysis" ISTFA 2021 doi: 10.31399/asm.cp.istfa2021p079

[6] Lenshin, A *et al* A. MicroRaman Study of Nanostructured Ultra-Thin AlGaN/GaN Thin Films Grown on Hybrid Compliant SiC/Por-Si Substrates. *Coatings* 2022, *12*, 626. https://doi.org/10.3390/coatings12050626

[7] Dolmanan, Surani Bin, K. B. Lee, L. Yuan, Susai Lawrence Selvaraj and Sudhiranjan Tripathy. "Tripathy Raman Scattering and PL Studies on AlGaN / GaN HEMT Layers on 200 mm Si (111) A." (2012).

[8] Monachon, C et al, Failure Analysis and Defect Inspection of Electronic Devices by High Resolution Cathodolumine scence- ISTFA 2017

[9] Sven Besendörfer et al, The impact of dislocations on AlGaN/GaN Schottky diodes and on gate failure of high electron mobility transistors, scientific reports (2020)10:17252, https://doi.org/10.1038/s41598-020-73977-2.

[10] Sven Besendörfer et al, Statistical of dislocation induced leakage current paths in AlGaN/GaN HEMT structures on Si and the impact of growth conditions, Applied Physics Express 15, 095502 (2022), https://doi.org/10.35848/1882-0786/ac8639

[11] D. Zhuang, J.H. Edgar, Wet etching of GaN, AlN and SiC: a review, Materials Science and Engineering R 48 (2005) 1-46, doi:10.1016/j.mser.2004.11.002

Postprint Accepted Author Manuscript : https://hal.science / https://doi.org/10.31399/asm.cp.istfa2023p0491