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Extracting Edge Conduction around Threshold in mesa-isolated SOI MOSFETs

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1. Abstract

This work proposes a methodology to decompose the center and edge current contributions around threshold in mesa-isolated SOI MOSFETs using 3D TCAD simulations. Applied to pMOS measurements, it reveals that the subthreshold regime is driven by the active edge, whatever the device width. It also explains why the threshold voltage modulation by the back-gate bias depends on the device width, as well as why these effects are worse for high channel doping values.

2. Introduction

3D sequential integration (3DSI) consists in vertically stacking active device layers, in a successional manner [1]. For example, mesa-isolated stackable 2.5V Silicon-On-Insulator (SOI) devices used for imager applications were demonstrated in [2]. The mesa isolation process is an easy and cost-friendly solution compared to low temperature Shallow Trench Isolation STI. An unusual transfer characteristic has been already observed in LOCAL Oxidation of Silicon (LOCOS) SOI MOSFETs [3], and on mesa-isolated SOI MOSFETs with five terminals, for which the corner threshold voltage was predicted using a model that uses the body potential value [4]. The specific behavior of these devices was explained in [5] by the irregular shape of the corners, the gate oxide thickness variation and the formation of a sharp beak at the edges, due to the accelerated corner oxide growth. A similar study done on Tri-Gate (TG) MOSFETs demonstrated that the low corner threshold voltage could be eliminated by using an undoped body [6]. In this work, the mesa impact on the subthreshold regime conduction in four terminals SOI MOSFETs is studied using an original method that isolates the active region's edge and center contributions. The dependence of those effects on the channel doping and on back-gate bias is investigated as well.

3. Device under test & Observations

The SOI p-MOSFET configuration was defined such as to fulfill the requirements for imager applications [2]: relatively high operating voltage ($V_{dd} = 2.5$ V), SiO_2 -polysilicon gate stack, 23 nm silicon film thickness (T_{Si}), 25 nm buried oxide thickness (T_{BOX}), 6 nm SiO_2 gate oxide and 250 nm nominal gate length (L_g). A TEM scan image is shown in **Figure 1.a**.

Drain current versus gate voltage characteristic (I_d - V_g) at $V_d = -0.1$ V on undoped channel pMOS for various device widths (W) are presented in **Figure 1.b**. It can be observed that there is a current proportionality to the device width at each part of the curve, starting from the subthreshold regime going up to the strong inversion regime. The transconductance ($g_m = dI_d/dV_g$) derivative, dg_m/dV_g , is known to exhibit a local maximum around a MOSFET's threshold voltage. This behavior is verified here, because as shown in **Figure 1.c**, dg_m/dV_g shows one clear hump meaning that there is only one channel conduction.

However, a different behavior is observed for the I_d - V_g of the p-MOSFET with doped channel (around 8.10^{17} at/cm³) in linear regime, which was also measured for various device widths (W). The corresponding curves are presented in **Figure 1.d**. Contrary to the undoped channel device, we find the current proportionality to the width only in the strong inversion region, nevertheless the subthreshold regime is the same for all device widths. In fact, a knee appears for the wide channel devices, between the subthreshold and moderate inversion regions. As a result, the dg_m/dV_g plotted in **Figure 1.e**, exhibits two humps: this indicates two independent conduction at different threshold voltages, V_t , the first around $V_g = -0.5$ V and the second

around $V_g = -0.7$ V. The observed effects are more noticeable in the case of large devices. However, this is often related to parasitic channel conduction on active edge, which is more visible in narrow devices [7,8].

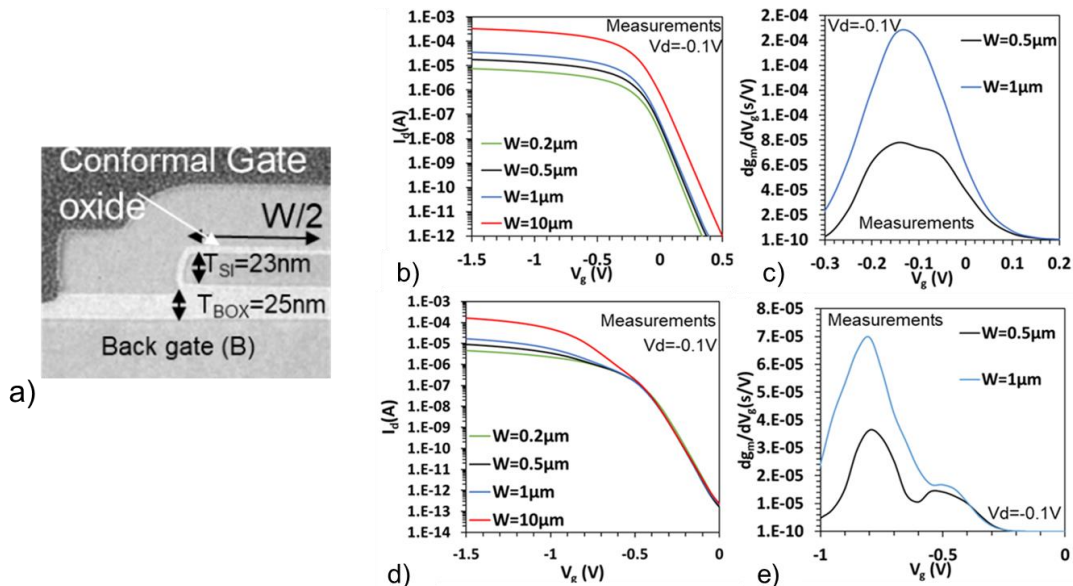


Figure 1 : a) mesa-isolated pMOS TEM cross section along W , and measured drain current and transconductance derivative (b,c) for undoped channel pMOS and doped channel pMOS (d,e), for various W and $V_d = -0.1$ V

Based on the TEM cross section, we defined a geometrical 3D TCAD structure with the same thicknesses values, a constant channel doping (8.10^{17} at/cm³), and with a gate oxide and polysilicon all around the active region (**Figure 2.a**): the structure is equivalent to a wide tri-gate MOSFET. Basic 3D TCAD simulations [9] were performed with only Poisson equation, drift-diffusion, SRH recombination and constant mobility. As our TCAD I_d - V_g and dg_m/dV_g for various device widths reproduce the trend of the experimental results concerning the behavior with varying W (**Figure 2.b & c**), it means that we can safely assume that the W -effect is only related to electrostatic (charge) and not transport effects.

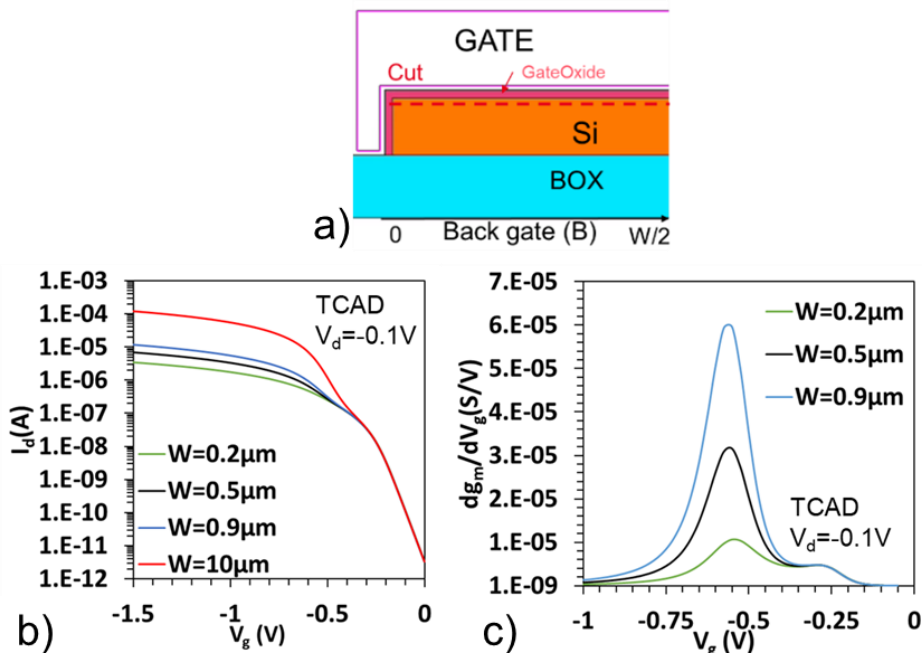


Figure 2 : a) 3D TCAD structure used to generate: b) Drain current (I_d) c) gm derivative (dg_m/dV_g) versus gate voltage (V_g) obtained by 3D TCAD pMOS simulation for various W

4. Decomposition methodology

From the 3D TCAD simulations, we have analyzed the potential in the width direction and at 1nm below the gate oxide, to understand the reason behind the early edge conduction. We extracted the potential variation, from active edge to the center in subthreshold regime ($V_g=-0.1V$) in **Figure 3.a**. For narrower devices, the potential has a “bell-shape” and its value in the center reduces with W . For $W > 0.2 \mu m$ however, this value exhibits a plateau at $\approx 0.1 \mu m$ from the edges, and across the center region of the channel.

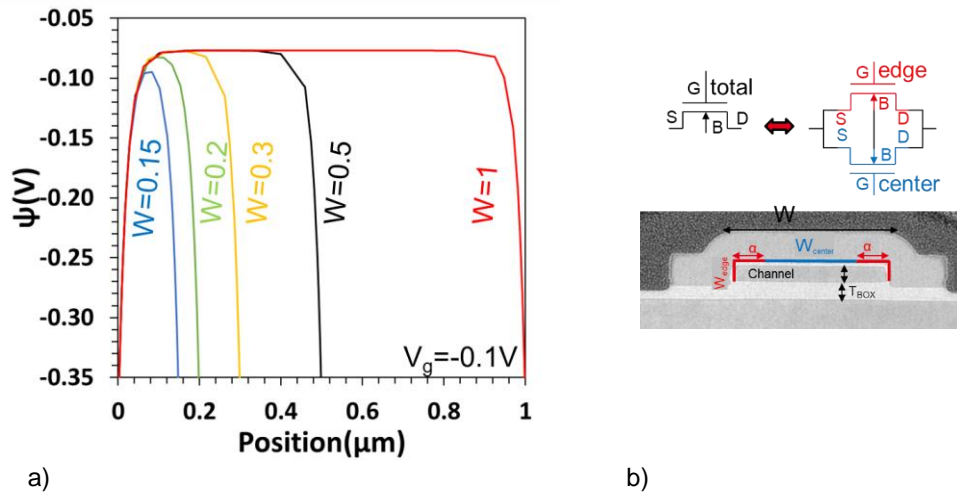


Figure 3 : a) Potential variation along W from 3D TCAD pMOS for various W and b) Device components schematic: Center and Edge operating in parallel

So, if the device width is higher than $0.2 \mu m$ ($W > 0.2 \mu m$), the mesa-isolated transistor can be seen as two transistors in parallel (**Figure 3.b**): the edge transistor with a constant, W -independent, current (in red) and the center one, similar to a planar SOI transistor, (in blue) (1), with width equal to $W - 2\alpha$, where 2α is the part of the top which is dominated by edge conduction.

$$I_{d,tot} = J_{d,center} W_{center} + J_{d,edge} W_{edge}, \quad W_{center} = W - 2\alpha \ \& \ W_{edge} = 2T_{Si} + 2\alpha \quad (1)$$

where $I_{d,tot}$ is the total current, $J_{d,center}$ the center transistor current density, $J_{d,edge}$ the edge transistor current density, and α is the center region portion governed by the edges.

Thus, to evaluate each contribution, we can use the $I_d - V_g$ curve of $W_{min} = 0.2 \mu m$ as a reference:

$$I_{d,edge} = J_{d,edge} W_{edge} = \left[I_{d,tot}(W) - I_{d,tot}(W = 0.2) \right] \frac{W - 2\alpha}{0.2 - 2\alpha} \frac{0.2 - 2\alpha}{0.2 - W} \quad (2)$$

Our methodology is used with 3D TCAD simulation on **Figure 4** with $\alpha = 90nm$ ($W = 0.2 \mu m$ in **Figure 3.a**). It demonstrates that the subthreshold regime is fully driven by the edge transistor, regardless the device width. It shows as well that the narrower structure is closer to a tri-gate architecture and is completely driven by the edge transistor.

Figure 4 explains as well that the knee appears only for wide devices, due to the difference in terms of current value at strong inversion between the several device widths W .

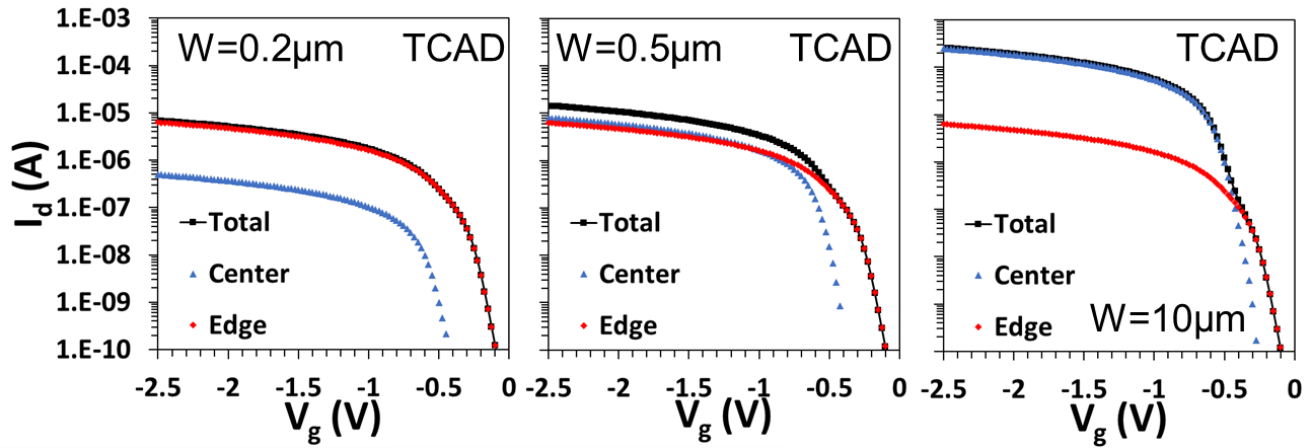


Figure 4 : 3D TCAD I_d - V_g in a linear regime ($V_d=-0.1V$): Extraction of center and edge contributions for devices with 3 W values 0.2, 0.5 and $10\mu m$

Additional TCAD simulations are performed to check our decomposition methodology validity with channel doping and back gate voltage V_b variation, and their impact on α . **Figure 5** shows the potential variation in the active from the center to the edge ($\Delta\psi$). Higher channel doping and/or higher V_b increase the potential difference between center and edge: the V_t difference between the 2 contributions increases and the double hump is more visible. The inset figures show also that α , extracted as the position where $\Delta\psi$ saturates and becomes negligible, i.e. smaller than $-0.5mV$, at the center of the device increases with increasing doping and V_b , which indicates that the edge device width W_{edge} increases. Moreover, it indicates that the “edge/center” transistor model is valid down to a minimum device width W_{min} , which increases with increasing the back-gate bias and the channel doping.

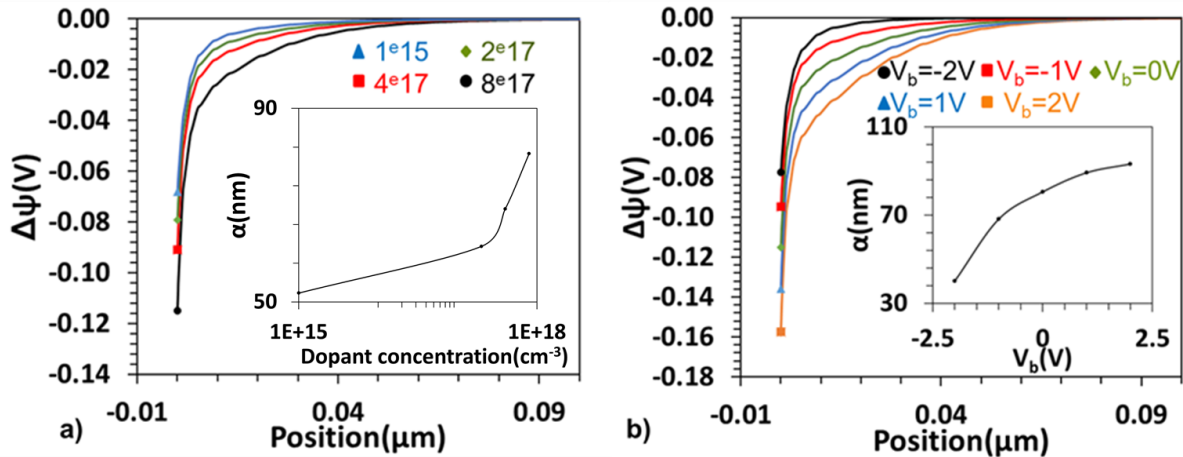


Figure 5: 3D TCAD pMOS $W=0.5\mu m$ $\Delta\psi$ vs position along W (1nm below gate oxide at ($V_g=V_t$) and extracted alpha value at $\Delta\psi=-0.5mV$ a) vs channel doping b) vs back gate bias

The potential variation versus V_g for several V_b values (**Figure 6.a**), is plotted for both components: edge (at 10nm far from the edge and 1nm below the gate oxide) and center (at 100nm far from the edge and 1nm below the gate oxide). First, we consider the edge component, dash curves on **Figure 6.a**. The gate voltage at which we reach a threshold potential of $-0.4V$ (where we are not impacted by the surface potential saturation), is extracted for each back-bias polarization (dashed curves). Then, the extracted values are used to extract the difference of potential to the extracted value for $V_b=0V$ “ $\Delta\psi$ ”, in order to perform the comparison to the ΔV_t extracted by our methodology in **Figure 6.b**. At a second time the same work is done for the center component. This demonstrates that the V_t extractions for the edge and the center follow the potential variations coming from 3D TCAD (**Figure 6.b**).

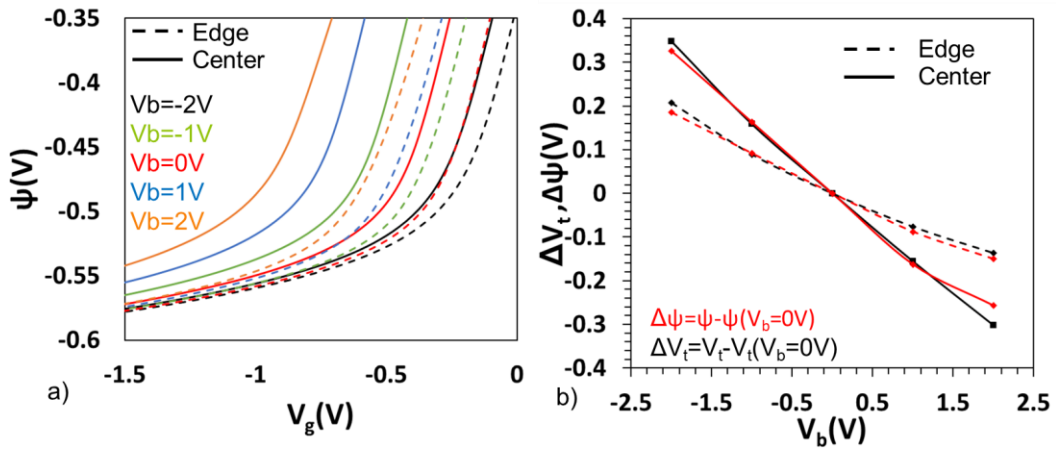


Figure 6: pMOS $W=0.5\mu\text{m}$ a) Potential versus V_g for several V_b values: $-2 \rightarrow 2\text{V}$ for center and edge components b) $\Delta\psi - V_b$ versus $\Delta V_t - V_b$ for both components

To identify α experimentally, the TCAD edge transistor transconductance ($g_{m,\text{edge}}$) versus V_g is plotted for several α values (**Figure 7.a**). For very low values of α (here $<0.04\mu\text{m}$), $g_{m,\text{edge}}$ does not follow the expected trend, providing an indicator to determine the minimum α value, α_{min} .

Then, the edge and center transistors $I_d - V_g$ are plotted for $\alpha > 0.04\mu\text{m}$ (**Figure 7.b**), from where we can conclude that if α is sufficiently high ($\alpha > \alpha_{\text{min}}$), the subthreshold regime is not impacted. This proves that our methodology can be used to analyze this regime.

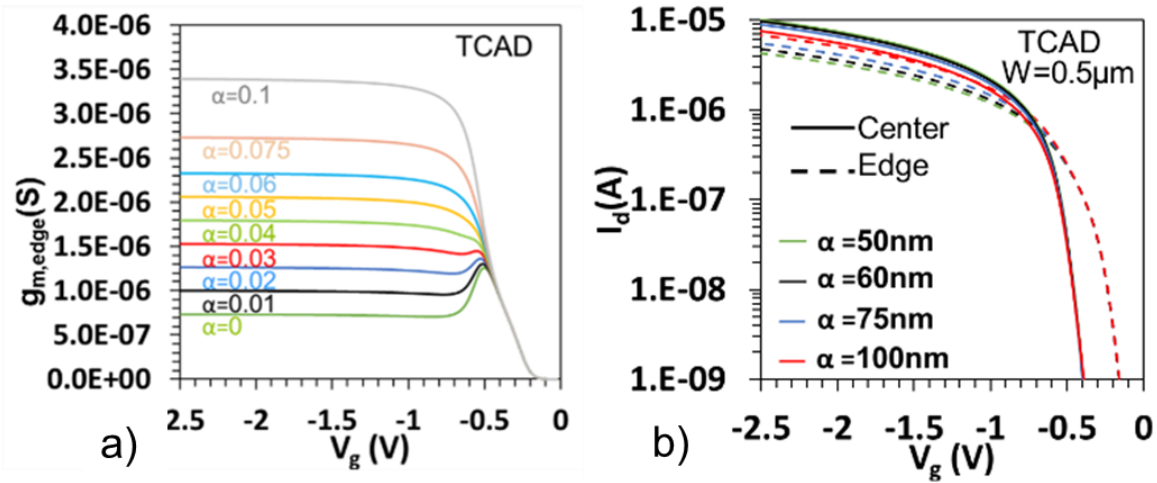


Figure 7 : pMOS 3D TCAD: a) Edge device transconductance $g_{m,\text{edge}} - V_g$ extracted for α (0 to 100nm) and b) pMOS 3D TCAD $I_d - V_g$ at $V_d = -0.1\text{V}$ for α from 50 to 100nm Edge & Center transistor

5. Experimental application

The threshold voltage V_t of doped channel devices was extracted at constant current ($10^{-7}(\text{W/L})$), with W the width of each current contributor) (**Figure 8**). The total current threshold voltage $V_{t,\text{tot}}$ for the narrowest structures is closer to that of edge component one $V_{t,\text{edge}}$. It shows that $V_{t,\text{tot}}$ (total transistor) depends on W , and it is closer to $V_{t,\text{center}}$ (center component) for higher W , because the extraction is done on a zone above the knee. This reveals that the threshold voltage is not impacted by the parasitic edge transistor, for the largest device ($W=10\mu\text{m}$) when the extraction is performed at a constant current equal to $10^{-7}(\text{W/L})$, and the problem remains if the extraction is done at a lower threshold current. This shows that the knee caused by the parasitic edge transistor skews the V_t extraction at a constant current. This also proves that the center transistor

behaves like a classical planar SOI one, because the center transistor V_t variation with V_b corresponds to the theoretical planar SOI trend from [10] (dashed curves in **Figure 8**).

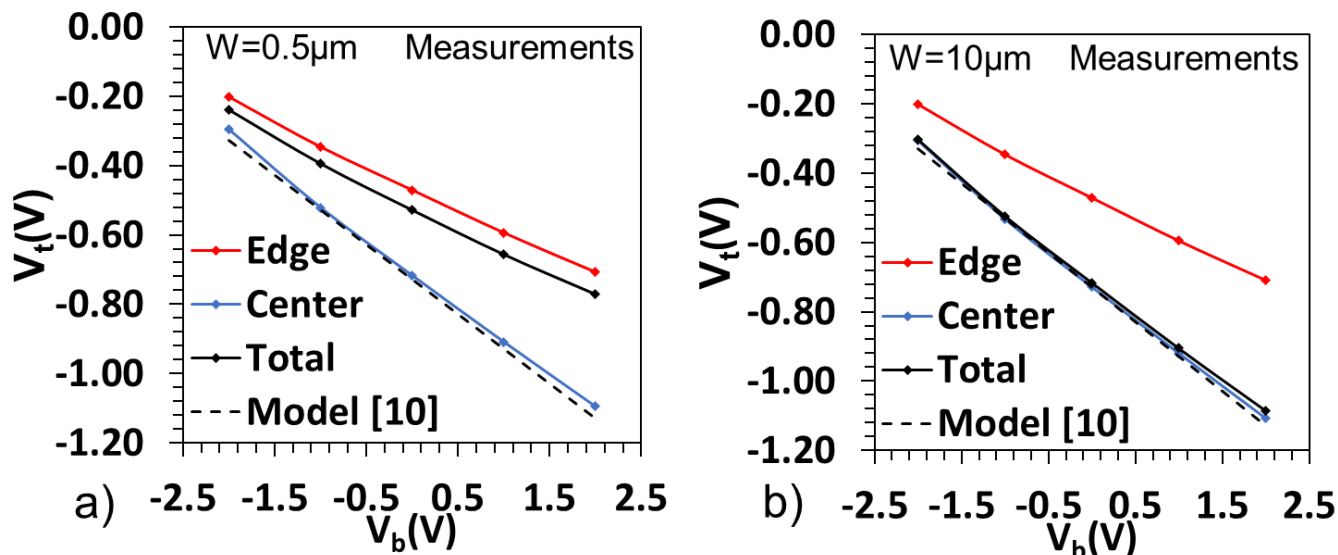


Figure 8 : pMOS measurement. Extracted threshold voltage in a linear regime V_t versus backgate polarization for edge, center and total transistor for several W values: a) $W=0.5\mu\text{m}$, b) $W=10\mu\text{m}$

For a pMOS with a doped channel device, the threshold voltage is then plotted versus the gate length for each component: total, edge and center in **Figure 9**. The difference of the threshold voltage to its value with a long channel device $L=1\mu\text{m}$ is then plotted to quantify the short channel effects ($\Delta V_{t,\text{SCE}}$). This demonstrates that the center transistor is the most impacted by the short channel effects.

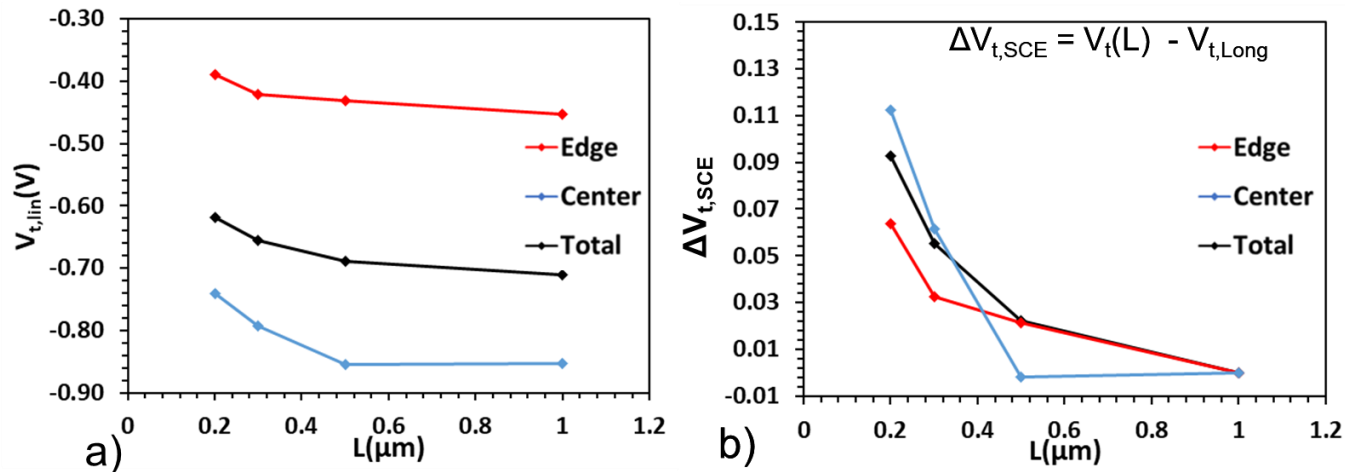


Figure 9: pMOS transistor $W=1\mu\text{m}$, a) extracted threshold voltage for each component total, edge and total versus gate length and b) difference of the threshold voltage to its value with a long channel device $L=1\mu\text{m}$

6. Conclusions

In this paper, we have demonstrated the presence of a parasitic transistor at the edges of SOI pMOSFETs due to the mesa isolation. This results in an early conduction which impacts the subthreshold region of the transfer characteristic. We have presented a methodology to decompose edge and center contributions in mesa-isolated SOI pMOSFETs, in order to properly study the operation in threshold regime. It was revealed that the subthreshold regime is always driven by the edges in a pMOS transistor with a doped channel. This

explains why the threshold voltage V_t is less modulated by the back-bias voltage. These effects are worsened when increasing the back-bias voltage V_b , or for higher channel dopant concentration as well. We have shown as well that the center transistor is more impacted by the short channel effects. Finally, the proposed model could be further developed to analyze the Floating Body effects, especially occurring in doped channel devices.

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