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# Noise modeling using look-up tables and DC measurements for cryogenic applications

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**Abstract**—There is today a lack of mature transistor-level compact models for the simulation of integrated circuits at cryogenic temperatures. This is particularly the case for the simulation of the noise behavior which is critical for most applications. In this paper, we aim at an efficient prediction of the white noise behavior of basic amplifying stages working at RF frequencies and cryogenic temperatures. For this, we propose the use of DC measurements that are incorporated in a Look-Up Table (LUT) and fed to a mathematical noise model. We illustrate the approach for the case of a transistor in common source configuration. The results of circuit simulation of the noise parameters in the standard temperature range are very close to the estimation of the same parameters using the LUT with just DC measurements. The approach can be readily extended to the analysis of circuits with multiple components. Next, the LUT approach is used for estimating the noise parameters at cryogenic conditions, considering DC measurements that have been carried out at these temperatures. The paper illustrates the feasibility of carrying out a cryogenic design using a LUT-based approach while accurate compact models are not yet available.

**Index Terms**—cryogenic modeling, noise estimation, look-up table design, CMOS quantum computing, Fano factor.

## I. INTRODUCTION

Recent advancements in quantum bit (qubit) research are paving the way for large scale quantum computers that will be able to address computational tasks beyond the reach of classical computers. Many applications are foreseen in areas as diverse as weather prediction, drug development, search algorithms and fundamental physics simulation. Such a computer requires the integration of millions of qubits working at cryogenic temperatures, while noise and power consumption must be at extremely stringent low values. This requires the use of cryogenic reactors with multiple refrigerated stages with the quantum bits placed at the lowest temperature level, typically in the order of mK.

Among multiple possibilities for building such a computer, the use of silicon technologies is a promising approach due to the high potential for integration [1]- [3]. Recent research has demonstrated “hot” silicon qubits that operate at several Kelvin [4], easing the thermal constraints and potentially enabling the integration of classical control electronics within

the qubit array [5]. Silicon technologies such as 28 nm FD-SOI are well suitable for the design of low-noise and low-power analog/RF readout interfaces. Furthermore, recent work has demonstrated correct functionality of circuits implemented with this technology at cryogenic temperatures [6] and the potential for building spin-based qubits [7].

Low Noise Amplifiers (LNAs) are ubiquitous circuits for the readout of quantum bits. Since they are the first element in the measurement chain, their noise impact is critical for guaranteeing a sufficient Signal-to-Noise Ratio (SNR). In previous work, we aimed at designing efficient 28 nm FD-SOI LNAs working at cryogenic temperatures, following a  $g_m/I_d$  design methodology as described in [8]. Unfortunately, current microelectronic design environments lack accurate cryogenic compact models, in particular for modeling the noise behavior and selecting the most suitable amplifying stages. In order to address this shortcoming, we propose to use a mathematical model, together with a numerical computing environment (eg. MATLAB), to predict noise behavior from DC measurements that are stored in a Look-Up Table (LUT) for basic amplifying stages. This mathematical model considers white noise since other sources of noise (such as flicker noise) can be neglected at the frequency of operation of the actual LNAs. The white noise model is based on the use of the shot-noise suppression factor (called Fano factor [9]) that shows consistent results with experimental data down to cryogenic temperatures [10].

This paper describes the derivation of the mathematical model and its integration within MATLAB to address the shortcomings of current compact models. Section II reviews the basic principles behind the LUT design and its motivation. Section III develops the mathematical noise model and the noise parameters that are considered for the evaluation of basic transistor configurations. The procedure for the extraction of the noise parameters using a look-up table with DC measurements is described. Section IV shows simulation results for the extraction of the noise parameters. The results obtained with a direct approach based on the LUT are compared with the results obtained via a circuit simulation at the standard temperature range to validate the LUT approach. The noise modeling approach based on suppressed-shot noise and network-based noise analysis together with the LUT-based extraction approach of noise parameters can be considered for

the evaluation of amplifying stages at cryogenic temperatures. Finally, Section VI gives some conclusions and directions for future work.

## II. DESIGN-ORIENTED LOOK-UP TABLE

The use of sophisticated compact models in a microelectronics design environment implies a lengthy iterative design process where the designer loses insight on the physical behavior. A comprehensive engineering solution for circuit design requires the derivation of a pragmatical transistor model, simple enough for giving sufficient insight of the phenomena taking place, but equally broad to capture its principal mechanisms. During many years, the square model has remained a quick way to size and understand the basics of the transistor behavior and electronic circuits. However, the increased complexity of modern technologies, associated with a reduction of the transistor sizes and the power supply levels, results in varied physical phenomena that render the square model inadequate.

A LUT-based design approach illustrated in Fig. 1 uses an interface between MATLAB and an electrical circuit simulator such as SPECTRE in order to provide a quick alternative to the design based on the square model [11]. The LUT is obtained with a 4-dimensional DC sweep of transistor length, gate to source, drain to source and back-gate voltages which allows the tabulation of required DC transistor parameters. Once loaded into MATLAB, the use of scripts and commands allows the analysis of a circuit architecture. Circuit output parameters are evaluated by direct calls to the LUT. This approach can provide a first design solution, which can later be refined with the use of the design environment and its accurate compact models if available.

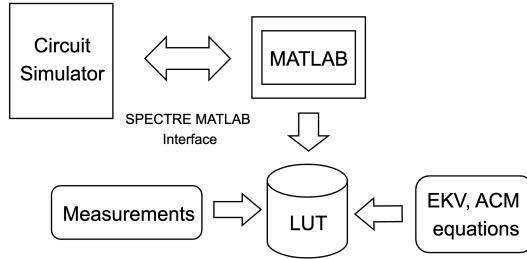


Fig. 1. Measurement data and EKV or ACM generated parameters are added to the LUT generated by the interface between MATLAB and SPECTRE.

The LUT is limited to data that can be obtained via electrical circuit simulation and the embedded compact models. This poses a problem for the design of cryogenic circuits since the compact models are no longer valid in this operation region. However, it is also possible to integrate in the LUT data obtained from actual measurements or data that can be derived from well-established easy-to-use models such as EKV and ACM. For the operation at cryogenic conditions, we also require a proper noise model and DC measurements to estimate the noise at different temperatures.

For cryogenic design, DC measurements outside the working limits of the compact model in the design environment

must be added to the LUT. This data may need to be first preprocessed to fit the intended working region of the LUT and then integrated into the MATLAB structure. The LUT for cryogenic design may be formed by DC measurements and simulation parameters obtained from simple constructed compact models such as EKV or ACM.

## III. CRYOGENIC NOISE MODEL PARAMETERS

The noise of any two-port circuit can be completely described by a series voltage noise source and a parallel current noise source at the input of the equivalent noiseless two-port circuit. These input-referred noise sources model the internal intrinsic noise sources and they have the advantage of allowing the study of the dependency of the noise to matching conditions, facilitating the calculation of the noise correlation matrix, since these noise sources are in general correlated with each other.

For a CMOS transistor, the standard channel thermal noise model overestimates the noise improvements seen in cryogenic amplifiers, hindering their sizing [10]. Assuming that the channel white noise in cryogenic conditions results essentially from suppressed shot noise, the noise at all operating regions and at cryogenic temperatures can be accurately modeled by means of a suppression coefficient called Fano factor  $F_a$  [12]. By considering the suppressed shot-noise model, we can construct the correlation matrix and derive from it the noise parameters of the two-port [14]. The noise correlation matrix for more complex architectures is easily calculated by simple operations on the individual component matrices.

In this Section, we explain the derivation of the noise correlation matrix for basic transistor configurations, the related noise parameters, and how this matrix representation can be estimated directly from the LUT parameters.

### A. Intrinsic MOSFET noise sources

The input-referred noise sources are calculated from a variation of the Pospieszalski model (Fig. 2) [15] that takes as the main contributors the suppressed shot-noise along the channel given by

$$\overline{i_{nd}^2} = 2qI_d\Delta fF_a \quad (1)$$

and the thermal generated noise source due to the gate resistance  $R_g$  given by

$$\overline{v_{ng}^2} = 4kT\Delta fR_g \quad (2)$$

where  $k$  is the Boltzmann constant,  $T$  is the device temperature,  $q$  is the elementary charge and  $\Delta f$  is the bandwidth in which the noise power is integrated. Both noise sources may be correlated due to the effect of transistor parasitics like  $C_{gd}$ .

If the technology model file used for the LUT generation has entries for the drain current  $I_d$  and the equivalent noise channel  $\overline{i_{nd}^2}$ , it is possible to derive the Fano factor  $F_a$  from (1). Otherwise, an alternative derivation using the EKV model [16] is given by

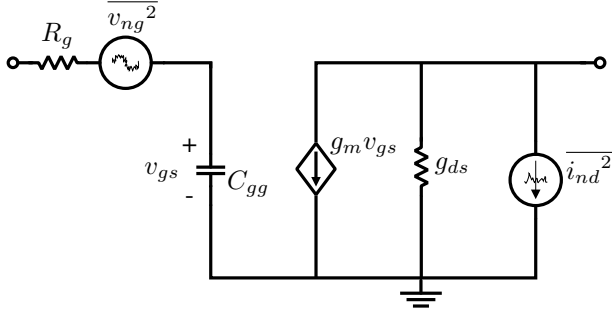


Fig. 2. The dominant noise contribution comes from channel noise ( $\overline{i_{nd}^2}$ ) followed by gate noise ( $\overline{v_{ng}^2}$ ) in a common source configuration.

$$F_a = 2\gamma_n U_T \frac{g_m}{I_d} \quad (3)$$

where  $g_m$  is the transconductance,  $\gamma_n$  is the thermal noise excess factor and  $U_T$  is the thermal voltage [10] [13]. It turns out that the Fano factor is almost independent from temperature, keeping a simple relationship to the normalized  $g_m/I_d$  given by

$$g_m/I_{d_{norm}} = \frac{g_m/I_d}{\max(g_m/I_d)} \quad (4)$$

which is a metric that is independent of technology and device geometry. In addition, [13] shows that it is also rather independent from temperature.

The modeling with a voltage noise source  $\overline{v_{ng}^2}$  of the effect of the gate resistance  $R_g$  may be less accurate at cryogenic conditions since the temperature behavior of the gate resistance is not yet fully understood [12]. An estimation of the gate resistance using the equivalent Y-parameters of a common source transistor when setting a transistor in strong inversion and  $v_d = 0$  is given by [19]

$$R_g = \text{real} \left( \frac{1}{Y_{11}} \right) \quad (5)$$

### B. Input-referred noise sources and noise correlation matrix

Considering the equivalent small signal noise model in Fig. 2 for a common source transistor, it is easy to derive the input-referred noise current source given by

$$\overline{i_n^2} = \overline{i_{nd}^2} \frac{\omega^2 C_{gg}^2}{g_m^2} \quad (6)$$

and the input-referred noise voltage source given by

$$\overline{v_n^2} = \overline{v_{ng}^2} + \frac{\overline{i_{nd}^2}}{g_m^2} (1 + \omega^2 R_g^2 C_{gg}^2) \quad (7)$$

Input-referred noise sources can be considered in a circuit consisting of many components, but as the complexity and number of components increase in a circuit architecture, a direct small signal approach becomes cumbersome. Instead, the use of the noise correlation ABCD-matrix  $[C_A]$  of each

component, constructed from the above input-referred noise sources as follows [19]

$$[C_A] = \begin{bmatrix} \langle v_n v_n^* \rangle & \langle v_n i_n^* \rangle \\ \langle i_n v_n^* \rangle & \langle i_n i_n^* \rangle \end{bmatrix} \quad (8)$$

simplifies the task.

Using the above results, the noise correlation ABCD-matrix for the common source transistor  $[C_{Acs}]$  is given by

$$[C_{Acs}] = \begin{bmatrix} \overline{v_{ng}^2} + \frac{\overline{i_{nd}^2}}{g_m^2} (1 + \omega^2 R_g^2 C_{gg}^2) & \frac{\overline{i_{nd}^2}}{g_m^2} (\omega^2 C_{gg}^2 R_g - j\omega C_{gg}) \\ \frac{\overline{i_{nd}^2}}{g_m^2} (\omega^2 C_{gg}^2 R_g + j\omega C_{gg}) & \overline{i_{nd}^2} \frac{\omega^2 C_{gg}^2}{g_m^2} \end{bmatrix} \quad (9)$$

### C. Noise parameters

We consider here the noise parameters derived from the *noise impedance formalism* in order to model the behavior of a two-port network. This includes three parameters: the minimum noise factor  $F_{min}$ , the optimum impedance  $Z_{sopt}$  required at the signal source to reach the minimum noise figure  $F_{min}$ , and the noise conductance  $G'_n$  which describes the degree of sensitivity by which the noise figure changes with respect to noise impedance mismatch. The three parameters are related as follows [18]

$$F = F_{min} + \frac{G'_n}{R_s} |Z_s - Z_{sopt}|^2 \quad (10)$$

The noise correlation ABCD-matrix and the two-port noise parameters are related by [18]

$$[C_A] = 4kT_o \Delta f \begin{bmatrix} R_n & \frac{F_{min}-1}{2} - R_n Y_{opt}^* \\ \frac{F_{min}-1}{2} - R_n Y_{opt} & R_n |Y_{opt}|^2 \end{bmatrix} \quad (11)$$

where  $T_o$  is the reference temperature of 290 K.

For the common source transistor, we can consider a white noise analysis considering the channel suppressed shot-noise and gate resistance noise models, which leads to the following formulae that is conceptually valid at cryogenic temperatures

$$G'_n = \frac{I_d F_a}{2U_{T_o}} \left( \frac{f}{f_t} \right)^2 \quad (12)$$

$$Z_{sopt} = \sqrt{R_g^2 + 2R_g \left( \frac{f_t}{f} \right)^2} \frac{U_T}{I_d F_a} + \frac{j}{\omega C_{gg}} \quad (13)$$

$$F_{min} = 1 + \frac{I_d F_a}{U_{T_o}} \left( \frac{f}{f_t} \right)^2 R_g^2 + \frac{f}{f_t} \sqrt{\left( \frac{I_d F_a}{U_{T_o}} \right)^2 \left( \frac{f}{f_t} \right)^2 R_g^2 + 2R_g \frac{I_d F_a}{U_{T_o}} \frac{T}{T_o}} \quad (14)$$

where  $f_t = \frac{g_m}{2\pi C_{gg}}$  and  $U_{T_o} = \frac{kT_o}{q}$ .

#### D. LUT-based extraction of noise parameters

The procedure for a look-up table noise computation in MATLAB starts by defining a two-port as an interconnection of basic stages. The type of noise representation of each stage is chosen depending on their interconnections. The noise correlation ABCD-matrix is preferred as indicated above. The noise correlation ABCD-matrix of the overall circuit is obtained by simple matrix multiplication of the components in a cascaded configuration [14]. For the case of two components, the calculation is as follows

$$C_A = A_1 C_{A_2} A_1^* + C_{A_1} \quad (15)$$

where  $C_A$  is the total noise correlation matrix of the cascaded circuit with component 2 connected at the output of component 1, and  $C_{A_i}$  and  $A_i$  for  $i = 1, 2$  correspond to the ABCD noise correlation and transmission matrices, respectively, of each component. For some configurations, the use of noise impedance [ $C_Z$ ] and admittance [ $C_Y$ ] correlation matrices may be required. Direct relationships exist for transforming noise impedance, admittance and ABCD-correlation matrices between each other [14].

For example, a cascode amplifier can be decomposed into three basic amplifying stages as shown in Fig. 3 which include a common source, common gate and load stages. The noise correlation ABCD-matrix of the cascode amplifier [ $C_{Acas}$ ] is derived as the product of the noise correlation ABCD-matrices of all stages which is not given here because of the long formulae.

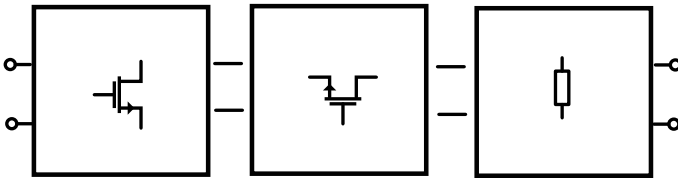


Fig. 3. The noise model of a cascoded amplifier is described by the multiplication of the noise correlation ABCD-matrices of the stages.

This matrix can then be evaluated from the LUT database for a given frequency, temperature and bias conditions. The relationship between the noise correlation ABCD-matrix and the IEEE noise parameters given in Eq. (11) allows the calculation of the noise performances of the two-port network at this frequency.

#### IV. LUT-BASED NOISE PARAMETER RESULTS

In this Section, we validate with simulation results the LUT-based extraction of the noise parameters of a 28 nm FD-SOI STMicroelectronics NMOS common source transistor. The LUT is generated with a circuit simulator using a 4-dimensional DC sweep of transistor length, gate to source, drain to source and substrate voltages for different temperatures, and tabulating all relevant device parameters for a fixed width  $W$  that is set at  $4 \mu\text{m}$ . We consider a transistor of length

30 nm biased at  $V_{gs} = 500 \text{ mV}$ ,  $V_{ds} = 1 \text{ V}$  and  $V_{sb} = 0 \text{ V}$  (back bias grounded).

The results in Fig. 4 extracted from the LUT show an almost linear relationship between the Fano factor  $F_a$  and the normalized  $\frac{G_m}{I_D}$  described in Eq. 3. For low values of  $\frac{G_m}{I_D}$ , the Fano factor is small showing that channel noise is mostly thermal which is the case of strong inversion when carrier drift is the major type of current. On the other hand, for high values of  $\frac{G_m}{I_D}$ , the Fano factor is close to 1 showing mostly shot channel noise which is the case in weak inversion when carrier diffusion is the major current type. This relationship varies only slightly with temperature in the standard temperature range [233.15, 398.15] K for which simulation data is available as shown in Fig.4 where the Fano factor variation over a temperature range of  $165^\circ\text{C}$  is smaller than 0.1 for a fixed  $\frac{G_m}{I_D}$  of 0.5. This is expected to be the case down to cryogenic temperatures. As a result, it is possible to estimate the channel noise relatively independently of temperature, just as a function of the transistor length and bias conditions that define the level of inversion given by  $\frac{G_m}{I_D}$ .

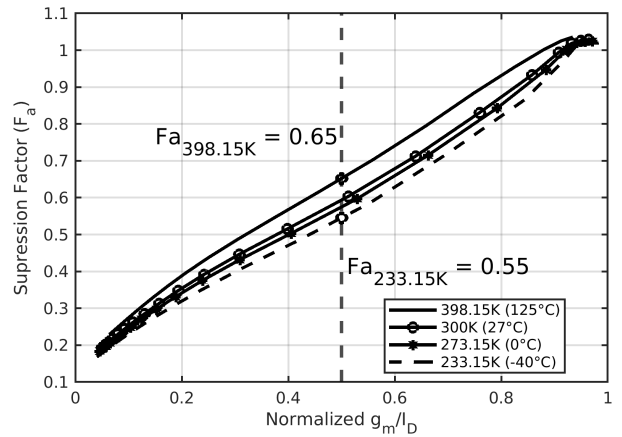


Fig. 4. Fano factor  $F_a$  versus normalized  $\frac{G_m}{I_D}$  for different temperatures in the standard range.

We next use the LUT to calculate the noise parameters. The gate resistance is calculated using (5) and it is assumed to be frequency independent. The results are given in Table I and compared with those obtained with a circuit simulation for different temperatures in the standard range. The results of the noise parameters as a function of frequency at 300 K derived from the look-up table are given in Fig. 5. At very high frequencies, the noise parameters grow quadratically, due to the dependency to the input gate capacitance of both sources. The small differences between LUT and circuit simulation results may be due to limitations of the noise model such as channel noise and gate resistance noise correlation due to the capacitance  $C_{gd}$  which has not been considered in the model of Fig. 2. The effect of this capacitance is more important at very high frequencies and for long channel transistors.

It is important to note that the threshold voltage temperature variation redefines the inversion region of the transistor, and

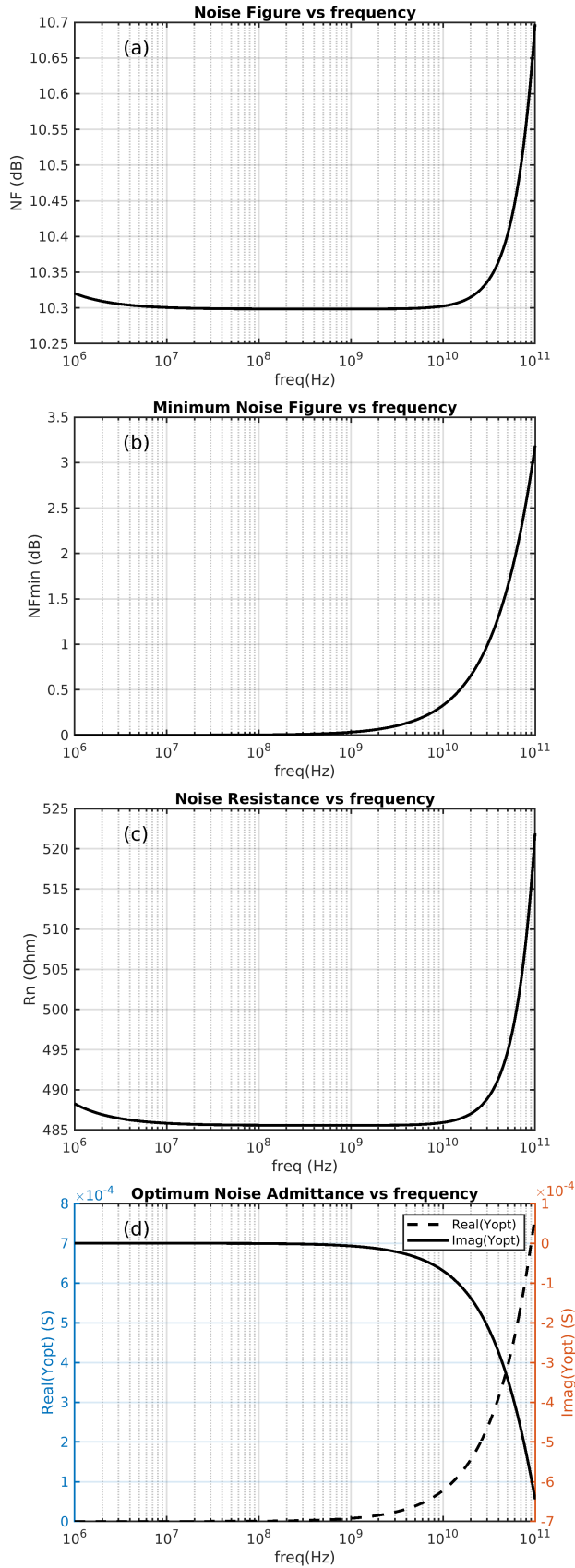


Fig. 5. Noise parameters of the common source transistor as a function of frequency obtained by look-up table calculations at 300 K.

TABLE I  
NOISE PARAMETERS AT 7GHZ FOR DIFFERENT TEMPERATURES.

Temp (K)	233.15	273.15	300	398.15
$NF_{LUT}$ (dB)	8.95	9.77	10.3	12.03
$NF_{SIM}$ (dB)	9.08	9.91	10.45	12.18
$NF_{minLUT}$ (mdB)	164.3	203.2	232.6	365
$NF_{minSIM}$ (mdB)	170	210	240	355.9
$Rn_{LUT}$ ( $\Omega$ )	342.3	424	485.7	747.2
$Rn_{SIM}$ ( $\Omega$ )	354.1	439.42	504.16	776.68
$Y_{optLUT}$ ( $\mu S$ )	55.0-47.6i	55.1-48.3i	55.2-49.0i	55.5-51.9i
$Y_{optSIM}$ ( $\mu S$ )	55.1-48.8i	55.1-49.5i	55.0-50.2i	54.8-52.7i

is thus the principal reason of the temperature dependency in Fig.4. A second major factor is attributed to the gate resistance. This effect reduces as temperature decreases since channel noise is more important. Notice also that the optimum noise admittance remains almost constant to temperature. This is attributed to the direct relationship between  $Y_{opt}$  and  $C_{gg}$  which mostly remains unchanged with temperature.

Table II compares the extraction of noise parameters via the LUT and circulation simulation for different transistor lengths at 300 K. Both results are still close, but the differences increase for longer transistors. Again, this is due to the parasitic capacitor  $C_{gd}$  which is not included in the noise model and which should be added for long transistors.

TABLE II  
NOISE PARAMETERS AT 7GHZ FOR DIFFERENT LENGTHS AT 300 K.

Length (nm)	34	100	300
$NF_{LUT}$ (dB)	10.44	10.16	14.15
$NF_{SIM}$ (dB)	10.15	10.07	13.5
$NF_{minLUT}$ (mdB)	238.6	611.5	3200
$NF_{minSIM}$ (mdB)	236	437	2270
$Rn_{LUT}$ ( $\Omega$ )	503.9	468.3	1233
$Rn_{SIM}$ ( $\Omega$ )	467.168	457.73	1065.2
$Y_{optLUT}$ ( $\mu S$ )	54.6-45.6i	15.1-23.7i	33-9i
$Y_{optSIM}$ ( $\mu S$ )	58.3-53.4i	7.11-14.1i	28-3.5i

From DC measurements of a 28 nm long FD-SOI common source transistor at 4 K with bias conditions as before ( $V_{gs} = 0.5V$ ,  $V_{ds} = 1V$  and  $V_{sb} = 0V$ ), we can calculate the cryogenic noise parameters. From the measurements we obtain  $C_{gg} = 2.2fF$ ,  $g_m = 5.2\mu S$ ,  $I_d = 347.82\mu A$  and from the linear temperature dependence of the gate resistance in Fig. 6 we can extrapolate  $R_g$  down to cryogenic temperatures (this is true at least down to 50 K as shown in [10]) giving  $R_g = 178.16$ . The accounted threshold voltage increase at cryogenic temperatures sets the transistor in weak inversion with an approximated Fano factor of 1.

Table III compares the LUT-extracted noise parameters for a 30 nm transistor at 300 K and a 28 nm one for which DC measurements are available at 4 K (unfortunately, both transistors have slightly different lengths since we cannot simulate transistors smaller than 30 nm and we only have cryogenic DC measurements at 28 nm). A frequency of 7 GHz is considered for a spin qubit readout. As expected the noise parameters are drastically diminished. Most importantly, it is theoretically possible to be noise adapted with a minimum

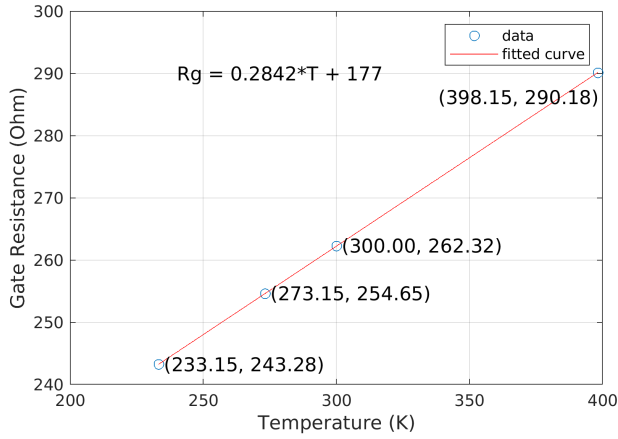


Fig. 6. Temperature dependence of the resistance gate  $R_g$  in the standard temperature range.

noise figure  $NF_{minLUT}$  of 31.13 mdB (noise temperature of 2 K). Given that the equivalent  $Z_{opt}$  ( $1/Y_{opt}$ ) diminishes at 4 K, it is possible to achieve simultaneous noise and power matching with less power consumption (by reducing the width  $W$ ) than at room temperature, and this can be further improved using the back-bias. Additionally, the total noise figure is 2 times less sensitive to input noise mismatch than at room temperature as shown by the parameter  $Rn_{LUT}$ . This shows the feasibility of the technology for the development of cryogenic readout circuits for quantum circuits.

TABLE III  
NOISE PARAMETERS AT 7GHZ AT ROOM AND CRYOGENIC TEMPERATURE.

Temp (K) / Length (nm)	300 / 30	4 / 28
$NF_{LUT}$ (dB)	10.3	7.69
$NF_{minLUT}$ (mdB)	232.6	31.13
$Rn_{LUT}$ ( $\Omega$ )	485.7	243.5
$Y_{optLUT}$ ( $\mu S$ )	55.2-49.0i	11.56-110i

## V. CONCLUSIONS AND FUTURE WORKS

This paper has presented a DC LUT-based design approach for extracting the noise parameters of a circuit down to cryogenic temperatures. Simulation results in the standard temperature range have validated the LUT-based approach for the case of a common source transistor. The paper demonstrates that an accurate representation of noise can be constructed out of just DC measurements. The approach can be readily used for the noise analysis of amplifying stages with multiple components. The intrinsic sources of transistor noise considered include channel noise and gate resistance noise down to cryogenic conditions, considering in particular the channel suppressed shot-noise model via the Fano factor. By making use of available DC cryogenic measurements, the noise parameters of a transistor at cryogenic temperatures have been predicted. The LUT-based approach paves the way for the optimization of the design of amplifying stages working at cryogenic conditions for which no compact models are yet

available. Future works with cryogenic noise measurements should validate this approach. Also we are aimed at using the LUT-based approach at cryogenic conditions combining the extraction of transmission and noise parameters so that the design trade-offs of basic amplifying stages for quantum circuit readout circuits can be analyzed and compared.

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