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# Static and LFN/RTN Local and Global Variability Analysis Using an Addressable Array Test Structure

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**Abstract**—The use of an addressable array test structure designed on a 28 nm FD-SOI technology for the variability analysis of static, low frequency noise (LFN) and Random Telegraph Noise (RTN) matching is presented. The experimental setup was validated, and a statistical analysis of the above electrical quantities is provided. Using such structures, combined with a switching matrix, local and global variability analysis can be performed while significantly increasing the number of samples, thus enabling a better description of the variations in LFN and RTN, especially when RTN signatures can be scarce. We show that local variations dominate the noise variability compared to global variations.

**Index Terms**—matching, low frequency noise, Random Telegraph Noise, variability, addressable test structure, statistical analysis

## I. INTRODUCTION

The reduction of the device area in CMOS technologies leads to greater variability of transistor matching, low frequency noise (LFN) and Random Telegraph Noise (RTN), which seriously affects the performances of analog and digital circuits [1]. Due to its intrinsic stochastic nature, a significant number of samples is needed to properly assess the LFN and RTN parameters variability, especially for small area devices, knowing that LFN and RTN variability scales with the inverse of the device area [2], [3]. To this end, the use of an addressable array test structure is proposed in this work to allow the characterization of multiple devices of different sizes from a 28 nm FD-SOI technology [4]. The test structure design enables the study of "global" variability corresponding to variations across the wafer, and "local" variability corresponding to variations on a single die at the minimal distances available. The test structure is first described, followed by a statistical analysis of static and noise parameters which validates the measurements and offers new results on the variability of these quantities on local and global scales.

## II. TEST STRUCTURE DESCRIPTION

### A. Test Structure General Design

The addressable test structure designed for this work, represented in Fig. 1, consists of an array of 2048 DUTs, arranged in 2 columns of 1024 identically designed and close pairs, that allows the measuring of the threshold voltage mismatch  $\sigma\Delta V_t$ , similarly to [5]. The test structure is embedded as a usual parametric test scribe using 25 pads with a 80  $\mu\text{m}$  pitch,

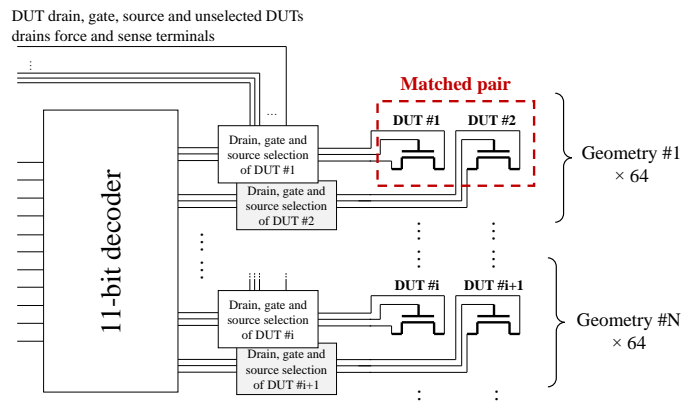


Fig. 1. Schematic representation of the addressable test structure.

with the entirety of it fitting in a 0.4  $\text{mm}^2$  region under the test scribe. A power supply is needed for the operation of the decoder, where the positive power supply voltage is set at  $V_{DD} = 1.8$  V and the negative power supply  $V_{SS}$  is set at ground.

### B. Test Structure Operation

Each DUT terminal is selected by switches powered by the internal circuit as shown in Fig. 2. The switch transistors consist of pairs of NMOS and PMOS of width  $W = 4$   $\mu\text{m}$ , length  $L = 0.15$   $\mu\text{m}$  and  $W = 12$   $\mu\text{m}$ ,  $L = 0.15$   $\mu\text{m}$  respectively. They are designed and placed to operate at a very low voltage and have an on-state resistance  $R_{ON} \approx 130$   $\Omega$ , which will limit the maximum current where the voltage drop across the switch remains negligible. Kelvin accesses are available on the drain, gate, and source terminals for each DUT, and the drain of the unselected DUTs is set with a dedicated pin at the same value as the drain voltage of the DUT to further minimize the leakage of drain access switches.

A 11-bit decoder, part of the addressing circuitry, addresses the 2048 transistors, where the first bit of address corresponds to the pair's left DUT if "0" or right DUT if "1". The following bits select the row of the transistor array.

### C. Experimental Setup and Measured Devices

The experimental setup is divided in two parts: on one side the noise measurement setup, and on the other side the

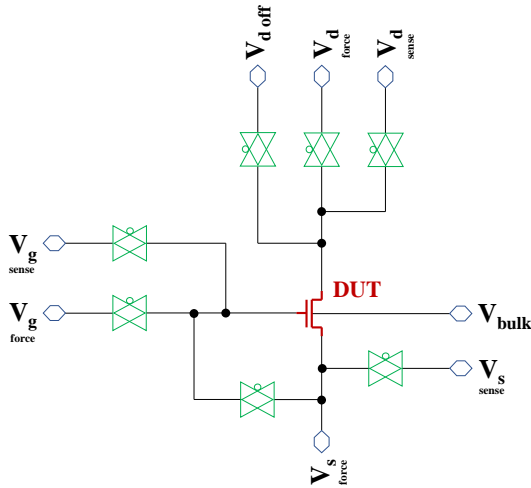


Fig. 2. Circuitry surrounding each DUT of the test structure. Kelvin accesses are available for the drain, gate and source terminals. Each DUT terminal is selected through switches.

addressing setup. Firstly, time and frequency domain noise measurements are done using the NOISYS equipment by Synergie Concept consisting of a low noise current amplifier, a precision voltmeter connected to the DC output of the amplifier, and a HP35670A spectrum analyzer connected to the AC output of the amplifier. The drain, gate, source, and bulk terminals of the DUT are connected to the bias units of the NOISYS equipment. Secondly, the addressing operation takes advantage of a switching matrix in which a voltage source  $V_{DD}$  is set as input. Thus, the 11 bits can be efficiently driven with one single voltage power supply. All the nodes (DUT terminals and addresses) are then connected to a 25-pin probe card mounted on an industrial prober.

To evaluate the viability of the test structure, NMOS transistors of  $EOT = 14 \text{ \AA}$  and a low  $V_t$  flavor were tested. A mismatch analysis was performed on 16 different geometries. For the noise analysis, the minimal accessible area transistor of  $W = 0.08 \text{ \mu m}$ ,  $L = 0.03 \text{ \mu m}$  and a larger one of  $W = 0.5 \text{ \mu m}$ ,  $L = 0.5 \text{ \mu m}$  were chosen. DC drain current ( $I_d$ ) and drain current noise ( $S_{I_d}$ ) power spectral density (PSD) measurements were performed for various gate voltages  $V_g$  bias in the linear regime ( $V_d = 0.05 \text{ V}$ ). The studies include global variability analysis corresponding to the statistical study across the wafer with one measured device per die for around 60 dies, and local variability analysis on a single die level with 100 measured devices on one die. Measurements of those devices on standard test structures, independent of the one designed for this work, were also performed as references to validate the results obtained from the addressable test structure.

### III. RESULTS AND DISCUSSION

#### A. Static Mismatch Analysis

Fig. 3(a) and Fig. 3(b) show the global  $I_d - V_g$  characteristics die-to-die spread of device #1 for the large and smaller

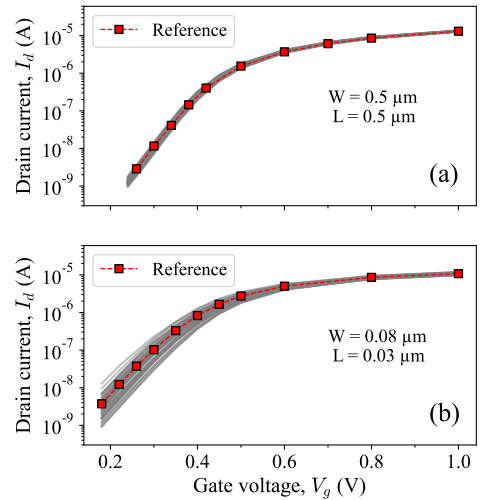


Fig. 3.  $I_d - V_g$  curves for all measured devices of  $W = 0.5 \text{ \mu m}$ ,  $L = 0.5 \text{ \mu m}$  transistors (a), and  $W = 0.08 \text{ \mu m}$ ,  $L = 0.03 \text{ \mu m}$  transistors (b). The squares correspond to the median characteristics from the independent standard test structure.

device, respectively. The current values and variability are a first indicator of the viability of the test structure, indicating that the measured currents correspond to the addressed devices and not to surrounding switch transistors. This is further confirmed by the measurements of devices of the same shapes from the independent standard test structure which exhibit the same median characteristics as the ones measured with the addressable test structure, as shown Fig. 3. Finally, the drain voltage across the switch transistors was measured by taking advantage of the Kelvin accesses of the DUT, showing a voltage drop of less than 5 mV under a gate voltage operation of 1 V, and thus demonstrating their negligible impact on the measurement of electrical characteristics of the DUT.

The single die mismatch analysis of the threshold voltage, extracted with the constant current method, is shown Fig. 4, where the extracted values clearly follow Pelgrom's law [6] with a coefficient  $A_{\Delta V_t} = 1.3 \text{ mV}\cdot\mu\text{m}$ . The test structure

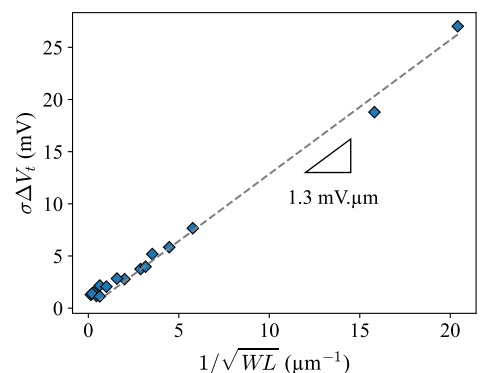


Fig. 4. Local (single die) transistor pairs mismatch standard deviation as a function of the inverse square root of device area.

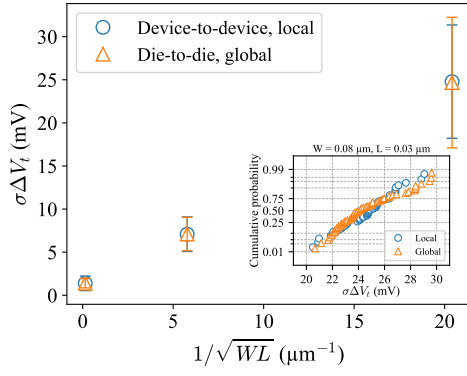


Fig. 5. Transistor pairs mismatch standard deviation as a function of the inverse square root of device area for the single die local samples and the die-to-die global samples. The distribution of  $\sigma\Delta V_t$  for the smallest geometry is represented in the inset, with normal percentiles scale.

allowed a comparison to be conducted between an analysis within a single die for 64 matching pairs per geometry, and between all 60 dies of a wafer, showing similar results and dispersion Fig. 5, demonstrating that local variations are dominant in the static variability processes.

### B. LFN Variability Analysis

The LFN variability analysis is undertaken using the input-referred equivalent gate voltage noise PSD  $S_{V_g} = S_{I_d}/g_m^2$ ,  $g_m$  being the transconductance, because it is suppressing the DC-related variability assuming that LFN is dominated by charge trapping/detrapping [7]. Examples of the noise spectra global spread of device #1 of the large and smaller geometries at a selected gate voltage  $V_g = 0.4$  V are shown in Fig. 6, including their median and extremum values. The median normalized drain current noise  $S_{I_d}/I_d^2$  extracted at  $f = 10$  Hz from the global samples for the two geometries are shown Fig. 7 with the carrier number fluctuations with correlated mobility fluctuations (CNF/CMF) model fit, given by [8], [9]:

$$\frac{S_{I_d}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \left(1 + \Omega \frac{I_d}{g_m}\right)^2 \quad (1)$$

In (1),  $S_{V_{fb}}$  is the flat-band voltage spectral density given by:

$$S_{V_{fb}} = \frac{q^2 k T N_t \lambda_t}{W L C_{ox}^2 f} \quad (2)$$

where  $N_t$  is the oxide trap density,  $\lambda_t$  is the tunnel attenuation distance, and  $\Omega = \alpha_{sc} \mu_{eff} C_{ox}$ , with  $\alpha_{sc}$  the Coulomb scattering coefficient. The CNF/CMF fit allows the extraction of the oxide trap density, with  $N_t = 3.0 \cdot 10^{17} \text{ cm}^{-3} \cdot \text{eV}^{-1}$  for the large geometry and  $N_t = 2.4 \cdot 10^{17} \text{ cm}^{-3} \cdot \text{eV}^{-1}$  for the small geometry. The global median  $S_{V_g}$  extracted at  $f = 10$  Hz for the two geometries is then compared in Fig. 8 to the local median  $S_{V_g}$  for 100 devices of one die and the reference values obtained from the independent standard structure, showing identical noise levels and thus the same extracted oxide trap density.

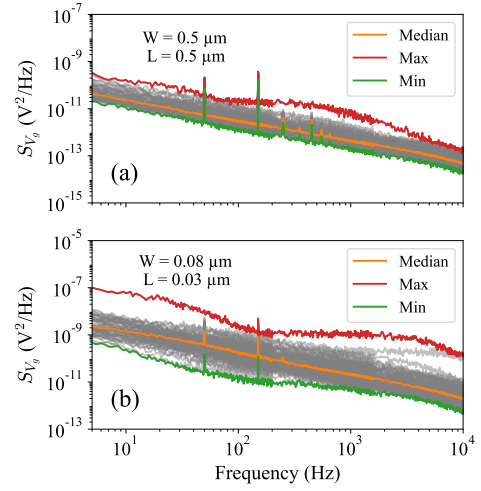


Fig. 6. Input-referred gate voltage noise PSD  $S_{V_g}$  of device #1 for all dies, of  $W = 0.5 \mu\text{m}$ ,  $L = 0.5 \mu\text{m}$  transistors (a), and  $W = 0.08 \mu\text{m}$ ,  $L = 0.03 \mu\text{m}$  transistors (b) for the same gate voltage  $V_g = 0.4$  V.

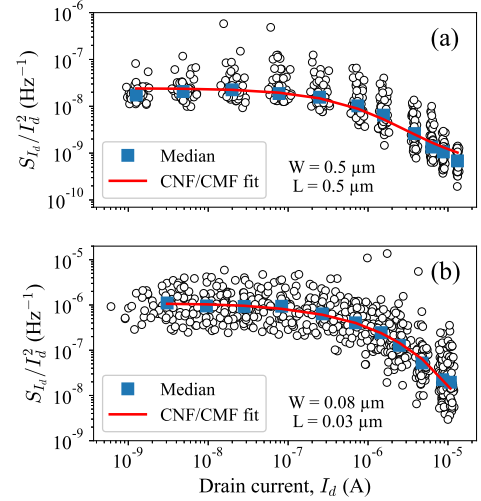


Fig. 7. Normalized drain current noise PSD  $S_{I_d}/I_d^2$  extracted at  $f = 10$  Hz of device #1, for all dies, of  $W = 0.5 \mu\text{m}$ ,  $L = 0.5 \mu\text{m}$  transistors (a), and  $W = 0.08 \mu\text{m}$ ,  $L = 0.03 \mu\text{m}$  transistors (b). The red line shows the CNF/CMF noise model fit to extract the trap density  $N_t$ .

The variability analysis is carried out by considering the standard deviation of  $\log(S_{V_g})$  since the measured data follows a log-normal distribution [10]. Fig. 9 shows global and local  $\sigma[\log(S_{V_g})]$  extracted at  $f = 10$  Hz versus the gate voltage for the two different geometries. A slight increase in standard deviation is observed when increasing the gate voltage, which could be related to the CMF impact on the noise in strong inversion as seen in Fig. 8. The standard deviation of  $\log(S_{V_g})$  was also measured for additional geometries to allow the study versus the inverse square root of device area Fig. 10. A 0.2 decade difference in standard deviation between the global and local samples of the small geometry is observed but can be explained by the stochastic nature of the choice of the samples, leading to the same conclusion as for the static

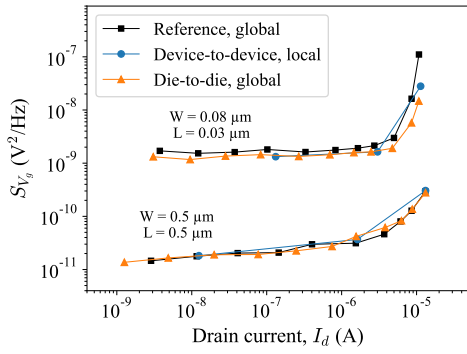


Fig. 8. Median input-referred gate voltage noise PSD  $S_{V_g}$  extracted at  $f = 10$  Hz as a function of the drain current, for all measured devices. The global samples, local samples and the results from the independent standard test structure are compared to each other, showing no significant difference.

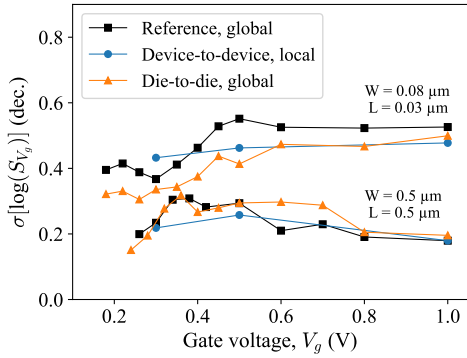


Fig. 9. Standard deviation of  $\log(S_{V_g})$  extracted at  $f = 10$  Hz as a function of the gate voltage, for all measured devices.

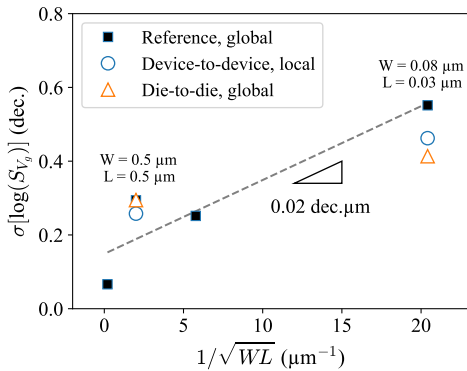


Fig. 10. Standard deviation of  $\log(S_{V_g})$  extracted at  $f = 10$  Hz and  $V_g = 0.5$  V as a function of the inverse square root of device area.

mismatch variability: local variations seem to dominate the noise variability processes. With the same noise levels and variability measured whether the sample is global with devices across the wafer, or local with multiple devices on a single die, the use of the addressable structure to perform statistical analysis of LFN is validated. RTN analysis with numerous devices can then be undertaken.

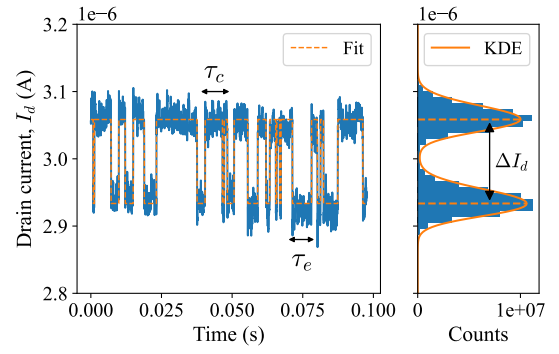


Fig. 11. Example of time-domain drain current noise measurement showing a RTN signature, and its associated histogram.

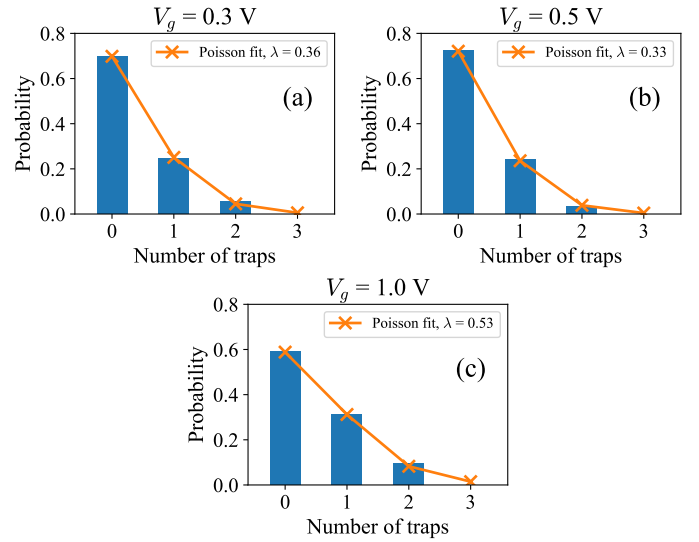


Fig. 12. Distribution of the number of active traps generating RTN in  $W = 0.08 \mu\text{m}$ ,  $L = 0.03 \mu\text{m}$  devices for  $V_g = 0.3$  V (a),  $V_g = 0.5$  V (b) and  $V_g = 1.0$  V (c), with fitted Poisson distributions.

### C. RTN Statistical Analysis

A statistical analysis of RTN was conducted locally on 100 devices of the small geometry  $W = 0.08 \mu\text{m}$ ,  $L = 0.03 \mu\text{m}$  and reproduced on two different dies with two different sampling frequencies, which adds up to 400 samples per  $V_g$ . An example of time-domain noise measurement using the addressable test structure and showing RTN is illustrated Fig. 11, with its associated amplitude  $\Delta I_d$  and trap mean capture and emission time constants  $\tau_c$  and  $\tau_e$ . Employing the processing of noise signals using smoothed histograms with kernel density estimation, as developed in [11], an estimation of the distribution of active traps responsible for RTN was performed and is shown Fig. 12. The RTN-inducing trap distribution follows a Poisson law [12], with the probability mass function given by:

$$f(k, \lambda) = \frac{\lambda^k e^{-\lambda}}{k!} \quad (3)$$

where  $k$  is the number of RTN-inducing traps in our case, and  $\lambda$  is the expected rate of occurrence or mean. Poisson fits



Fig. 13. Cartography of the detected RTN traps within the columns of the test structure corresponding to the  $W = 0.08 \mu\text{m}$ ,  $L = 0.03 \mu\text{m}$  devices, for two different dies, extracted at  $V_g = 1 \text{ V}$ .

conducted on the distributions show a mean  $\lambda$  between 0.33 and 0.56 depending on the gate voltage, with a net increase for  $V_g = 1 \text{ V}$ , representing a proportion of RTN signatures ranging from 30% to 40% in the studied samples. This means that in the case of an analysis carried out globally with around 60 devices, while an estimation of the trap distribution is feasible, only a few RTN signatures can be found which is not sufficient to establish relevant distributions of trap parameters. The addressable test structure thus allows the acquisition of a greater number of samples for the statistical analysis of RTN. A cartography of the RTN-induced traps within the scribe for the two different dies at  $V_g = 1 \text{ V}$  is shown Fig. 13, where the local distribution of traps within the scribe seems random. Traps mean capture and emission time constants  $\tau_c$  and  $\tau_e$  were extracted and presented on a capture/emission time map Fig. 14, showing a single explicit cluster, meaning that the traps responsible for RTN are from the same type and nature [13]. The distributions of the RTN amplitudes in terms of  $V_t$  shifts,  $\Delta V_t = \Delta I_d / g_m$ , are represented Fig. 15, showing possible log-normal distribution as mentioned in other studies [14]. The increase in  $\Delta V_t$  as  $V_g$  increases could be explained by the general higher noise level in strong inversion associated with CMF, also discussed in section III-B. The intermediate  $V_g$  shows a more scattered distribution, possibly due to the responsible traps being active in a wider gate voltage range, taking into account traps in common with the ones detected at  $V_g = 0.3 \text{ V}$  and  $V_g = 1 \text{ V}$ .

The addressable test structure thereby allows a significant increase in the number of measured devices, consequently improving the statistical analysis of RTN, since its study needs numerous samples that can be scarce depending on the geometry or the technology.

#### IV. CONCLUSION

The viability of using an addressable array test structure for the statistical analysis of static mismatch, LFN and RTN has been demonstrated. Noise level and variability analysis performed on devices from the test structure were presented. Local and global variability analysis are made possible, showing a significant dominance of the impact of local variations on the variability. Local studies using the addressable test structure on a few dies can thus be conducted, allowing the increase in the number of samples and enabling a better understanding of the variations in static and noise parameters such as the number of traps and their characteristics.

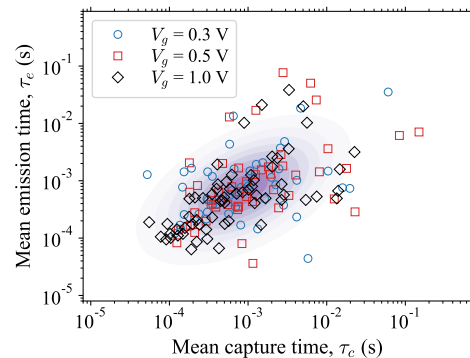


Fig. 14. Capture/emission time map extracted from the detected RTN signatures, for three different gate voltages.

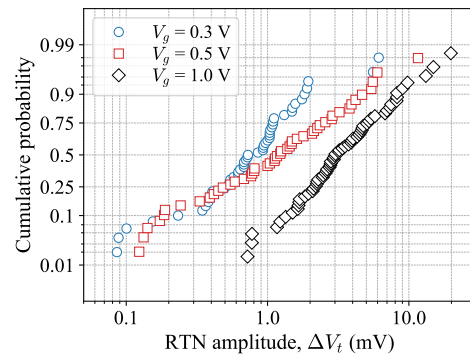


Fig. 15. RTN amplitude  $\Delta V_t$  distributions for three different gate voltages, with normal percentiles scale.

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