



HAL
open science

Drain Current Variability in 2-levels Stacked Nanowire Gate All Around P-type Field Effect Transistors

Donghyun Kim, Sylvain Barraud, Gérard Ghibaudo, Christoforos Theodorou,
Jae Woo Lee

► **To cite this version:**

Donghyun Kim, Sylvain Barraud, Gérard Ghibaudo, Christoforos Theodorou, Jae Woo Lee. Drain Current Variability in 2-levels Stacked Nanowire Gate All Around P-type Field Effect Transistors. 2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Mar 2023, Seoul, South Korea. pp.1-3, 10.1109/EDTM55494.2023.10103067 . hal-04305370

HAL Id: hal-04305370

<https://hal.science/hal-04305370>

Submitted on 27 Nov 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Drain Current Variability in 2-levels Stacked Nanowire Gate All Around P-type Field Effect Transistors

Donghyun Kim^{1,2}, Sylvain Barraud³, Gerard Ghibaudo¹, Christoforos Theodorou¹ and Jae Woo Lee^{2*}

E-mail: orion627@korea.ac.kr

¹Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, Grenoble INP, CNRS, IMEP-LAHC, 3 Parvis Louis Néel, 38016 Grenoble, France

²Electronics and information engineering, Korea University, 30019 Sejong, Republic of Korea

³Univ. Grenoble Alpes, CEA, LETI, 17 Av. des Martyrs, 38054 Grenoble, France

Abstract

An experimental study of drain current statistical characteristics in two vertically stacked nanowire MOSFETs (bottom one: Omega shaped and top one: nanowire) is presented. The most critical parameter variations are identified using an advanced mismatch model that well describes the experimental results, while the impact of channel geometry is examined for every source of process variations.

(Keywords: Nanowire, CMOS, FDSOI, global variability)

Introduction

Since the introduction of FinFETs, the multi gate structure has been considered as the key technology solution for further scaling down. For better gate control of the channel, gate all around (GAA) nanowire (NW) or nanosheet (NS) field effect transistors (FETs) have been developed for the next generation sub-15 nm complementary metal-oxide-semiconductor (CMOS) technology for nodes, exhibiting improved performance metrics such as I_{on}/I_{off} ratio, and subthreshold swing (SS) etc. Due to the aggressive scaling and the complexity of fabrication process however, device-to-device variability is becoming a limiting factor for the performance of GAA NW-based circuits. Generally, the variability within a wafer is divided in local (intra-die variations) and global (inter-die variations). From a circuit design point of view, it is important to consider the local variability (difference between

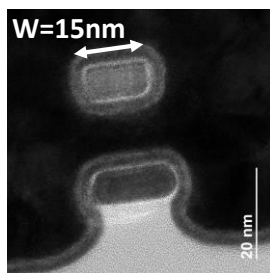


Figure 1. Cross-section TEM image of 2-vertically stacked Nanowire FETs with gate stacks (HfO_2 , TiN, and W metal)

neighboring transistors of the same circuit), but global variability is also a key parameter for evaluating and optimizing the process variation. In this study, we investigate the drain current, I_D , variability through measurements and model fitting in 2 vertically Stacked GAA NW FETs, aiming to identify the main sources of parameter variations and their dependence on channel geometry.

Device Information and Experimental Setup

Vertically stacked NW FETs were fabricated by CEA-LETI with state-of-the-art FDSOI technology. The channels width W and length L , in the devices under study varied in the range of 0.01-0.02 μm and 0.015-0.2 μm , respectively. These devices are composed of stacked nanowires (bottom one:

Omega gate shape and top one: GAA NW) as shown

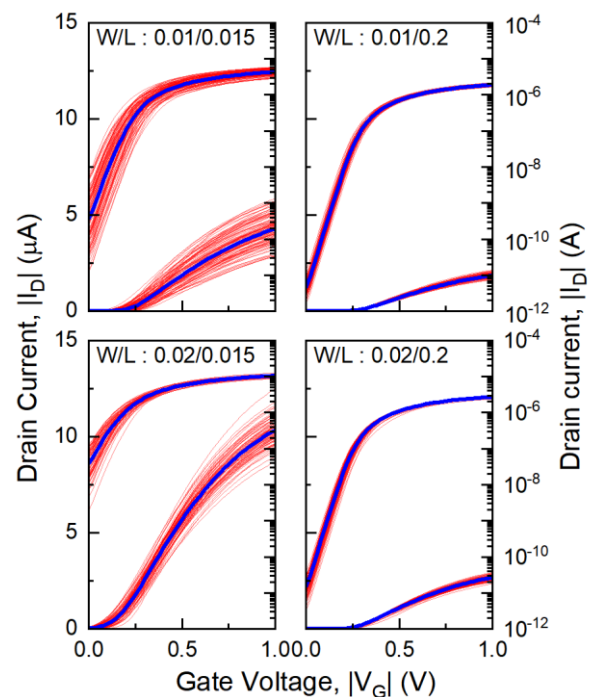


Figure 2. Typical I_D - V_G characteristics (red line) for various geometries on over 90 dies and average values (blue) on measured devices

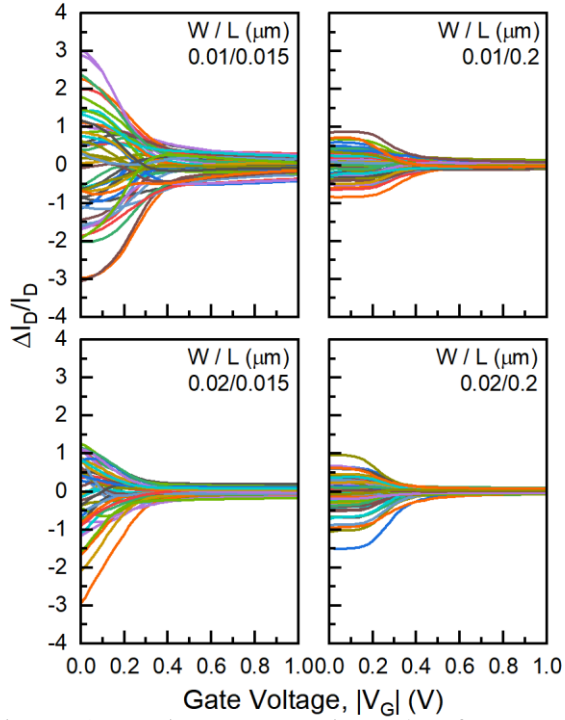


Figure 3. Drain current mismatch of NW FETs according to gate voltage on various geometries in Figure 1. The work function tunable metal gate and high-k dielectrics are composed of the layers with W/TiN/HfO₂ (equivalent oxide thickness EOT is 1.2 nm), and buried oxide BOX thickness is 145 nm. Transfer characteristics were measured with the gate voltage V_G from 0 to 1 V and drain voltage $V_D=30$ mV in linear region by using Agilent B1500 Semiconductor Device Parameter Analyzer and Cascade MicroTech automatic probe station. To conduct statistical characterization of global variability, static measurements were performed for over 90 dies and problematic measurements were filtered out.

Experimental Results and Analysis

Figure 2 presents typical linear, and log scaled plots of I_D - V_G characteristics for various geometries. Shorter L geometries on both of W (0.01 and 0.02 μm) obviously indicates higher variability of device characteristics. Especially, at $L=0.015$ μm device, electrical characteristics have large variation of on/off currents and threshold voltage V_{TH} regardless of the device W . Furthermore, comparing to $W=0.01$ μm with same device L , the $W=0.02$ μm device has high off current values. It seems to be difficult to optimize the device fabrication processes in aggressive scaled geometries.

The conventional intra-die local variability of I_D is calculated by using the logarithmic difference between two drain current value for the matching pair devices within the same die. On the other hand, the inter-die global variability is carried out by using average value from all measured $\Delta I_D/I_D = \ln(I_D/I_{D,avg})$, when only one current is obtained per die. As shown in Figure 3, the global variability of shortest device $L=0.015$ μm with $W=0.01$ μm is at least 3 times larger than one of longer channel device with $L=0.2$ μm . Because of relatively low V_{TH} for $W/L=0.02$ $\mu\text{m}/0.015$ μm , the variability of this case has smaller than $W=0.01$ μm . Following the Pelgrom's law [4], the drain current global mismatches for larger area devices are notably lower.

In Figure 4, the normalized standard deviations of the drain current mismatch are shown for different geometries. Despite of normalization for geometries, standard deviation of device $W/L=0.01$ $\mu\text{m}/0.015$ μm has larger than those of different geometries.

In order to elucidate these drain current mismatch dependences, we utilized the drain current variability model which is explained by Eq. (1). This equation is valid to linear regime and also weak to strong inversion following V_G . According to Eq. (1), the current mismatch could be attributed to uncorrelated origins of parameter variations: V_{TH} , β , and R_{SD} where $\beta=\mu_0 C_{ox} V_D W/L$ current gain factor, and R_{SD} the source/drain series resistance [1, 2].

$$\sigma^2(\Delta I_D/I_D) = (g_m/I_D)^2 \cdot \sigma^2(\Delta V_{TH}) + [1 - g_d \cdot R_{SD}] \cdot \sigma^2(\Delta \beta/\beta) + g_d^2 \cdot \sigma^2(\Delta R_{SD}) \quad \text{Eq. (1)}$$

where $\sigma(\Delta V_{TH})$, $\sigma(\Delta \beta/\beta)$, and $\sigma(\Delta R_{SD})$ are the

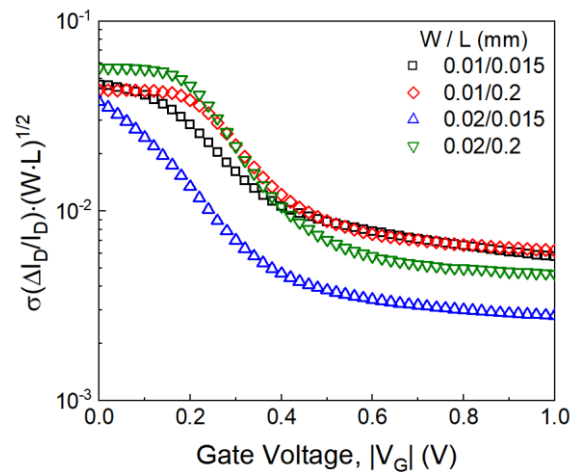


Figure 4. Normalized standard deviations of the drain current mismatch for different geometries in linear regime.

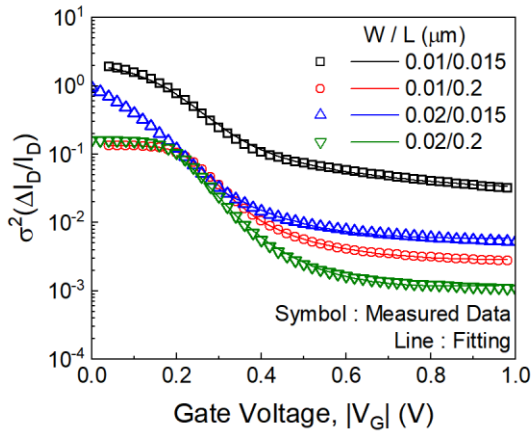


Figure 5. Mismatch variance versus gate voltage for different geometries. Mismatch fitting model (line) has a good agreement with experimental results (symbol)

standard deviations of each device parameter which are mentioned in parentheses, $I_{D,th}$ the drain current value for deciding V_{TH} , $g_d=I_D/V_D$ the channel conductance, and g_m the transconductance.

The variances of I_D mismatch as a function of V_G for various geometries are shown in Figure 5. Experimental data (symbols) and variability model (lines) which is explained in Eq. (1) demonstrated a good agreement from weak to strong inversion within all cases of devices [3]. Regardless of device W , I_D variances similarly decrease in high inversion region. It might be explained that the terms of standard deviations with V_{TH} and β are dominant to variability model following V_G . And, the variances of short devices $L=0.015$ have approximately 1 decade larger than those of long channel devices. It should be explained Pelgrom's law as Figure 3. As shown in Table 1, the standard deviations of each parameter were extracted by variability model for linear regime. Additionally, all standard deviations have similar trends following the device area according to Pelgrom's law [4].

Table 1. The standard deviations of variability parameters

W/L ($\mu\text{m}/\mu\text{m}$)	$\sigma(\Delta V_{TH})$ (mV)	$\sigma(\Delta\beta/\beta)$	$\sigma(\Delta R_{SD}/R_{SD})$
0.01/0.015	38.4	0.287	0.198
0.01/0.2	9.3	0.078	0.073
0.02/0.015	26.4	0.099	0.104
0.02/0.2	9.7	0.039	0.051

Conclusion

We carried out the drain current global variability for 2 vertically stacked GAA NW FETs. The global variability model was well fitted by experimental data for all cases of NW FETs devices. Furthermore, the extracted standard deviations from variability fitting are inversely proportional to the effective area of device.

Acknowledgments

This work has been supported by co-supervisor program between UGA and Korea University Sejong. And also supported by NRF-2022R1A2C1010447.

References

- [1] Rahhal, L., Bajolet, A., Diouf, C., Cros, A., Rosa, J., Planes, N., & Ghibaudo, G. (2013, March). New methodology for drain current local variability characterization using Y function method. In 2013 IEEE International Conference on Microelectronic Test Structures (ICMTS) (pp. 99-103).
- [2] Ioannidis, E. G., Theodorou, C. G., Haendler, S., Josse, E., Dimitriadis, C. A., & Ghibaudo, G. (2015). Impact of source-drain series resistance on drain current mismatch in advanced fully depleted SOI n-MOSFETs. IEEE Electron Device Letters, 36(5), 433-435.
- [3] Rahhal, L., Bajolet, A., Manceau, J. P., Rosa, J., Ricq, S., Lassere, S., & Ghibaudo, G. (2014, April). Mismatch trends in 20nm gate-last bulk CMOS technology. In 2014 15th International Conference on Ultimate Integration on Silicon (ULIS) (pp. 133-136). IEEE.
- [4] Pelgrom, M. J., Duinmaijer, A. C., & Welbers, A. P. (1989). Matching properties of MOS transistors. IEEE Journal of solid-state circuits, 24(5), 1433-1439.