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[a] *Department of Physics, Aristotle University of Thessaloniki, 54124 Thessaloniki, Greece*
[b] *Department of Informatics and Telecommunications, University of Ioannina, Arta, Greece*
[c] *IMEP-LAHC, INPG – Minatec, 3 Parvis Louis Néel, 38016 Grenoble, France*
[d] *CEA-LETI Minatec, 17 rue des Martyrs, 38054 Grenoble, France*

ABSTRACT

The threshold voltage of rectangular p-type triple-gate junctionless transistors (JLTs) is studied experimentally using the transconductance derivative (dg_m/dV_g) method, after correcting the drain current from the impact of series resistance. The effect of series resistance on the dg_m/dV_g behavior is highlighted. In the investigated devices, the high series resistance affects the dg_m/dV_g behavior more than the short-channel effects. The results show that, in addition to the flat-band voltage, for the first time two threshold voltages V_{th1} and V_{th2} are observed within the partial depletion region in devices with channel length varying from 95 to 25 nm. Numerical simulations of the holes density distribution reveal the absence of corner effects due to the unique bulk neutral conduction, whereas V_{th1} and V_{th2} correspond to the threshold voltages of the side gates and top gate, respectively. The correct extraction of the flat-band voltage has been confirmed with numerical simulations of the holes density distribution. Experimental measurements of p-type JLTs with variable being the fin width indicate that the threshold voltages V_{th1} and V_{th2} are due to the different interface states density at the side and top gates.

Keywords:
Junctionless transistors
p-type triple-gate transistors
Multiple threshold voltages
Numerical simulations
Interface states

1. Introduction

Triple-gate junctionless transistors (JLTs) have been considered as promising devices to extend the scaling limit to lower channel lengths, avoiding ultra-high doping concentration gradients at the source/drain junctions [1]. Compared to the inversion mode triple-gate transistors, JLTs offer lower off-state current, near ideal subthreshold slope and less mobility degradation with gate voltage [1]. In a recent work, it has been suggested that the triple-gate architecture in JLTs exhibits corner effects in spite of the bulk neutral conduction mechanism [2]. The corner effects have been extensively studied by three-dimensional device simulations in inversion mode triple-gate transistors by several groups [3-9]. Due to local increase of the electron density at the corners of the fin, independent channels located at the fin corners are activated at different gate voltages. As a result, the transconductance derivative (dg_m/dV_g) method revealed that the triple-gate inversion mode transistors can present more than one threshold voltages, which becomes a serious technological problem [7]. In inversion mode triple-gate transistors, due to the corner effects the channels located next to the top and bottom corners of the fin have lower threshold voltages compared to the sidewall gates [7].

The operation of JLTs present the special feature of involving two conduction regimes, such as bulk neutral channel and surface accumulation layer, separated by the flat-band voltage V_{fb}. In n-type JLTs, the threshold voltage has been investigated experimentally using the dg_m/dV_g method in devices with a planar structure (fin width W_{fin} = 10 µm) [10,11]. Two peaks were observed in the dg_m/dV_g versus V_g plot, with the first (lower) representing the bulk conduction threshold voltage V_{th} and the second (higher) the flat band voltage V_{fb}. A methodology to separate the surface accumulation and bulk conduction in n-type JLTs with single threshold voltage has been proposed by using the standard Y-function method to extract the bulk and accumulation low-field mobility [11]. Furthermore, the impact of the source-drain series resistance R_{sd} on the dg_m/dV_g versus V_g plot has been highlighted in planar n-type JLTs, suggesting a method to eliminate the R_{sd} effect for extracting the parameters V_{th} and V_{fb} [12]. Last years, the electrical properties, the dynamic response, the effect of crystallographic orientations and reliability issues in p-type triple-gate JLTs have been studied extensively [13-17]. Furthermore, using the threshold voltage extracted with the g_m/I_d method [18], a new method for extraction of the n-type JLT parameters (flat-band voltage, fin width and doping concentration) has been proposed [19].

In this article, with careful multiple-peak fit analysis of the experimental dg_m/dV_g versus V_g plots derived after eliminating the effect of series resistance, the threshold voltage V_{th} of rectangular cross-section p-type triple-gate JLTs is studied in terms of the channel length. In contrast to planar n-type JLTs of low series resistance exhibiting two peaks corresponding to the conduction threshold voltage and flat-band voltage [12], in all rectangular p-type triple gate JLTs of high series resistance the intrinsic dg_m/dV_g versus V_g plots exhibit three peaks, highlighting the presence of the flat-band voltage and two conduction threshold voltages within the partial depletion region. The impact of the series resistance and short-channel effects on the dg_m/dV_g behavior for extracting the threshold voltage and flat-band voltage in p-type JLTs is discussed. Multiple threshold voltages are a technological problem causing difficulties in separating surface accumulation and bulk conduction and complexity in compact modeling. However, multiple threshold voltages in rectangular p-type JLTs has never been observed so far. The origin of the two conduction threshold voltages is clarified by numerical simulation and experimental results of p-type JLTs with rectangular cross-section.

2. Experimental details

The measured single p-type JLTs were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) [20]. After thinning the Si body down to about 10 nm, a full-sheet implantation was carried out before active patterning with a boron doping targeted at about 2×10^{19} cm^{-3}. The high-k-metal gate stack is composed of HfSiON/TiN/p^+-polysilicon, with equivalent oxide

thickness of 1.2 nm, and the TiN metal gate used features a work function close to mid-gap. Using a nitride spacer on the sidewalls of the gate, an additional implantation was performed to source/drain regions in order to improve electrical performance by reducing access resistance, resulting in source/drain doping level about 10^{20} cm^{-3}. The implantation process can give rise to an increased number of interface states at the gate oxide-Si interface, which in turn may cause increase in threshold voltage, reduction in transconductance and increase in leakage current. Previous investigation has shown that for a certain substrate dopant concentration, the Si-SiO_2 interface state density is much higher in boron-implanted silicon than in phosphorus-implanted silicon [21]. This difference in interface state density has been attributed to a higher strain in boron-implanted silicon, due to a larger lattice mismatch caused by the smaller boron atoms, explaining the low series resistance in n-type JLTs [12]. In the investigated devices of rectangular cross-section, the channel length L is varying from 25 to 95 nm, with fixed fin height H_{fin} = 10 nm and fin width W_{fin} = 26 nm. The impact of the fin width on the performance behavior has been investigated in p-type JLTs with rectangular cross-section, composed of an array of 50 parallel nanowires with doping concentration 2×10^{19} cm^{-3}, channel length L = 10 μm, fin height H_{fin} = 10 nm and fin widths W_{fin} = 20, 40 and 190 nm.

Three-dimensional numerical simulations of a long channel device (L=95nm) were performed, using the Silvaco (Atlas) simulation tool, using the models of band-gap narrowing, Shockley-Read-Hall generation-recombination and field-dependent mobility. Quantum confinement effects were not considered, since these effects become significant when the silicon thickness is less than 10 nm [22].

3. Results and discussion

Fig. 1(a) shows the transfer characteristics (I_d-V_g) at drain voltage V_d = -0.03 and -1 V of a p-type JNT with L = 95 nm, H_{gin} = 10 nm and W_{fin} = 26 nm. The drain induced barrier lowering (DIBL), defined as the difference between the gate voltages at constant drain current $I_d = 10^{-7}$ A/μm divided by ΔV_d between V_d = -0.03 V and V_d = -1 V, is -0.02 V/V. The low DIBL parameter indicates negligible short channel effects. For accurate extraction of the series resistance R_{sd} of the triple gate JLTs, an extraction method based on the total resistance $R_{tot} = V_d/I_{d,tot}$, measured at V_d = -30 mV in the accumulation regime, has been applied [23]. The total resistance, defined as the sum of the channel resistance and series resistance, is given by [23]:

$$R_{tot} = \left[1 + \theta\left(V_g - V_{fb}\right)\right]\sqrt{\frac{V_d L}{\mu C_{ox}}}\frac{\sqrt{g_m}}{I_d} + R_{sd} \ , \qquad (1)$$

where θ is the mobility degradation factor, μ is the carrier mobility and C_{ox} is the gate capacitance per unit of length. Considering that the inverse Y-function $g_m^{1/2}/I_d$ is R_{sd} independent, the curve of R_{tot} as a function of $g_m^{1/2}/I_d$ can be approximated by a straight line, the intercept of which with the vertical axis gives the series resistance. The accuracy of the series resistance extraction method has been demonstrated through numerical simulations and experimental results [23]. The total resistance R_{tot} measured at V_d = -30 mV is plotted as a function of the inverse Y-function $g_m^{1/2}/I_d$ in Fig. 1(b). This curve is approximated by a straight line and the intercept with the vertical axis gives the series resistance R_{sd} = 18.15 kΩ. It is noticed that the commonly used method of exponential fitting in the R_{tot} versus gate voltage curve [24], the value of the obtained R_{sd} is strongly dependent on the analyzed voltage range. Furthermore, the transfer length method (TLM) for extracting the series resistance is not used, since non-ideal ohmic contacts at the source and drain sides can result in severe device-to-device variability in series resistance.

It is worth noting that the measured series resistance of the p-type JNT is high in spite of the additional implantation in the extensions performed to reduce the access resistance. To understand the reason why the series resistance is high, we studied the effect of fin width on the device performance. Fig. 2 presents the transfer characteristics of p-type JLTs composed by 50 parallel nanowires with fixed channel length L = 10 μm, fin height H_{fin} = 10 nm and fin widths W_{fin} = 20, 40 and 190 nm,

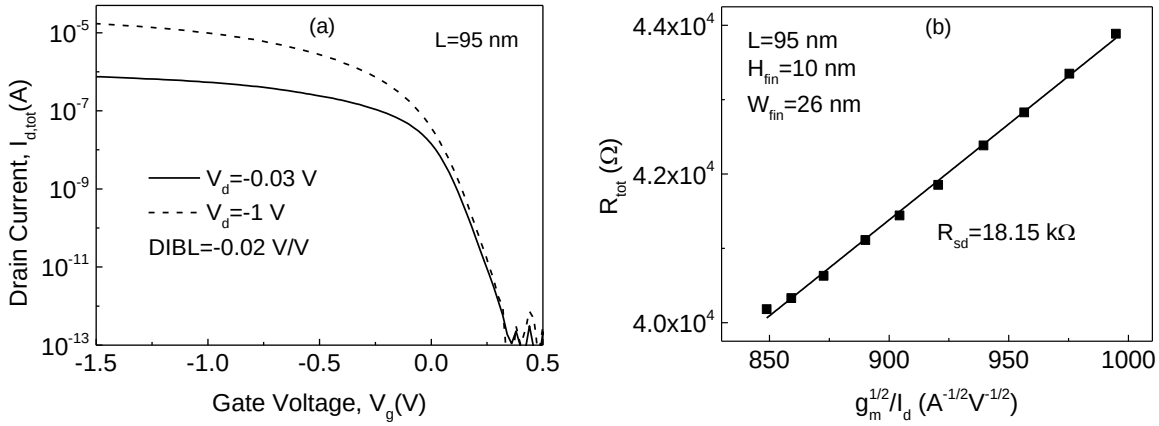


Fig. 1. (a) Measured drain current as a function of gate voltage of p-type triple gate JLT with fin height H_{fin} = 10 nm, fin width W_{fin} = 26 nm and channel lengths L = 95 and 75 nm. (b) Total resistance R_{tot} as a function of the inverse Y-function $g_m^{1/2} / I_d$. The insets show the DIBL parameter and the series resistance R_{sd} of the transistors.

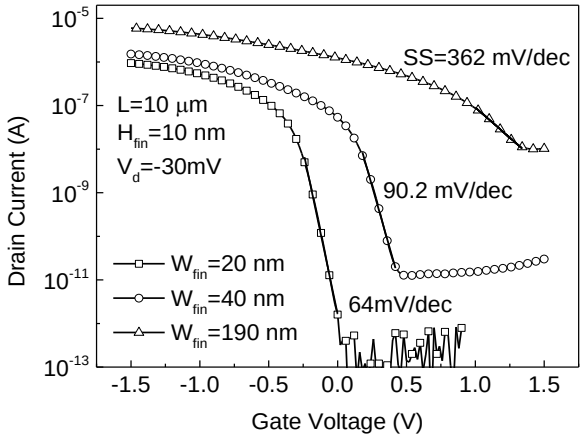


Fig. 2. Drain current as a function of gate voltage of p-type triple gate JLTs composed of an array of 50 parallel nanowires with channel length L = 10 μm, fin height H_{fin} = 10 nm and fin width W_{fin} = 20, 40 and 190 nm, measured at drain voltage V_d = -30 mV.

measured at drain voltage V_d = -30 mV. For the narrow fin device (W_{fin} = 20 nm) the subthreshold slope approaches the ideal value of 64 mV/dec, whereas for the wide fin device (W_{fin} = 190 nm) the subthreshold slope is strongly degraded to 362 mV/dec. Furthermore, the leakage current is increased dramatically with increasing W_{fin} from 20 to 190 nm These findings clearly indicate that the top gate interface is dominated by interface states of density much higher compared to that of the side gates interfaces. The high density of interface states can explain the high series resistance at the source and drain contacts. Moreover, the asymmetric distribution of the density of interface states is expected to cause different threshold voltages for the top and side gates, which can be represented by two peaks in the dg_m/dV_g versus V_g plots.

The threshold voltage V_{th} of the triple-gate JLTs was obtained using the transconductance derivative method at drain bias V_d = -30 mV [25]. For the JLT of Fig. 1, the as-measured derivative dg_m/dV_g as a function of V_g is plotted with dashed line in Fig. 2(a). Two peaks are distinguished in the as-measured dg_m/dV_g versus V_g characteristic of the JLT with L = 95 nm. The drain current corrected from the impact of R_{sd} was calculated from the relation [12]:

$$I_d = \left(\frac{V_d}{I_{d,tot}} - R_{sd} \right)^{-1} \times V_d \ , \qquad (2)$$

where $I_{d,tot}$ denotes the measured drain current.

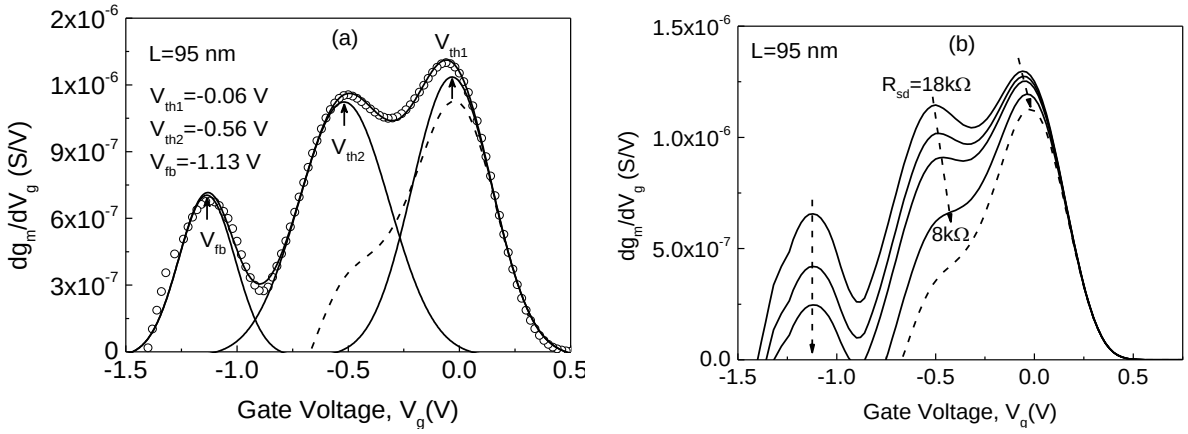


Fig. 3. (a) Plots of dg_m/dV_g versus V_g of the p-type triple gate JLT of Fig. 1(a)**.** The dashed line represents the as-measured dg_m/dV_g versus V_g curve, the symbols the R_{sd}-corrected experimental dg_m/dV_g versus V_g curve and the solid lines its decomposition into three Gaussian curves. (b) Effect of the series resistance R_{sd} on the behavior of dg_m/dV_g.

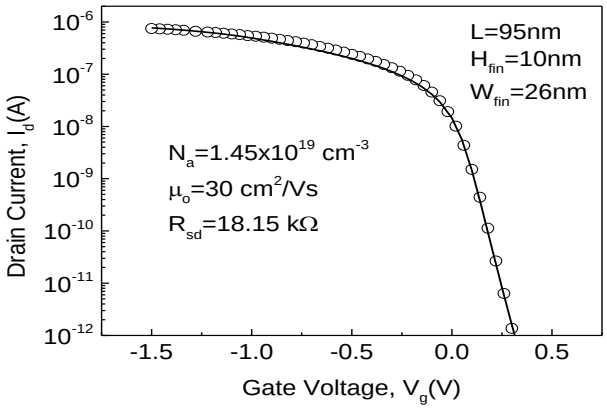
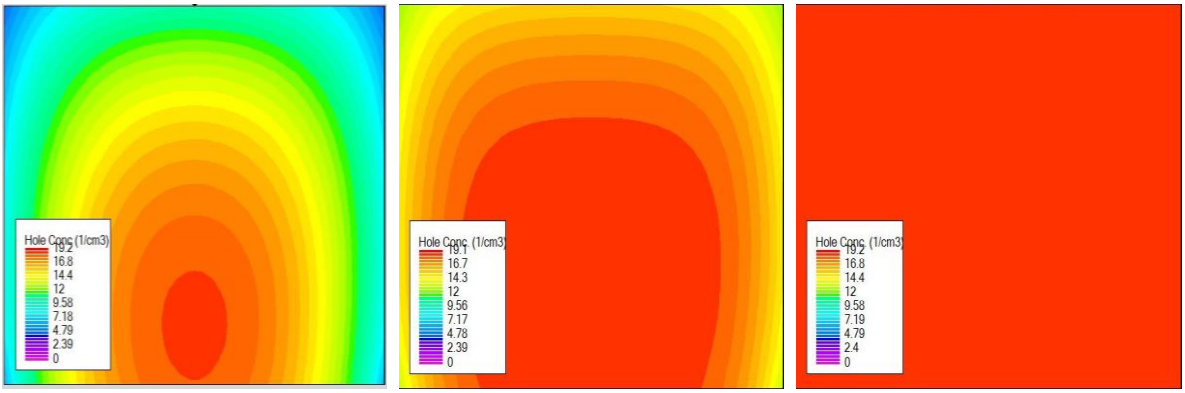


Fig. 4. Transfer characteristic at drain voltage V_d = -30 mV of the triple gate JLT of Fig. 1(a) with fin height H_{fin} = 10 nm, fin width W_{fin} = 26 nm and channel length L = 95 nm. The symbols represent the experimental data and the solid line the TCAD simulation data obtained using the parameters presented in the inset.

The intrinsic dg_m/dV_g versus V_g characteristic, obtained from the R_{sd}-corrected I_d of Fig. 1(a) at V_d = -30 mV is plotted with symbols in Fig. 3(a), together with its decomposition into three Gaussian curves, indicating that two independent channels located in different regions are activated at different gate voltages. The first and second peaks from right correspond to the conduction threshold voltages V_{th1} = -0.06 V and V_{th2} = -0.56 V separating the partial depletion from full depletion region, while the third peak corresponds to the flat-band voltage V_{fb} = -1.13 V, i.e. the threshold of the accumulation conduction channel. The observed two threshold voltages within the partial depletion region of the p-type JLT can be attributed to the asymmetric distribution of the interface states density of the side and top gates. The effect of R_{sd} on the dg_m/dV_g behavior is shown in Fig. 3(b). As the series resistance is reduced from 18 to 8 kΩ, the peak corresponding to V_{th2} is more reduced compared to that of V_{th1} with simultaneous shift to higher values, whereas the peak of V_{fb} is completely vanished. Therefore, as the series resistance seriously affects the dg_m/dV_g versus V_g plots, the value of R_{sd} in Eq. (2) is critical to reveal the peak corresponding to V_{fb} and for accurate extraction of the parameters V_{th1} and V_{th2}.

To clarify further the physical origin of the conduction threshold voltages V_{th1} and V_{th2} within the partial depletion region and verify the obtained flat band-band voltage V_{fb}, the distribution of the holes density has been determined with numerical simulations. The simulated transfer characteristic of the p-type JLT with L = 95 nm , H_{fin} = 10 nm and W_{fin} = 26 nm is presented in Fig. 4, reproducing with



(a) (b) (c)

Fig. 5. Hole density distributions at drain voltage V_d = -30 mV and gate voltages (a) $V_g = V_{th1}$ = -0.06 V, (b) $V_g = V_{th2}$ = -0.56 V and (c) $V_g = V_{fb}$ = -1.13 V in the middle of the channel of the rectangular p-type triple gate JLT with dimensions: L = 95 nm, H_{fin} = 10 nm and W_{fin} = 26 nm. The insets show the logarithm of the holes concentration distributions.

good accuracy the experimental transfer characteristic using the extracted series resistance of R_{sd} = 18.15 kΩ, doping concentration $N_A = 1.45\times10^{19}$ cm^{-3} and low field mobility μ_0 = 30 $cm^2/V\cdot s$. After calibration of the simulation tool, the distributions of the hole density in the middle of the channel when the devices is operated at drain bias voltage V_d = -30 mV and gate voltages $V_g = V_{th1}$ = -0.06 V, $V_g = V_{th2}$ = -0.56 V and $V_g = V_{fb}$ = -1.13 V were obtained as presented in Fig. 5. In Fig. 5(a), a depletion of the holes density in the upper corners of the fin is observed, indicating the absence of the corner effects due to the unique volume conduction in JLTs, in contrast with the inversion mode triple gate MOSFETs [2-8].

As shown in Fig. 5(a), at $V_g = V_{th1}$ = -0.06 V the holes conduction path is located in the middle of the channel and close to the interface with BOX as in double gate (DG) JLTs [26], indicating that the threshold voltage V_{th1} is due to the side gates. For gate voltage above V_{th1}, the holes conduction path is extended closer to the top of the channel, indicating that the threshold voltage V_{th2} is due to the top gate. The conclusion for the origin of V_{th1} and V_{th2} derived from the hole density distribution at different gate voltages is consistent with the finding of the asymmetric distribution of interface states at the side and top gates. At gate voltage V_g = -1.13 V, the whole channel becomes neutral with hole density equal to the doping density N_A and the current flows through the entire channel [Fig. 5(c)]. Therefore, numerical simulations show that the gate voltage of V_g = -1.13 V corresponds to the flat-band voltage V_{fb}, which is in agreement with the flat-band voltage extracted experimentally in Fig. 3(a) after correcting the drain current from the impact of series resistance R_{sd}.

For p-type JLTs with channel length varying from 75 to 25 nm, the as-measured and the intrinsic dg_m/dV_g versus V_g characteristics obtained after correcting the drain current from the impact of R_{sd}, together with their decomposition into Gaussian curves are presented in Fig. 6. The insets of Figs. 6(a)-6(d) present the series resistance R_{sd} and DIBL parameter of the JLTs. The short channel effects become stronger with decreasing the channel length, whereas the series resistance varies lying in the range of about 11-27 kΩ. In all cases, after careful multiple-peak fit analysis of the intrinsic dg_m/dV_g versus V_g curves, three clear peaks are observed corresponding to the two threshold voltages V_{th1} and V_{th2} and the flat-band voltage V_{fb}. These results suggest that in the investigated p-type JLTs, the high series resistance affects the dg_m/dV_g behavior more than short-channel effects. In contrast, in n-type JLTs exhibiting low series resistance, in short-channel devices the short-channel effects affect the dg_m/dV_g behavior more than the R_{sd} effects [12]. The extracted device parameters V_{th1}, V_{th2} and V_{fb} as a function of the channel length are presented in Fig. 7. In the JLTs of the studied technology, high

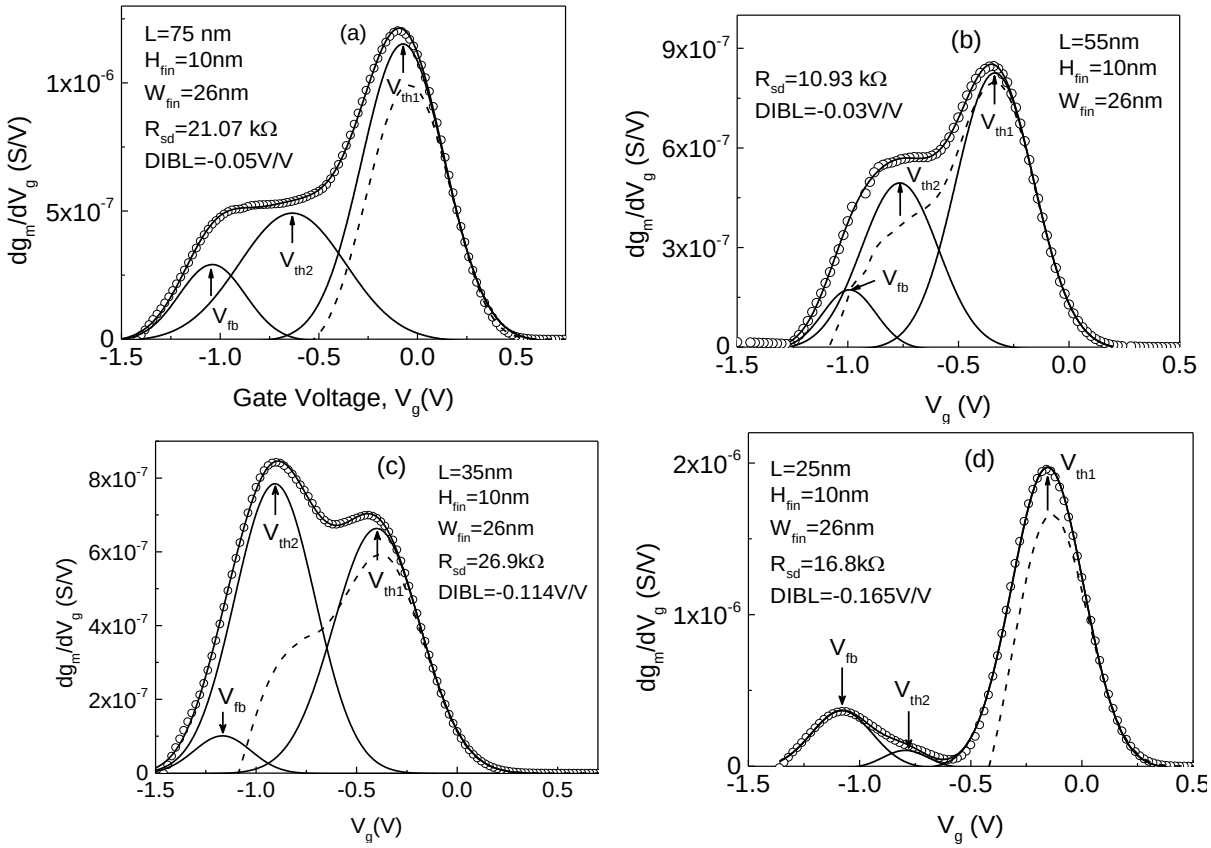


Fig. 6 Measured plots of dg_m/dV_g versus V_g in p-type triple gate JLTs with fin height H_{fin} = 10 nm, fin width W_{fin} = 26 nm and channel lengths L = 75, 55, 35 and 25 nm. The dashed lines represent the as-measured dg_m/dV_g versus V_g curves and the solid lines their decomposition into three Gaussian curves.

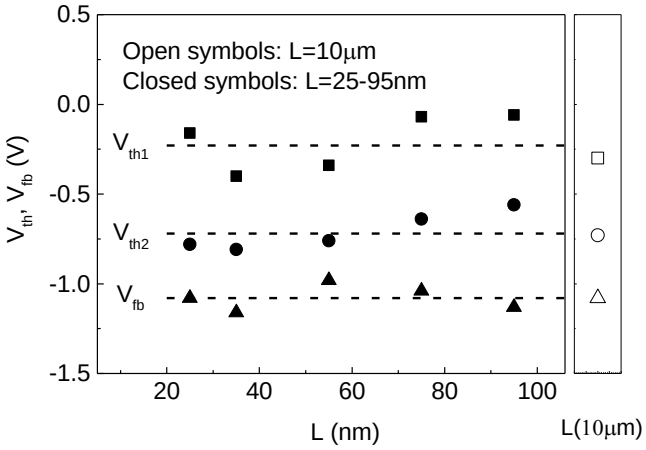


Fig. 7. Extracted experimental parameters V_{th1}, V_{th2} and V_{fb} as a function of channel length L of isolated p-type triple gate JLTs with fin height H_{fin} = 10 nm and fin width W_{fin} = 26 nm. For comparison, the extracted parameters V_{th1}, V_{th2} and V_{fb} of a typical array of 50 parallel p-type triple gate JLTs with fin height H_{fin} = 10 nm and fin width W_{fin} = 20 nm and channel length L = 10 μm are also presented.

series resistance effects affect the dg_m/dV_g behavior more than short-channel effects. Indeed, the threshold voltages V_{th1} and V_{th2} remain almost invariable with the channel length varying from 25 nm to 10 μm as shown in Fig. 7.

4. Conclusion

Detailed experimental study of the threshold voltage in rectangular p-type triple-gate JLTs was carried out using the transconductance derivative method. In devices with channel length varying from 95 to 25 nm, after correcting the drain current from the impact of series resistance, multiple-peak fit analysis of the intrinsic dg_m/dV_g versus V_g curves present three peaks corresponding to the two conduction threshold voltages V_{th1} and V_{th2} and flat-band voltage V_{fb}. The effect of series resistance on the dg_m/dV_g behavior is highlighted. In contrast to n-type JLTs of low series resistance, in the investigated p-type JLTs the high series resistance affects the dg_m/dV_g behavior stronger than the short-channel effects. Numerical simulations of the holes density distribution reveal the absence of corner effects in p-type triple-gate JLTs due to the unique bulk neutral conduction, whereas V_{th1} and V_{th2} correspond to the threshold voltages of the top gate and side gates, respectively. The correct extraction of flat-band voltage is verified with numerical simulation of the holes density distribution at different gates voltages. Numerical simulations and experimental results of p-type JLTs with variable being the fin width indicate that the observed threshold voltages V_{th1} and V_{th2} are correlated with the different density of interface states at the side gates and top gate, respectively. The overall results show that the two threshold voltages in p-type JLTs can be avoided by reducing the implantation process-induced density of top and side gates interface states.

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