Integrated Technology in SiC for Harsh Environement Power Electronics, Sensors and Quantum Nanophotonics

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SiC – one of the most technologically advanced wide bandgap semiconductor

	Eg (eV)	ε_r	μ_n ($cm^2.V^{-1}.s^{-1}$)	μ_p ($cm^2.V^{-1}.s^{-1}$)	E_c ($MV.cm^{-1}$)	ν_{sat} ($10^7 cm.s^{-1}$)	λ ($W.cm^{-1}.K^{-1}$)
Si	1,1	11,8	1450	500	0,2-0,8	1	1,5
2H-GaN	3,39	9	900	350	3,3	2,5	1,3
GaAs	1,42	12,9	8000	400	0,4-0,9	0,7	0,46
3C-SiC	2,2	9,6	900	45	1,2	2	4,5
6H-SiC	3	9,7	370	90	2,4	2	4,5
4H-SiC	3,26	10	600	115	2	2	4,5
Diamond	5,45	5,5	1900	3800	5,6	2,7	20

Electronic fields:

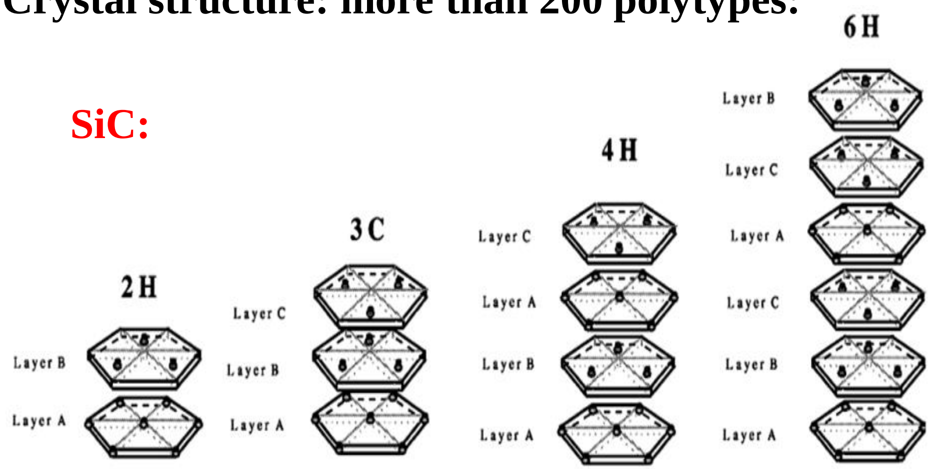
- High temperature
- High power
- Compact systems
- Low switching losses
- High-frequency

Harsh environnement

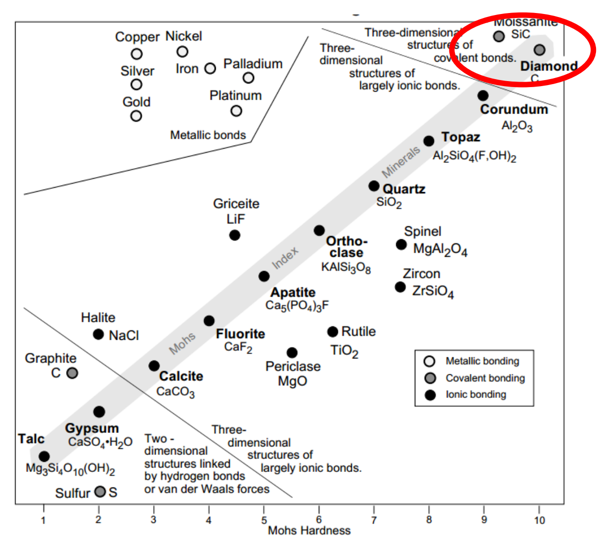
- Strong interatomic bonding
- High chemical inertness
- Good bio-compatibility

Crystal structure: more than 200 polytypes:

SiC:

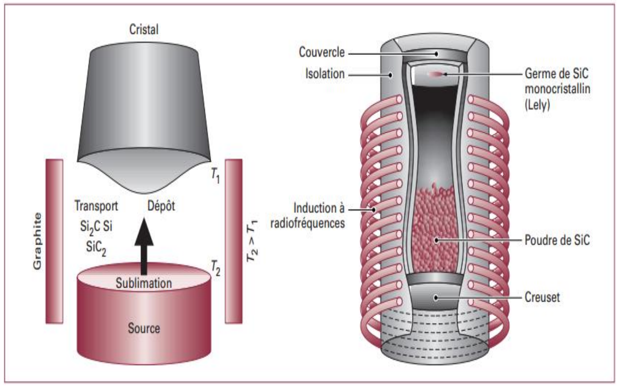


Hardness (Mohs scale)

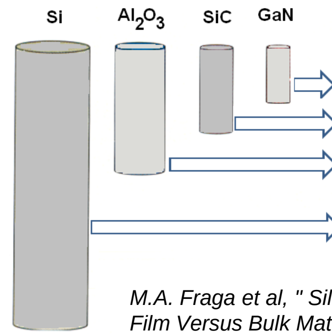


Particular and complex processes for the growth and technology

"ingot growth" SiC~2000°C (without liquid phase)



Considerable « cost »

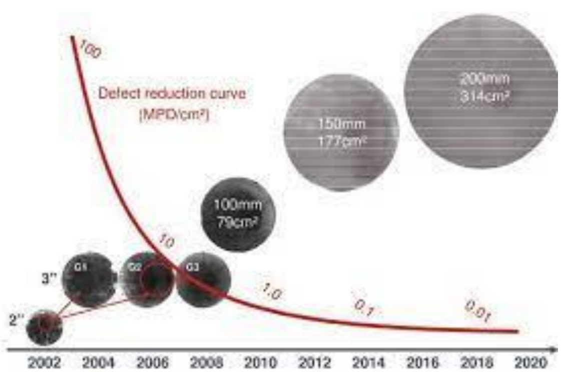


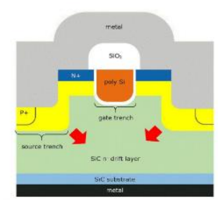
Wafers per ingot	Wafer price
< 10	x 100
< 50	x 30
< 100	x 10
>100	x 1

M.A. Fraga et al, " Silicon Carbide in Microsystem Technology - Thin Film Versus Bulk Material", 2015, INTECH Ed

But remarkable industrial investments in power electronics over the last decades:

- **continuous progress in reduction of defect densities,**
- **increase of wafer size**
- **and lowering of wafers costs.**





MOSFET in SiC

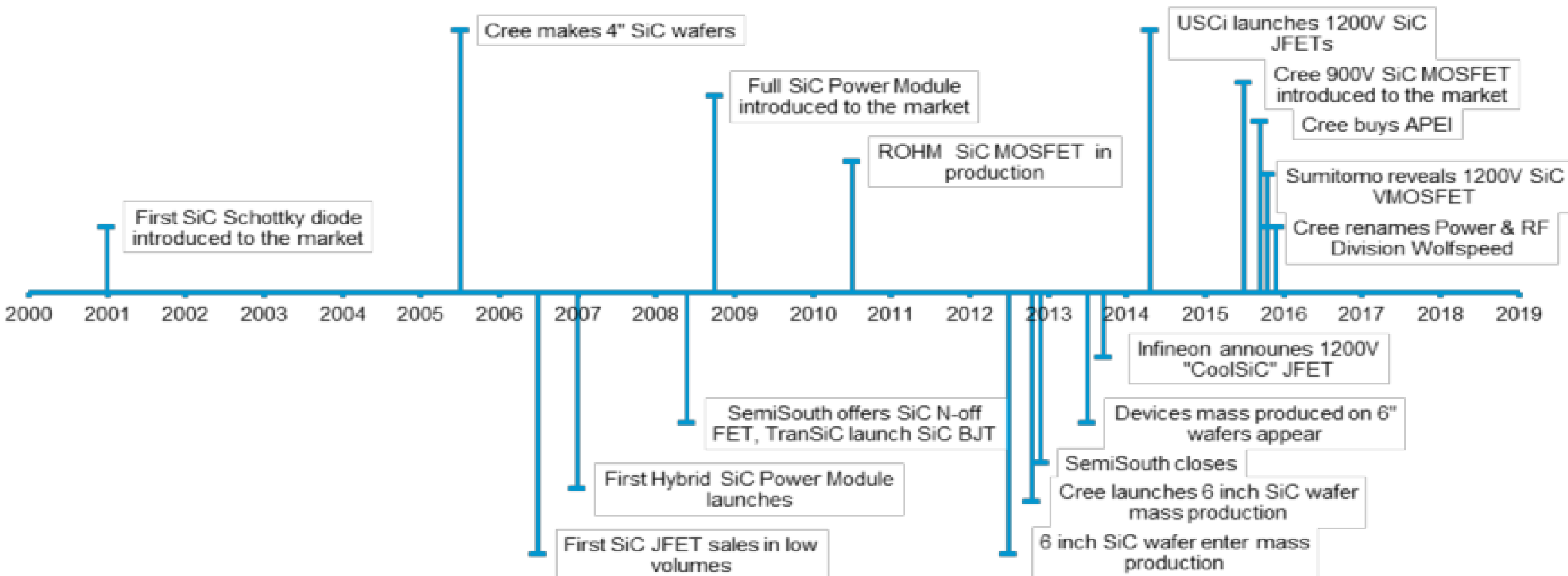
ROHM SEMICONDUCTOR

Wolfspeed. A CREE COMPANY

infineon

Power discrete SiC devices already commercialized (Farnell…)

Main industrial developments in recent years for the manufacture of power devices in SiC (4H-SiC)



Critical technological steps to develop (power) devices in SiC:

- Improve the quality of the SiC substrate:
  - decrease the density of the point and extended defects: "micropipes" , dislocations ;
  - increasing the wafer size – to fit with Si technological compatibility.

- Doping: a fundamental step to create active layers
  - mainly by ion implantation ;
  - needing high temperature annealing ~1700°to recover the crystal crystallinity and to activate the doping ;
  - avoiding Si sublimation and thus a doping loss by SiC etching ;
  - use a C-cap to encapsulate the substrate.

- Packaging, surface and interface improvements:
  - MOS interface : SiO_2/SiC: decrease the interface trap density ;
  - develop a robust packaging to fully benefit from the SiC properties.

SiC technological developing today

Power electronics :

- Monolithic integration of SiC devices in the same single crystal wafer

- to improve reliability in power electronics,
- to reduce the size of converters,
- to improve the switching operation speed,
- to decrease the power loss.

- Increasing the breakdown voltage of the single discrete devices (~30 kV)

New emerging application fields:

- Quantic nanophotonics and robust optoelectronics

- Color centers in SiC–(near)IR emission at RT
- SiC white LED – without rare-earth metals.

- Harsh environment sensors

- neutron detectors, UV photodectors , bio – electrochemical sensors...

From end of 2018: a new techological line we develop for SiC 100/150 mm

Two platforms (clean-rooms):

- ESIEE (Paris Marne-la-Vallée): **proved Si 100/150 mm technology**
- Nano'Mat (Troyes/Reims) : **SiC specific and complementary machines**

Not only for power electronics but also for the new emerging fields:

- sensors with SCR, piezo, bio-electrochemical
- nanophotonics, optoelectronics, plasmonics

A technological transfer of know-how developed in Lyon (limited to 50mm).
Support from academic projects (ANR, Europe, Région GE…) and direct demand from industrial partners

UMR CNRS 9007

ESIEE Paris cleanrooms

650 m² in ISO 5 and ISO 7

120 equipments to cover fully and standard steps to fabricate µ-systems and µ-sensors :

- Thin films deposition, thermal oxidation, photolithography, wet and dry plasma etching, wet chemical cleaning, electroplating, wire-bonding, wafer cutting, back-end packaging.

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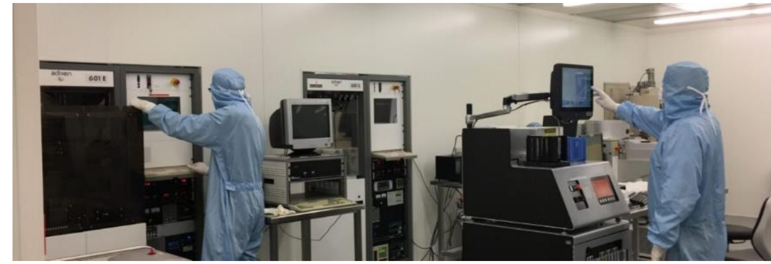

ESIEE Paris cleanrooms

Different technological lines :

- more classic (Si, glass, piezoelectric materials)
- more specifics (flexible systems with integrated carbonic materials: diamond, nanotubes, graphene).

Each equipment is compatible with:

- 4 inches wafers
- 2 to 8 inches for certain steps.
- not for parts or little samples!

Several industrial partners implanted in this cleanroom

ESIEE PARIS

Laboratoire ESYCOM

UMR CNRS 9007

For <u>SiC 100mm</u> technological line we validated:

- Wet chemical cleaning and etching
- UV lithography (positive and negative photoresist, double-side, lift-off)
- Thermal oxidation (dry and wet)
- Sputtering: Ni, TiW, Au, SiO_2 (metal contacts, plasma etching and ion implantation masks)
- LPCVD and PECVD with Si_3N_4
- Plasma etching (RIE et DRIE) to locally open thin films, dielectrics (up to ~2µm)
- Cutting SiC wafers with Disco DAD dicing saw

All these machines are currently used at ESIEE on 100mm silicon wafers <u>for academic and industrial projects</u>

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Lumière nanomatériaux nanotechnologies

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Specific and dedicated equipments for SiC (compatibles for 100mm)

- SiC ICP/RIE plasma etching
- Post-ion implantation annealing at high temperatures : AET RTP 1900°C furnace
- E-beam evaporators: Ni/Ti/Al (p-type contact) Si
- RTA annealing - JIPELEC JETFirst furnace, an equipment also present at URCA and that we frequently used
- E-beam lithographie (quantum technology)

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TROYES

UNIVERSITE DE REIMS
CHAMPAGNE-ARDENNE

At Nano'Mat we utilized less technological equipments but they are indispensable and represents key steps.

Physico-chemical characterizations : FEGSEM, AFM, KPFM, µRaman, PL…

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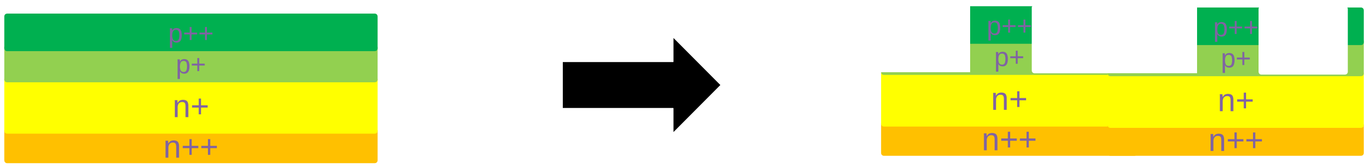
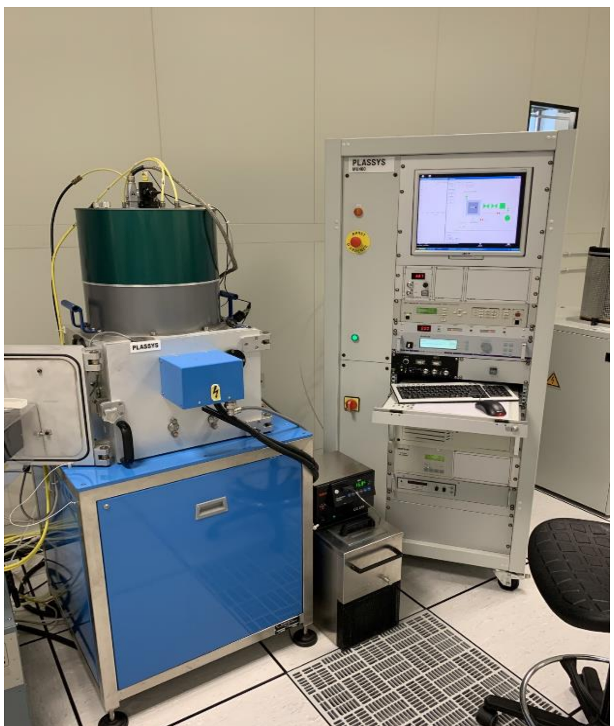
L2n – Nano-microfabrication of electronic devices in SiC

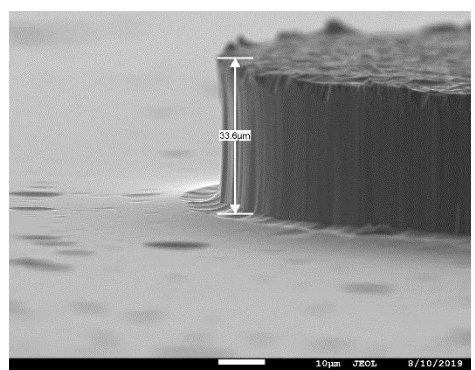
Local plasma etching of 4H-SiC layers



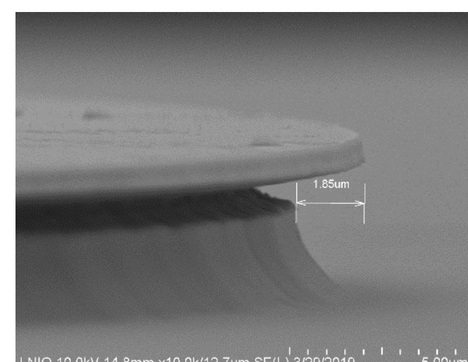


- ICP/RIE etching with SF_6
  → MU400 Plassys reactor

~35µm mesa and via

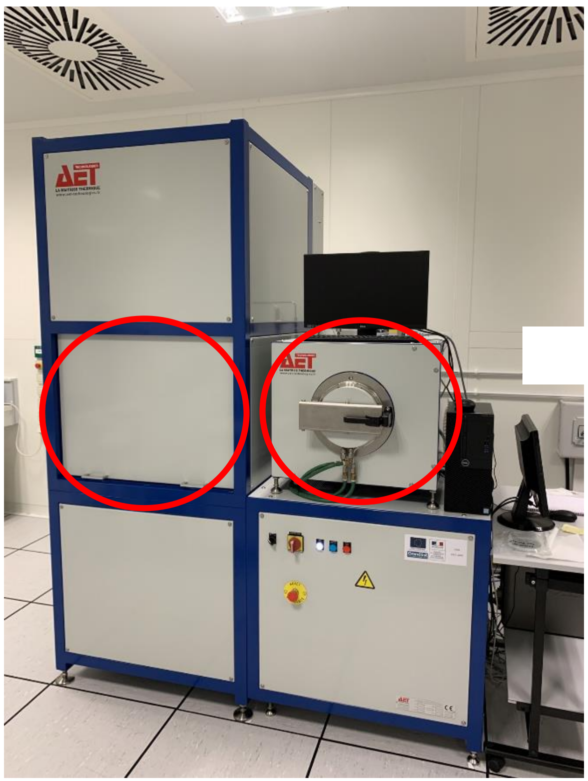


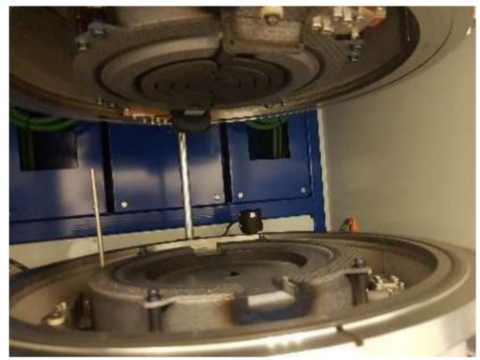
"isotropic" etching - ICP mode



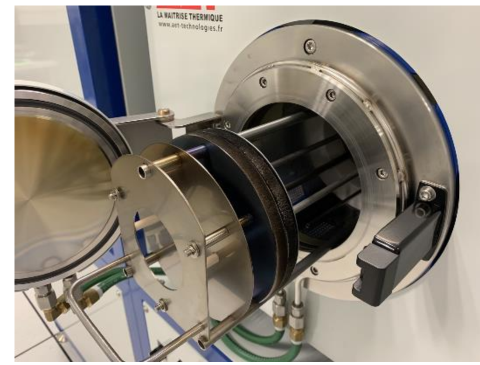
L2n – Nano-microfabrication of electronic devices in SiC

High temperature post –ion implantation annealing and recrystallisation of SiC thin layers

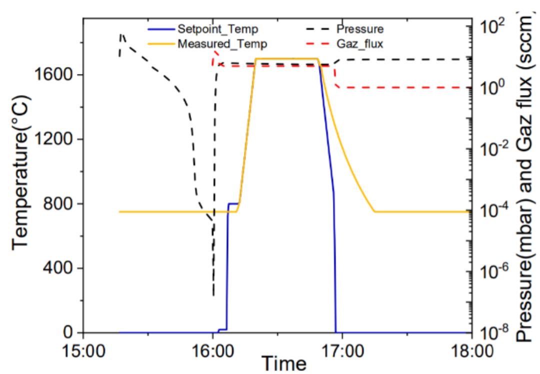




RTP



Pyrolyse



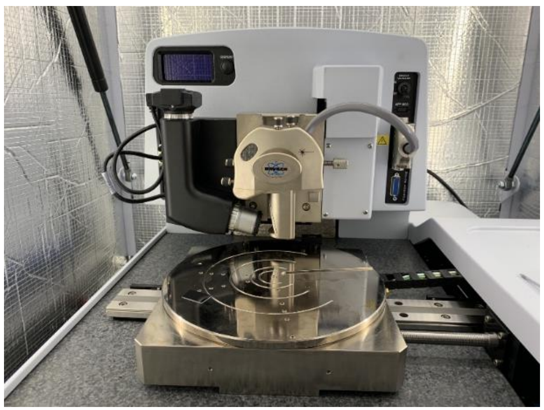
RTP pressure and temperature profiles under Ar with a plateau of 30min at 1700°C

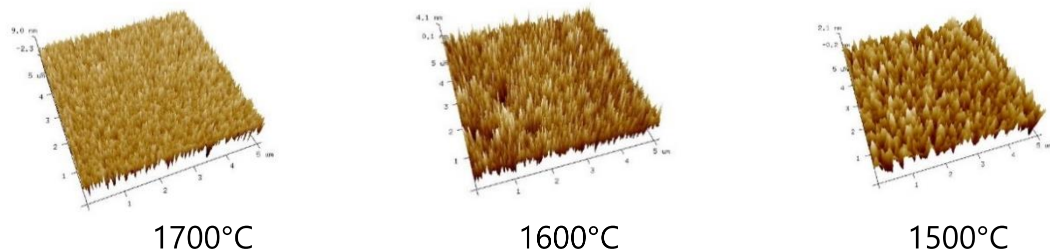
AET furnace

- RTP chamber with graphite resistors : heating temperature: 800 et 2000°C under Ar.
- More classic quartz tube chamber to form C-cap layer by pyrolyse : up to 900°C under Ar.

L2n – Nano-characterization of electronic devices in SiC

AFM/KPFM : Atomic/Kelvin Probe Force Microscopy

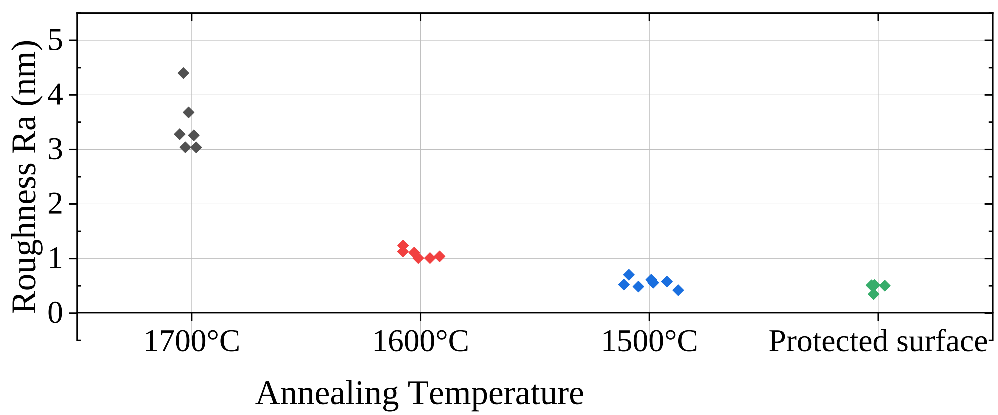




4H-SiC surface topography after annealing at different temperatures

Bruker's Dimension Icon Peak Force :

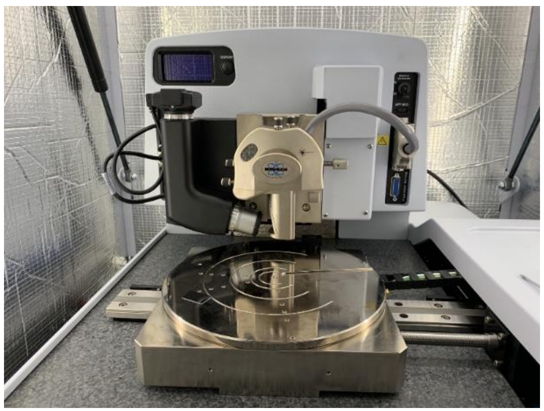
- SiC surface topography
- Roughness: AR layers control of light emission/absorption



4H-SiC roughness (Ra): control of the light emission/ absorption

L2n – Nano-characterization of electronic devices in SiC

AFM/KPFM : Atomic/Kelvin Probe Force Microscopy



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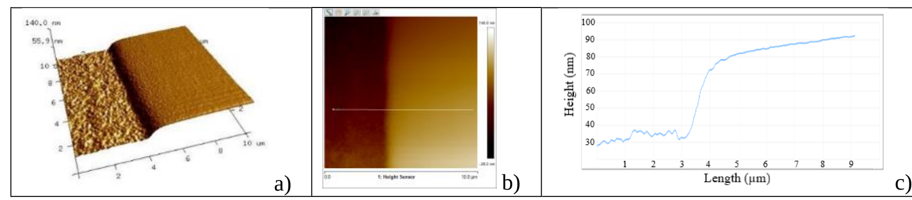
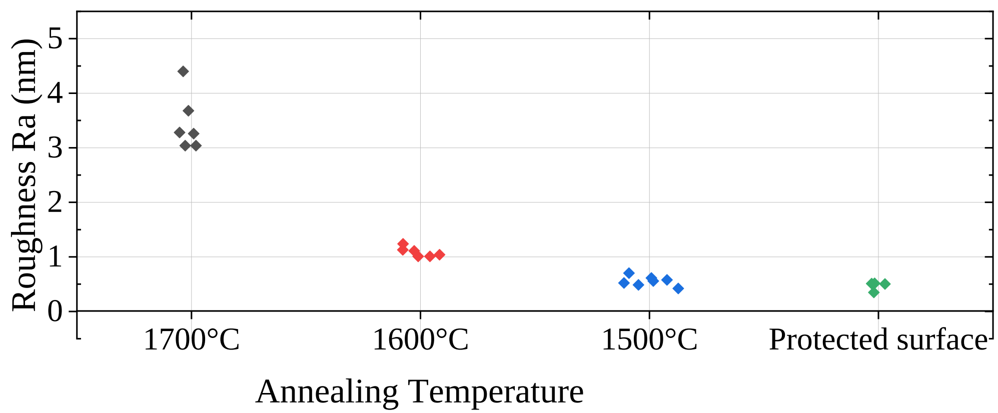


Protected area boundary patterned by photolithography after 1600°C annealing.



4H-SiC roughness (Ra): control of the light emission/ absorption

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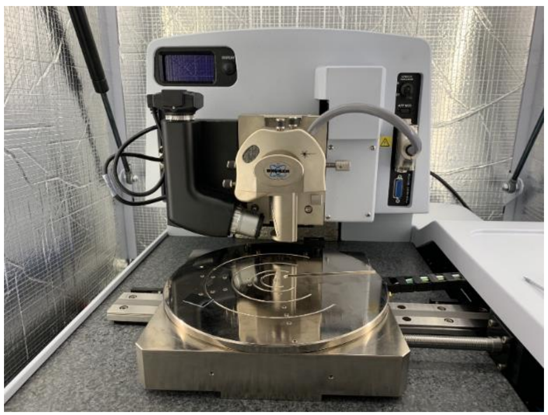
AFM/KPFM : Atomic/Kelvin Probe Force Microscopy

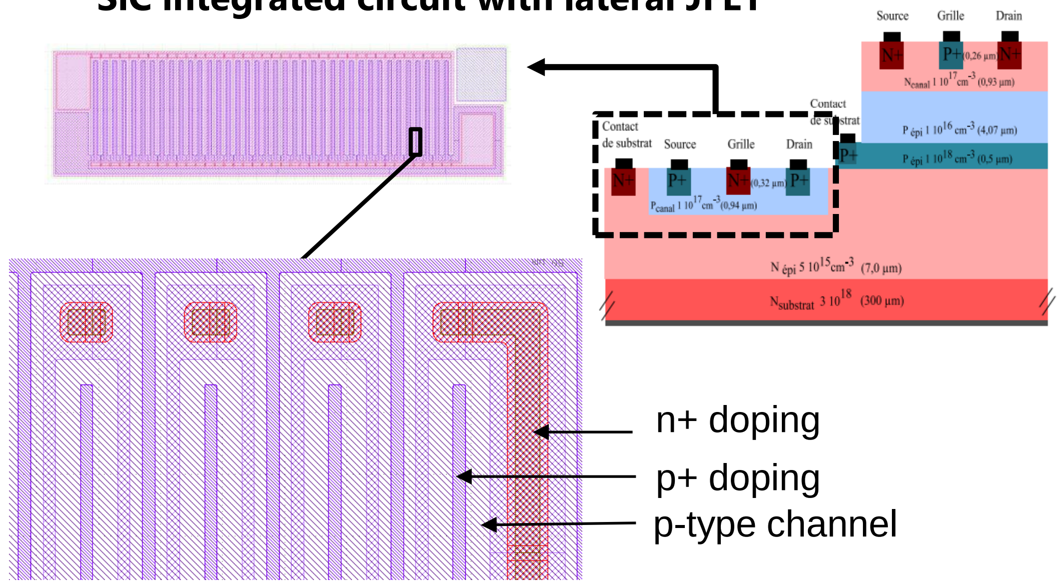


Bruker's Dimension Icon Peak Force :

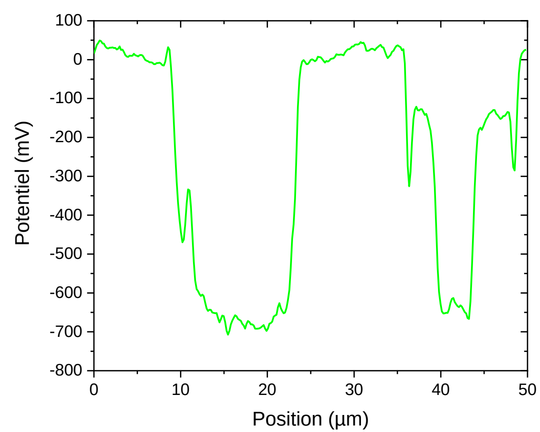
- SiC surface topography
- Roughness: AR layers control of light emission/absorption

→ KPFM – p/n junction cartography

SiC integrated circuit with lateral JFET



KPFM: surface **potential** microscopy (WF)



- p+ and n+ layers are identified from p-type channel
- A difference of 700mV between p and n-type layers
- Smooth surface topography (AFM – not shown)

L2n – Nano-characterization of electronic devices in SiC

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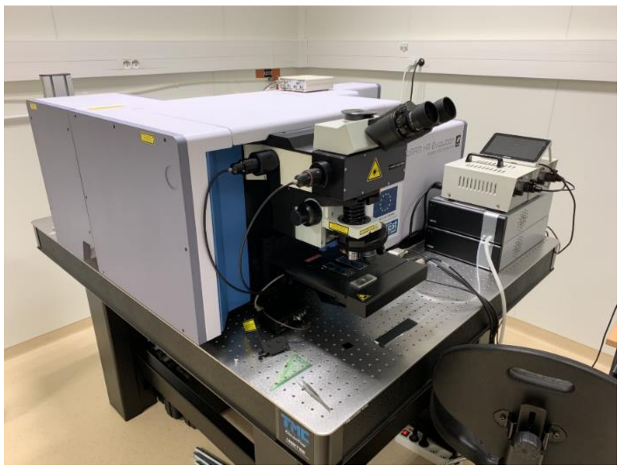
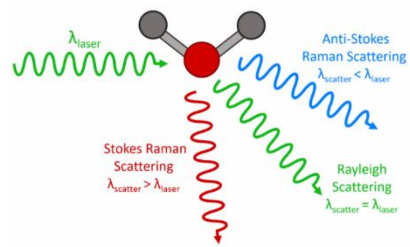
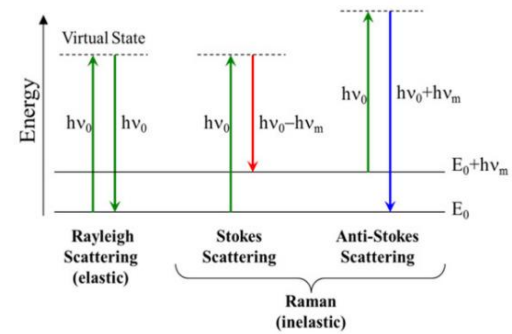
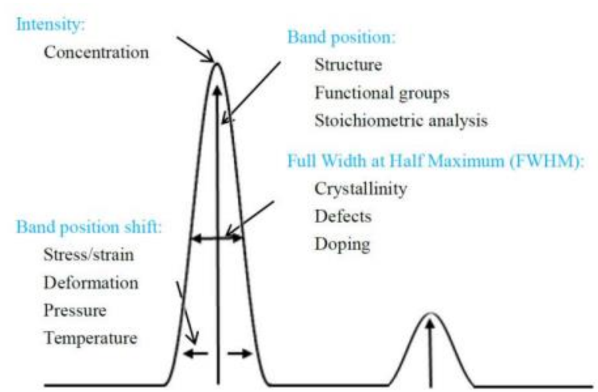
μ-Raman Microscopy





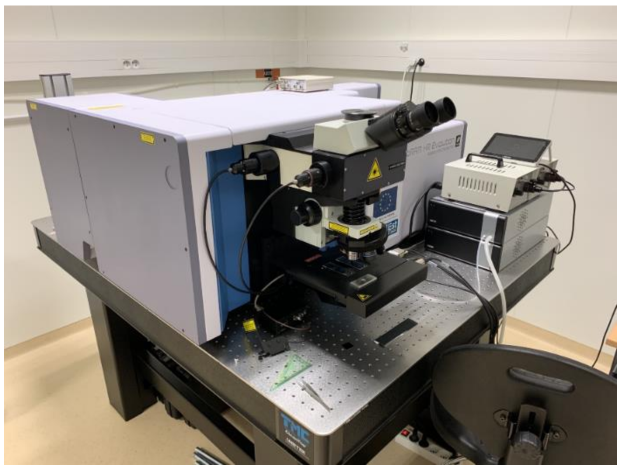


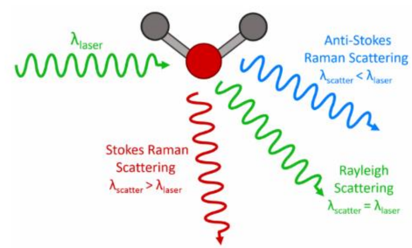


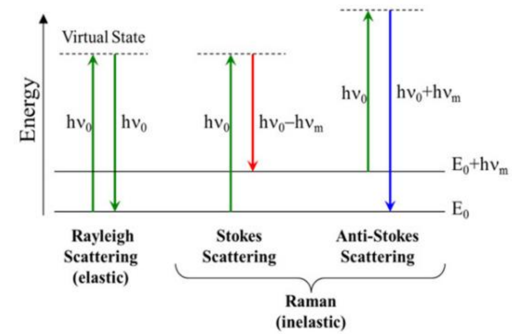
- SiC strong interatomic bonding
  → favourable for Raman scattering diffraction
- Raman very sensitive to crystal structure, polytype, defects, doping …
- PL also possible (from 320 to 1000nm)

L2n – Nano-characterization of electronic devices in SiC

µ-Raman Microscopy







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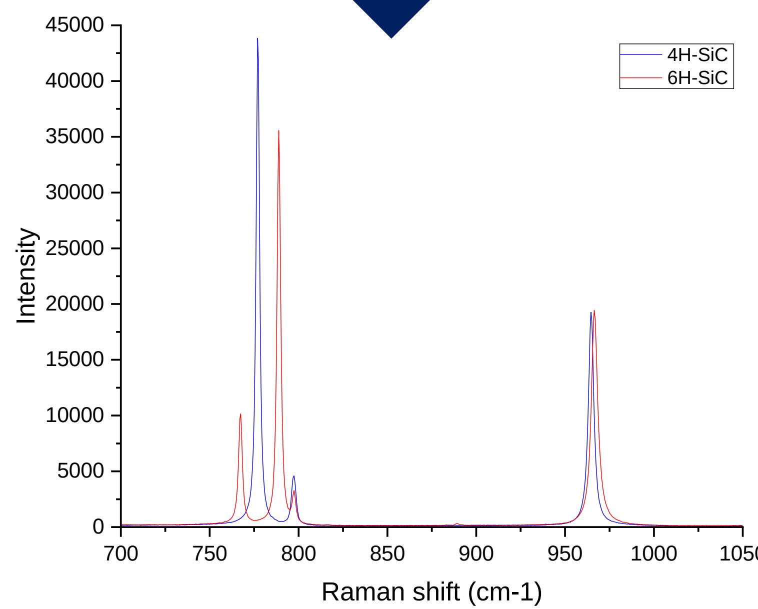
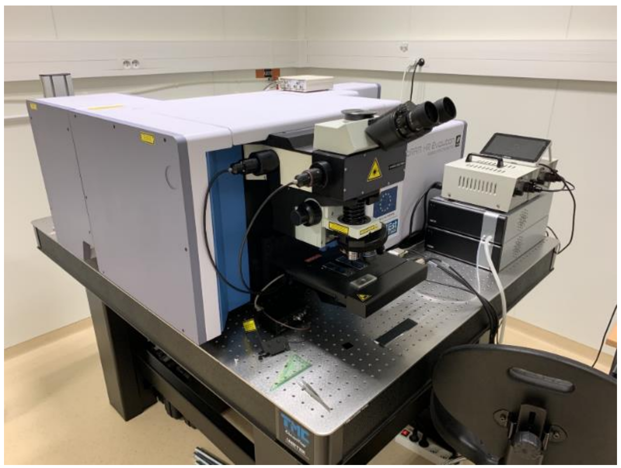
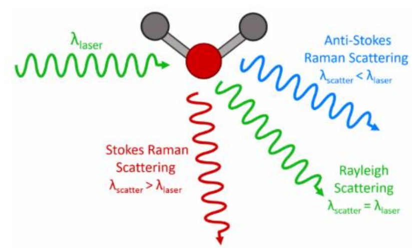
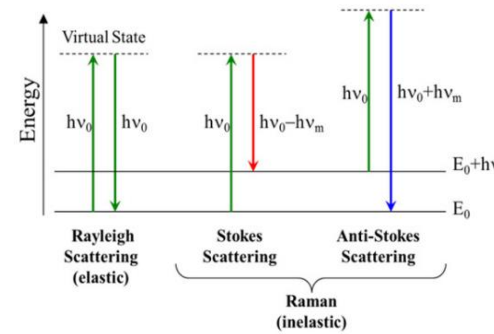


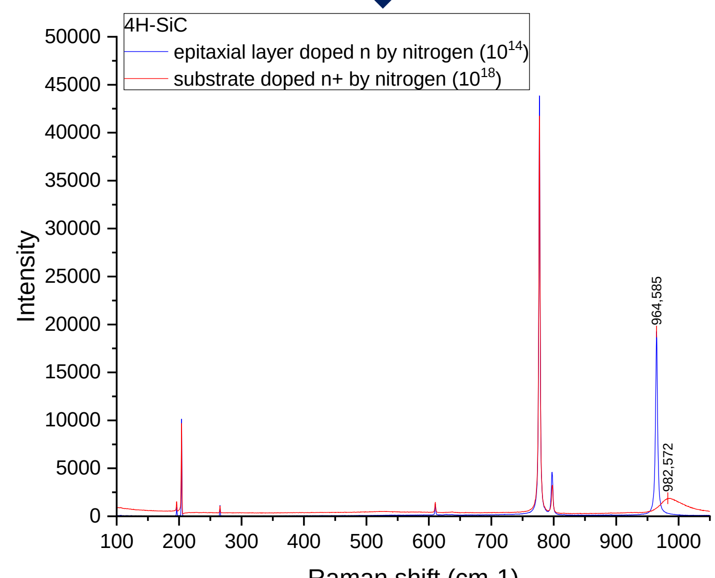
L2n – Nano-characterization of electronic devices in SiC

µ-Raman Microscopy









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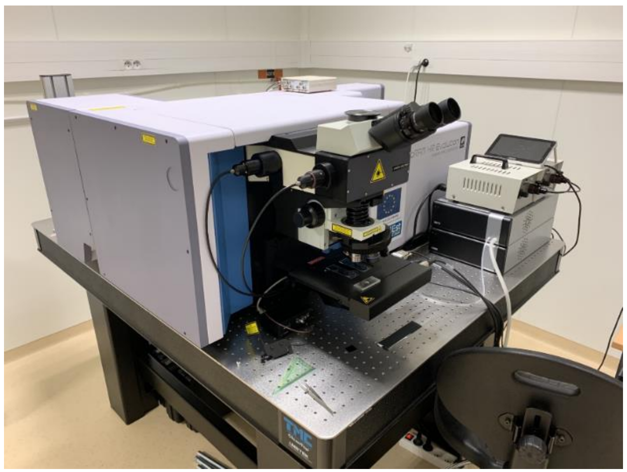
L2n – Nano-characterization of electronic devices in SiC

µ-Raman Microscopy



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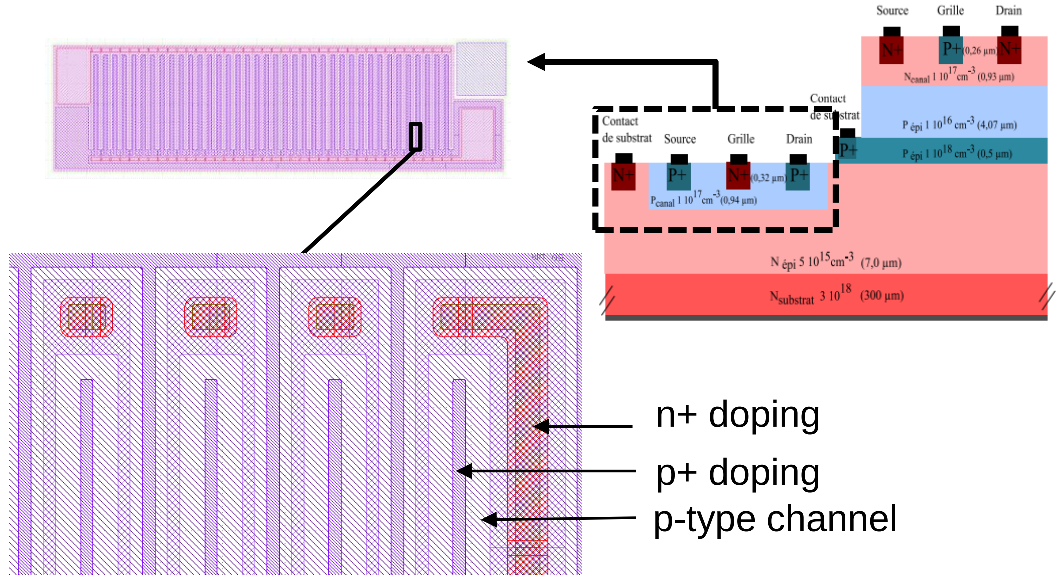
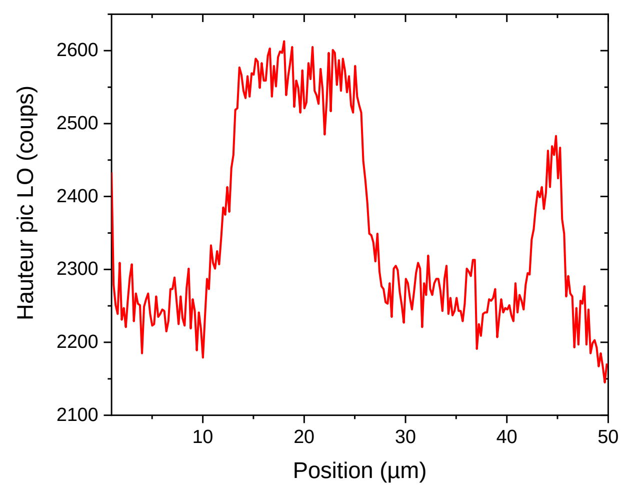


µ Raman scanning (in UV 325 nm)



- p and n+ are identified from from n- layers
- Complementary results compared to KPFM

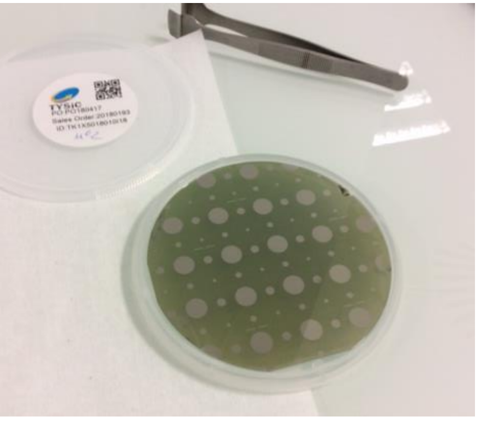
Implementation of a 100/150 mm SiC technological fabrication line

1) Progressively starting with little runs (end 2018 and beginning of 2019)

- to test the feasibility based on our past experience and by training if necessary on new equipment,
- technology transfer : Nanolyon (Lyon cleanroom 50mm) -> ESIEE/Nano'Mat,
- with the support of two engineering teams from the two research structure,s
- high number of trips/missions -> ESIEE Paris and also Lyon, Strasbourg, ISL…

Step validated during 2019 – industrial project NEDSiC (Magdala society)

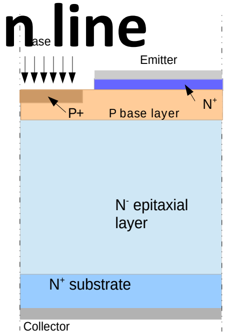
- neutron detectors in SiC,
- PiN structure with a large SCR (HPSI substrates),
- high precision (revers current extremely low – fA)
- 2 runs delivered,
- process-flow defined with critical technological steps validated for the future SiC projects.



SiC 100 mmm wafer processed:

A project set up and managed with the support of the UTT (50 k€)

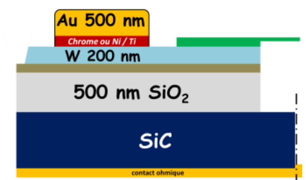
Implementation of a 100/150 mm SiC technological fabrication line



2) Shift to larger and more numerous projects

ANR HV-PhotoSW - High Voltage Photo-Switches

- CE05 (Une énergie durable, propre, sure et efficace)
- Ampère CNRS - Institut franco-allemand de recherches de Saint-Louis -NOVASIC S.A.
- 2019 – 2023 – 465 k€

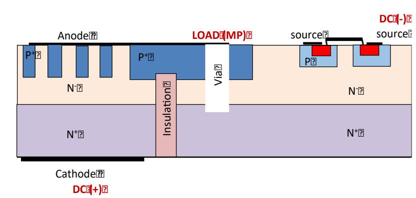


E**SACAT 2 – Cold cathodes fabrication on SiC**

- industrial project supported by Thales

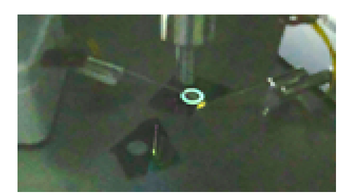
ANR MUS²IC - Monolithic Ultimate Switching cell in SIlicon Carbide

- CE05 (Une énergie durable, propre, sure et efficace)
- LAPLACE, LAAS, L2n, AMPERE
- 2022 - 2026 – 504 k€



Fabrication of LED (white and with color centers) in SiC

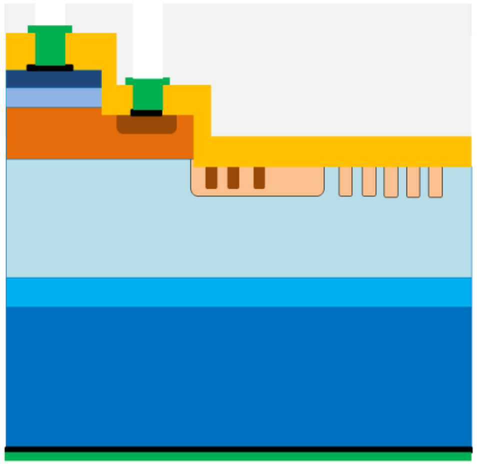
- SATT SAYENS, CNRS
- 2 patents: **FR2201067** and **FR2201064**

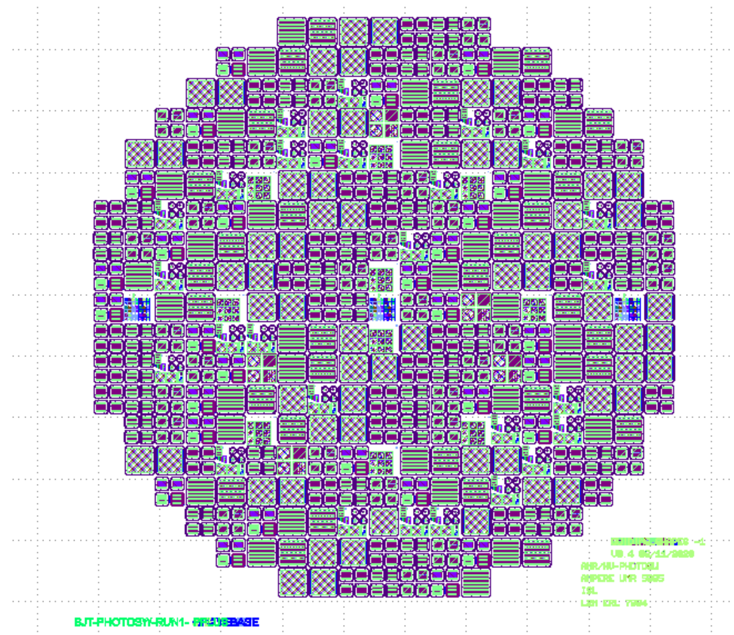


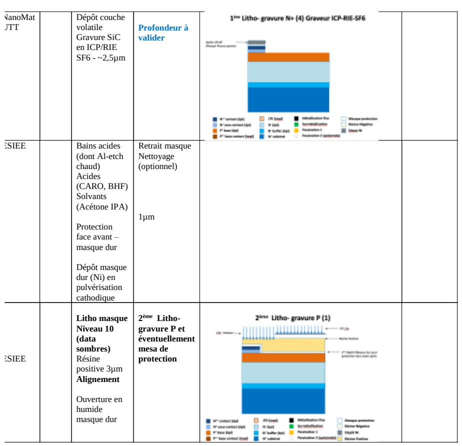
KRASiC – Région GE – ph-d student project Enora Vuillermet

- engineering of SiC defects (color centers) for luminescent devices

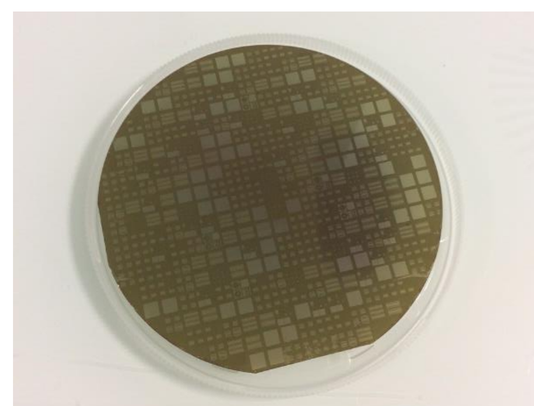
Process-flow HV-Photo SW: 11 mask levels, about one hundred steps



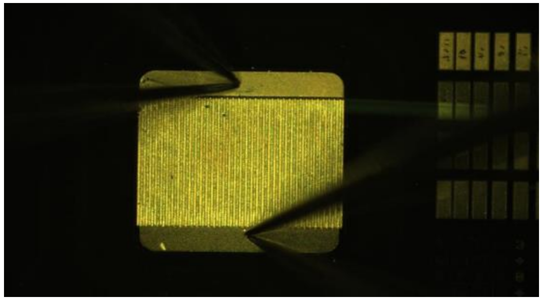


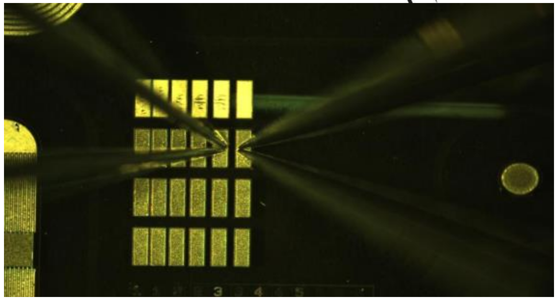


NanoMat UTT		Dépôt couche volatile Gravure SiC en ICP/RIE SF6 - ~2,5µm	**Profondeur à valider**	**1ère Litho- gravure N+ (4) Graveur ICP-RIE-SF6**	
ESIEE		Bains acides (dont Al-etch chaud) Acides (CARO, BHF) Solvants (Acétone IPA) Protection face avant – masque dur Dépôt masque dur (Ni) en pulvérisation cathodique	Retrait masque Nettoyage (optionnel) 1µm		
ESIEE		**Litho masque Niveau 10 (data sombres)** Résine positive 3µm **Alignement** Ouverture en humide masque dur	**2ème Litho- gravure P et éventuellement mesa de protection**	**2ème Litho- gravure P (1)**	

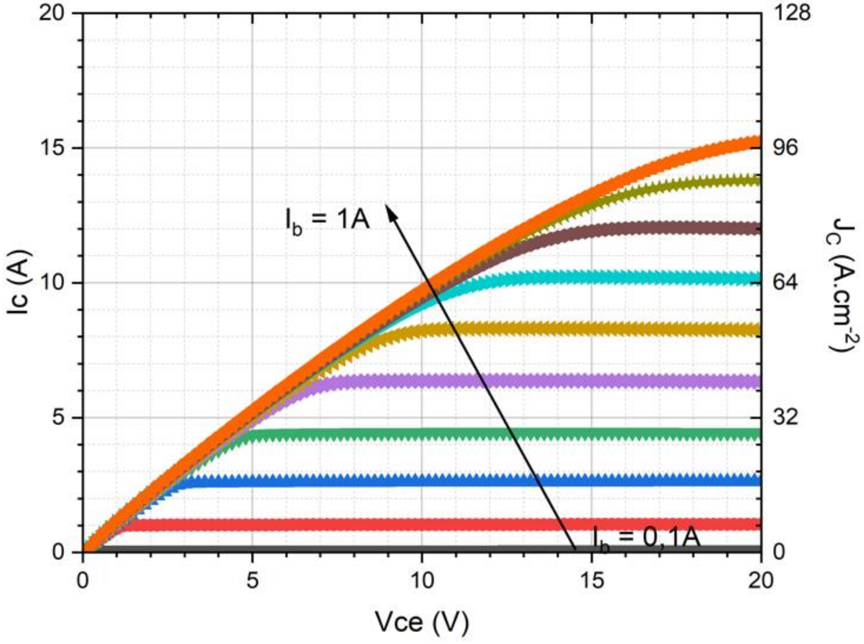


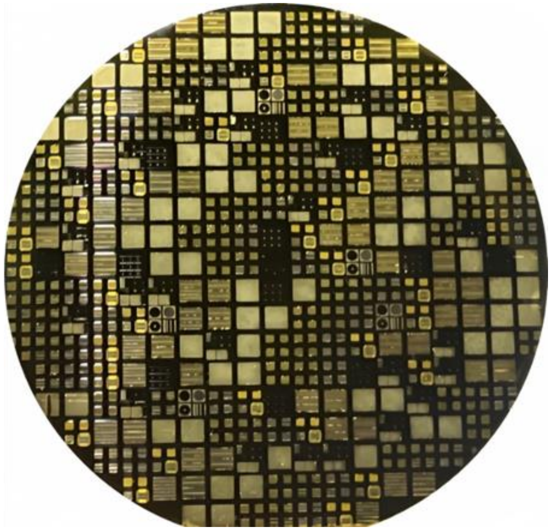
Electrical cahracterizations – 1st run





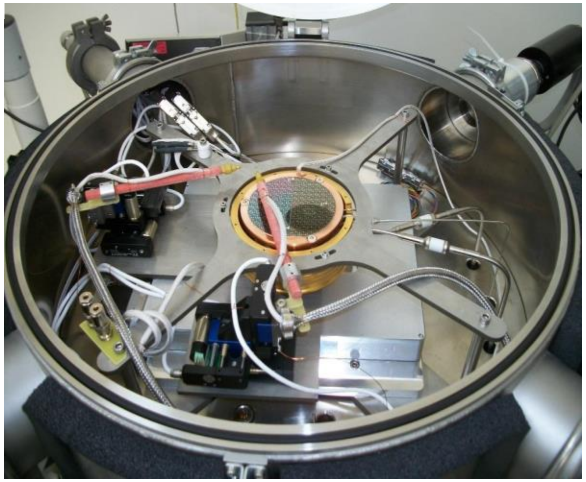
5 mm x 5 mm electrical BJT

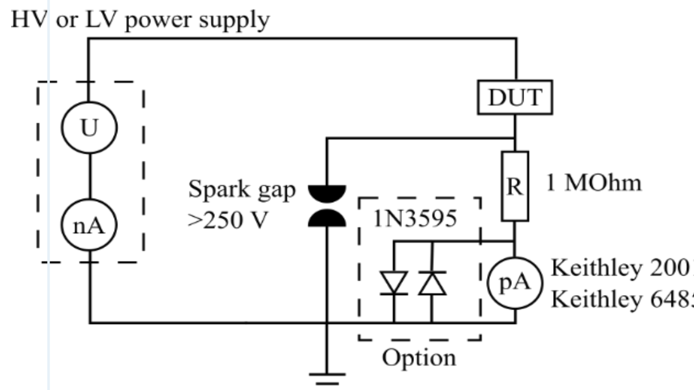




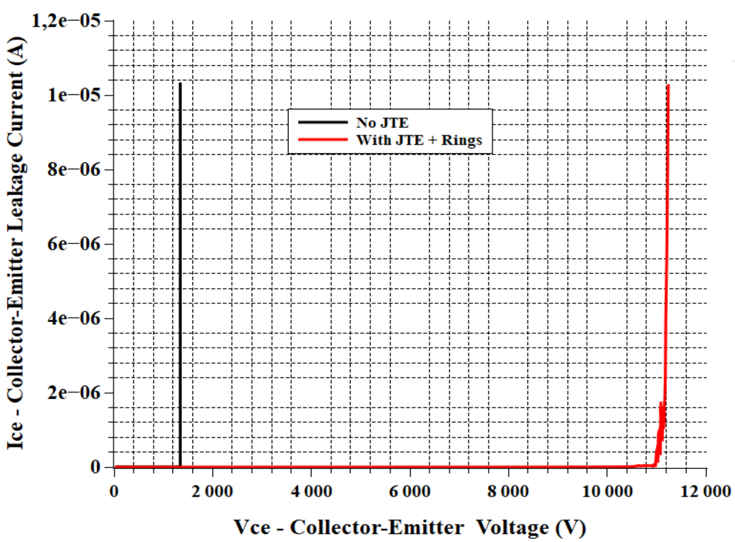
Current gain: 15

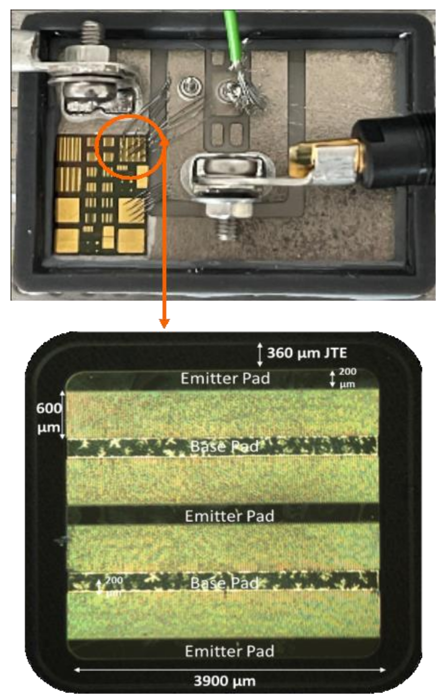
Breakdown voltage: 11kV (the goal was 10kV)





Reverse IV characteristics - open emitter blocking



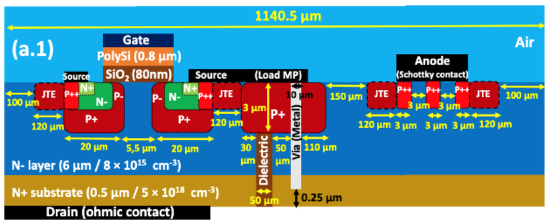


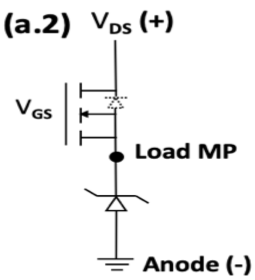
Electroluminescence at high voltage

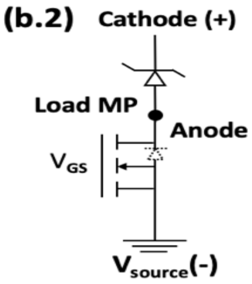
ANR MUS²IC - Monolithic Ultimate Switching cell in SIlicon Carbide

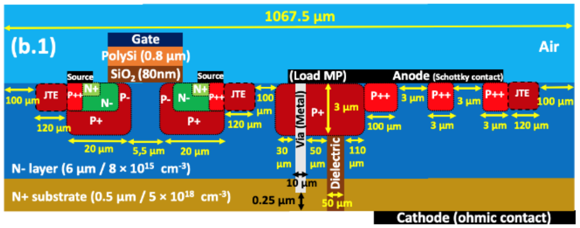
For Ultimate Efficient Power Vertical Integration

Full-SiC Single-Chip Buck and Boost MOSFET-JBS Converters :

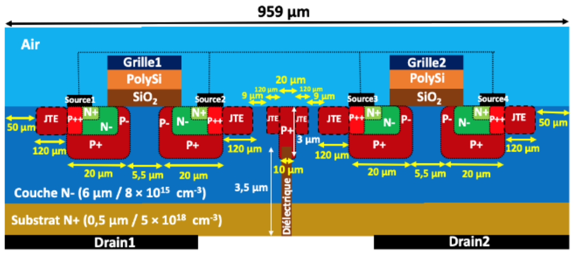


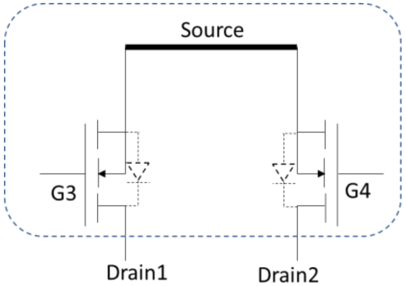






Full-SiC Single-Chip High-Side and Low-Side Dual-Mosfet :





→ **Technological realization of the deep vertical insulating SiC etched-trench region**

- by both and alternative fluorinated plasma and electrochemical eteching

- same process is need to isolate color centers in quantum nanophotonic cavities