



Toward an Innovative Monolithic Integration of Vertical and Lateral GaN Devices

Zahraa Zaidan, Nedal Al Taradeh, Christophe Rodriguez, Abdelatif Jaouad, Ali Soltani, Josiane Tasselli, Karine Isoird, Luong Việt Phung, Camille Sonnevile, Dominique Planson, et al.

► To cite this version:

Zahraa Zaidan, Nedal Al Taradeh, Christophe Rodriguez, Abdelatif Jaouad, Ali Soltani, et al.. Toward an Innovative Monolithic Integration of Vertical and Lateral GaN Devices. Conférence Euro-méditerranéenne Organisé par Matériaux, Composants et Systèmes (EMCMDS), Nov 2022, Fez, Morocco. hal-04303675

HAL Id: hal-04303675

<https://hal.science/hal-04303675>

Submitted on 18 Dec 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Toward an Innovative Monolithic Integration of Vertical and Lateral GaN Devices

Zahraa Zaidan^{1,2}, Nedal Al Taradeh¹, Christophe Rodriguez¹, Abdelatif Jaouad¹, Ali Soltani¹, Josiane Tasselli², Karine Isoird², Luong Viet Phung⁴, Camille Sonnevile⁴, Dominique Planson⁴, Yvon Cordier³, Frédéric Morancho² and Hassan Maher¹

¹ CNRS-LN2, 3IT-Université de Sherbrooke, 3000 Boulevard de l'Université, Sherbrooke J1K 0A5, QC, Canada

² LAAS-CNRS, Université de Toulouse, CNRS, UPS, Toulouse, France

³ CNRS-CRHEA, rue Bernard Grégory, 06560 Valbonne, France

⁴ Univ. Lyon, INSA Lyon, Univ. Claude Bernard Lyon 1, Ecole Centrale Lyon, CNRS, Ampère, F-69621, France

Email: Zahraa.Zaidan@USherbrooke.ca

Abstract—This work presents an innovative technology where GaN-based vertical and lateral devices are monolithically integrated. Indeed, this technology will enable to drive high-power switching devices (vertical GaN power FinFETs) using lateral GaN HEMTs with minimum losses and high stability. The main challenge of this technology is the electrical isolation between these two devices. In this paper, a new isolation approach is presented to avoid any degradation of the lateral transistor performance. In fact, the high voltage applied at the drain of the vertical GaN power FinFET can drastically affect the drain current of the lateral GaN HEMT. To overcome this problem, a highly doped n⁺ GaN layer is inserted between the epi-layers of these two devices. TCAD-Sentaurus simulator is used to validate this new approach. Indeed, this highly n-doped GaN layer is blocking the vertical high electrical field and preventing any depletion of the 2D gas of the lateral GaN HEMT. To the best of our knowledge, it is the first time where the vertical and lateral GaN devices are integrated within the same technology.

Keywords— GaN HEMT, vertical GaN FinFET, TCAD-Sentaurus, isolation, highly doped GaN, integrated circuits

I. INTRODUCTION

The exceptional physical properties of gallium nitride (GaN) recently attracted researcher's attention as a substitute for silicon in many applications [1]. GaN is a high-saturation-velocity material that withstands high temperature and high voltage thanks to its high breakdown electrical field and wide band gap [2]. The use of GaN-based devices has prompted the development of a number of devices like GaN HEMTs [3] and vertical GaN devices [4]. GaN-based power converters should occupy a significant part of the semiconductor market over the next decade by promising huge economic advantages specially in the Electric Vehicle industry (EV) with Power Electronic Conversion Systems (PECS) [5]. In our work we have designed a new technology for power converter by integrating GaN vertical and lateral devices on the same wafer. This approach allows to obtain a high-power switch, monolithically integrated with HEMT-based gate driver, and to enhance overall performance. The electrical isolation between these two GaN devices is a big challenge. In fact, the vertical GaN power FinFET is grown on n-doped GaN substrate shared with the HEMT. So, the backside of this last will be exposed to high voltage and its performance will be degraded. To solve this problem, we used TCAD-Sentaurus simulation to study a new technique to isolate vertical and lateral GaN transistors integrated on the same wafer.

II. SIMULATION RESULTS

The adopted approach in this work to insulate the lateral from the vertical GaN device is based on the insertion of a highly doped n-type GaN layer with a donor concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and a thickness of $t_{\text{iso}} = 0.2 \mu\text{m}$ between these two devices (Figure 1). The TCAD-Sentaurus software is used to evaluate the impact of this additional n⁺ GaN layer on the device performance. As shown in Figure 2, without the n⁺ layer, the HEMT output characteristics ($I_{\text{DS}}-V_{\text{DS}}$) are drastically degraded when a high voltage (1000 V) is applied on the backside contact (Vertical power GaN device contact). Using our new approach, we observe that the problem is solved even when applying the high voltage on the backside contact (Figure 3). The grounded extra layer is blocking the vertical electric field and improves the HEMT's performance. The HEMT on-resistance (R_{ON}) vs the voltage applied to the backside contact is presented in Figure 4. We can observe that R_{ON} increases from 5.7 $\Omega\cdot\text{mm}$ to 48.38 $\Omega\cdot\text{mm}$ as the applied voltage exceeds 900 V, until the device exhibits a diode behavior at 1000 V. The influence of both thickness and doping concentration of this extra layer has been investigated as presented in Figures 5 and 6. We can determine from these graphs that the thickness and doping concentration needed to isolate lateral from vertical devices are $t_{\text{iso}} = 10 \text{ nm}$ and $N_{\text{d}} = 1 \times 10^{18} \text{ cm}^{-3}$, respectively. We can conclude that our approach solves the initial problem and allows to monolithically integrate vertical and lateral GaN devices within the same technology. To the best of our knowledge, this is the first time that such an innovative approach is proposed to tackle the difficulties related to the fabrication of efficient high voltage switching systems based on GaN.

1. Li H, et al., in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC- ECCE Asia), 563–569 (2016)

2. Heckel T, et al., in 2015 IEEE International Telecommunications Energy Conference (INTELEC), 1–6 (2015)

3. Rolland G, et al., Energies, 6098 (2021)

4. Sun M., et al., IEEE Electron Device Letters, 509–512 (2017)

5. Kinzer D, et al., IEEE Power Electronics Magazine, 14–21 (2016)

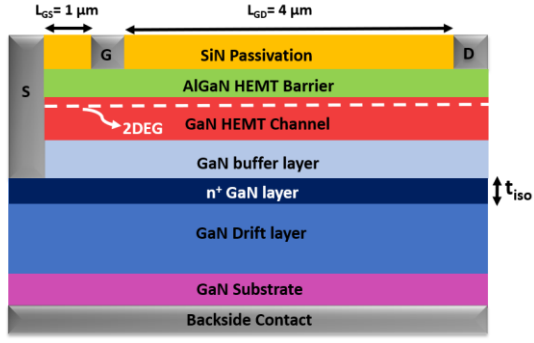


Fig. 1. AlGaIn/GaN HEMT schematic cross section showing the position of the n^+ GaN insulation layer as used in the TCAD-Sentaurus simulations

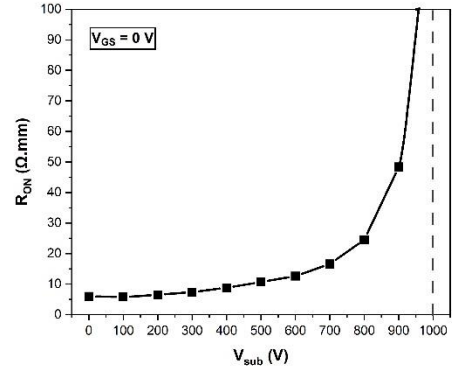


Fig. 4. Impact of the applied backside voltage (V_{sub}) on the on-resistance (R_{ON}) of the simulated HEMT device

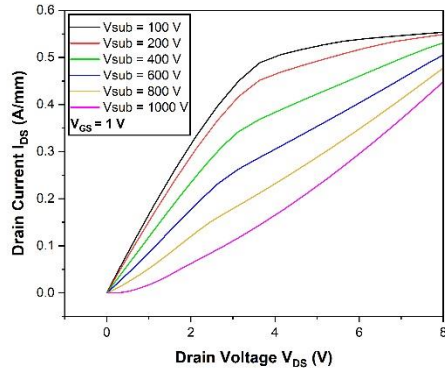


Fig. 2. $I_D(V_{DS})$ output characteristics of the simulated HEMT device with different applied voltages (V_{sub}) on the backside contact (Vertical power GaN device contact)

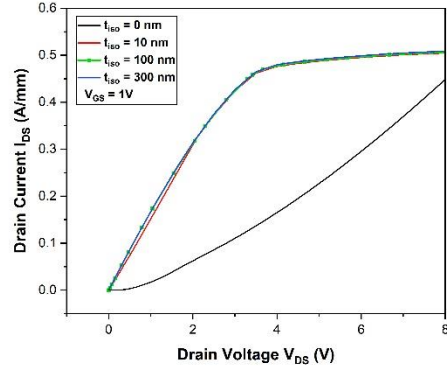


Fig. 5. $I_D(V_{DS})$ output characteristics of the simulated HEMT device with different thicknesses (t_{iso}) of the n^+ GaN layer at 1000 V applied voltage on the backside contact

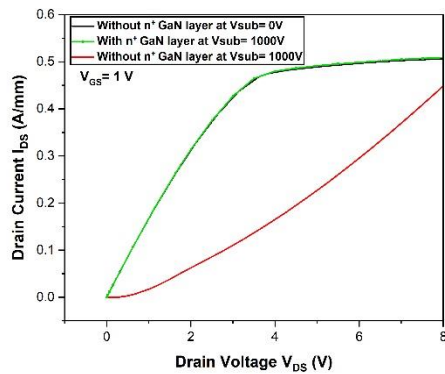


Fig. 3. $I_D(V_{DS})$ output characteristics of the simulated HEMT device with and without n^+ GaN layer at V_{sub} applied on the backside contact

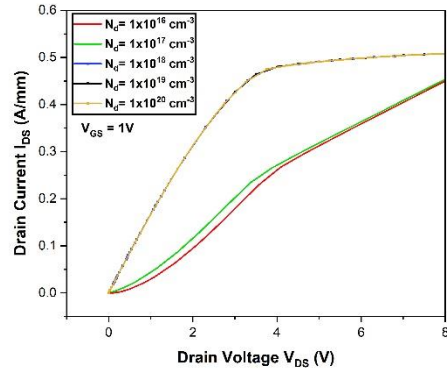


Fig. 6. $I_D(V_{DS})$ output characteristics of the simulated HEMT device with different donor doping concentrations (N_d) of n^+ GaN layer at 1000 V applied voltage on the backside contact