3D interconnects for III-V semiconductor heterostructures for miniaturized power devices

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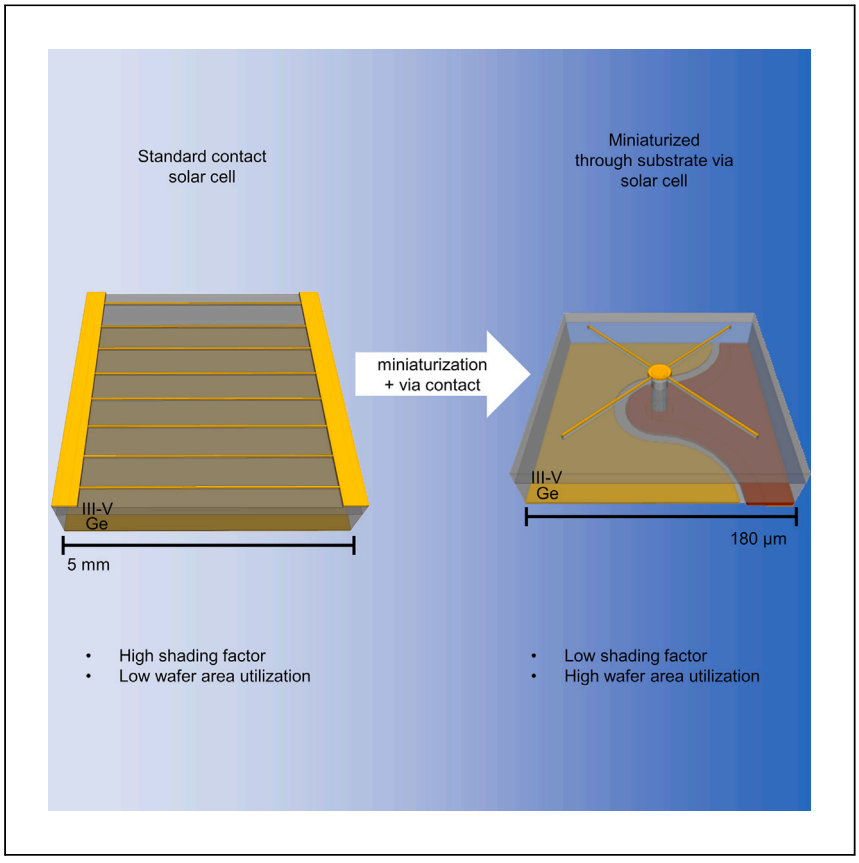

This work by de Lafontaine et al. reports a method to fabricate 3D interconnects on III-V semiconductor devices. A proof of concept is realized on III-V/Ge triple-junction solar cells with an area 3 orders of magnitude smaller compared with standard chips. This strategy enables device miniaturization with increased wafer area use.

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Highlights

3D interconnects on III-V devices offer high power density and miniaturization

3D interconnects are fabricated on III-V/Ge triple-junction micro solar cells

The interconnects achieve a 6-fold increase in wafer area use

The interconnects enable device area reduction by up to 3 orders of magnitude

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3D interconnects for III-V semiconductor heterostructures for miniaturized power devices

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SUMMARY

Three-dimensional (3D) interconnects increase chip power density and enable miniaturization. Photonic chips require new processes to enable transitioning to 3D interconnects. We fabricate 3D interconnects on a multijunction solar cell, leveraging processes such as III-V heterostructure plasma etching, gold electrodeposition, and chemical-mechanical polishing to integrate through substrate vias to the heterostructure. Wafer bonding is used to handle 20-μm-thin III-V films. The strategy enables us to demonstrate photonic power devices having areas 3 orders of magnitude smaller compared to standard chips. The design also yields a small shading factor below 3%. Compared to miniaturized photonic power devices with two-dimensional connections, 3D interconnects achieve a 6-fold increase in wafer area use. These improvements will enhance the power yield per wafer while unlocking high-density and miniaturized devices for applications such as power over fiber, the internet of things, and microconcentrator photovoltaics.

INTRODUCTION

Miniaturization and densification of power devices are the cornerstone of modern technologies for fields such as photovoltaics, photonics, betavoltaics, thermophotovoltaics, and power electronics. Densification in a two-dimensional (2D) framework faces ever increasing difficulties from lithography and packaging limitations. Over the past decades, three-dimensional (3D) integration has already been developed and refined for silicon-based electronics to support the historical rate of progress of complementary metal oxide semiconductor (CMOS) scaling.[1–5] Through substrate vias (TSVs) enable chip and device stacking while providing electrical power and communication.

For optical power applications, silicon has several limitations compared with III-V semiconductors. Its indirect bandgap prevents efficient light conversion to electricity for photovoltaic and photonic applications. Its fixed bandgap limits photonic, photovoltaic, betavoltaic, and thermophotovoltaic applications to a limited spectral region. III-V semiconductors can cover all wavelengths from the mid-infrared to the ultraviolet C region. Furthermore, silicon electronic mobility is several orders of magnitude lower than some III-V semiconductors.[6,7]

Improving both densification and efficiency of power devices ultimately requires 3D integration of III-V semiconductors. For GaN and SiC power-electronic modules,

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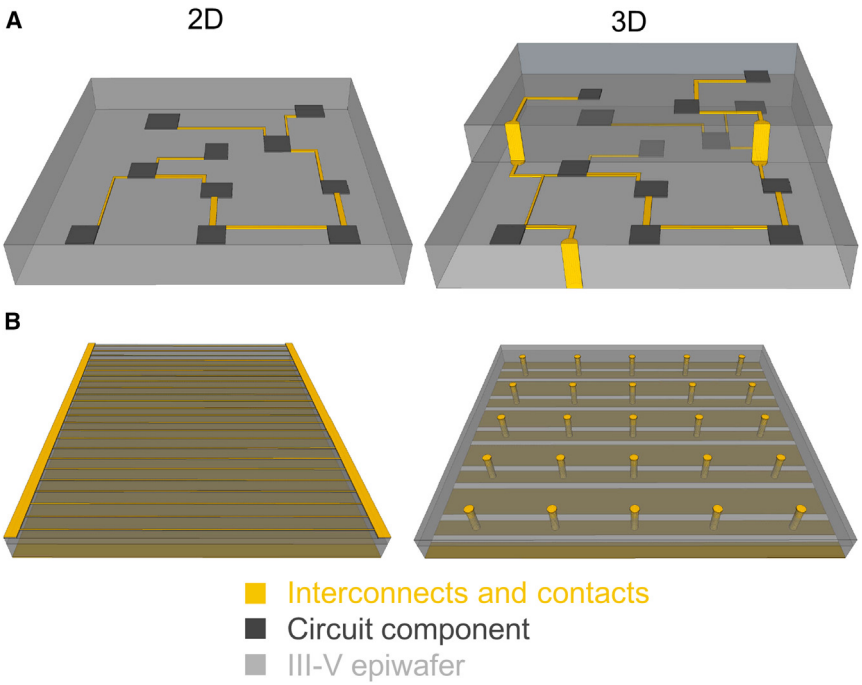


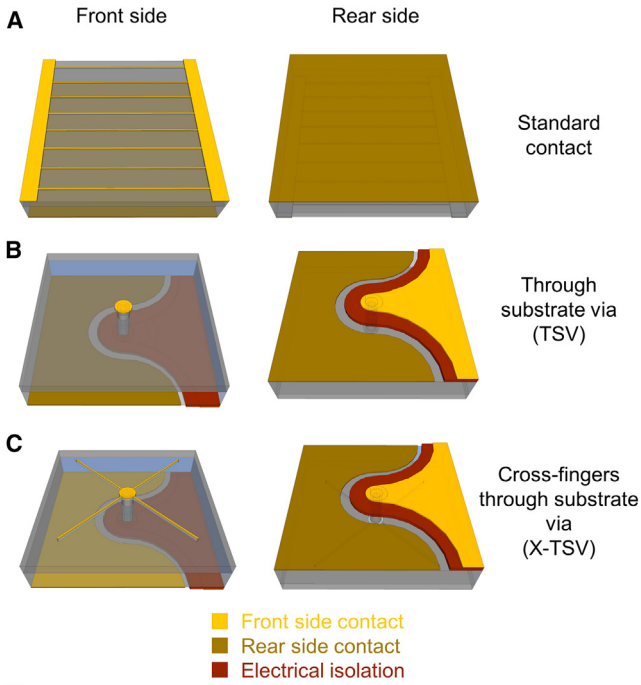
Figure 1. Densification and power loss mitigation through 3D integration

(A) Schematics of a 2D electronic circuit on a III-V epiwafer and a 3D electronic circuit on two III-V epiwafers bonded together and interconnected with through substrate vias.

(B) Thermophotovoltaic cell with 2D planar contacts and 3D interconnections using TSVs.

flip-chip[8,9] and hybrid approaches with Si TSVs[10–12] are still used, but some developments were performed for SiC via etching.[13] TSVs would also improve densification of high frequency devices such as high-electron-mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). Figure 1A illustrates how power component densification can be improved from 2D to 3D integration by stacking III-V epiwafers and interconnecting them with TSVs. For betavoltaic devices, a 3D scheme would improve power output by stacking multiple layers of radioisotope materials and III-V cells.[14,15] For thermophotovoltaic conversion, III-V alloys are used to convert heat into electricity.[16,17] Because of the low bandgap used, thermophotovoltaic devices generate high current densities ($\sim 1 \frac{A}{cm^2}$ under a 2,000°C source[16]) and could benefit from 3D interconnects to mitigate series resistance losses. The schematics in Figure 1B illustrate this strategy by reducing the metallization path length with a 3D integration using TSVs, which limits the joule losses compared with planar contacts with a 2D integration. For photovoltaics, 3D interconnects can increase the conversion efficiency and reduce the shading. Metal wrap through (MWT) was first developed on Si solar cells to reduce the shading factor to a value ranging between 3.4% and 5.6%.[18–22] The concept has been recently transposed to III-V photovoltaics.[23–25] Simulation results have shown that TSVs could reduce the series resistance by 70% compared with standard contacts on triple-junction solar cells.[26]

In this work, we demonstrate 3D interconnects on III-V heterostructures to increase the efficiency, increase the power density and miniaturize the device. The proof of concept has been performed on a micro-scale III-V/Ge multijunction solar cell by adding TSV contacts. III-V multijunction solar cells currently hold several conversion efficiency records,[27–30] but they are limited by shading and resistive losses. Micro-scale solar cells (μcells) have been proposed to alleviate heat dissipation and



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Design	Shading factor [%]	Best Efficiency [%]
Si metal wrap through	3.4 - 5.6	18.3
III-V Standard	6 - 68	47.6
III-V TSV	0.45	28.3
III-V X-TSV	2.80	18.3

Figure 2. Solar cell architectures and shading factor comparison

(A–C) Schematic of (A) a standard busbar and grid lines micro solar cell, (B) a through substrate via contact micro solar cell (TSV), and (C) a cross-fingers through substrate via contact (X-TSV) micro solar cell from the front side (left) and the rear side (right).

(D) The table compares the shading factor for each design. The shading factors for metal wrap through (MWT) Si solar cells and the efficiencies were taken from the literature[18–22,25,27] and this work.

resistive losses.[31–38] It has been the object of a growing interest for both numerical simulations[32,36] and experimental works.[33,34,36,37] As depicted in Figure 2A, the device size can be reduced, but the two busbars on the front side cannot, that is because their areas are fixed by packaging requirements. This leads to an increased ratio of metallized to active area as the device size is reduced,[36] reducing the power yield per wafer. Furthermore, it increases the dark current contribution and reduces the open-circuit voltage.[36] Photonic power converters[39–43] also suffer from the same effects as they are miniaturized and will benefit from 3D interconnects. Various other power devices are facing similar challenges as internet-of-things devices are being miniaturized.

Using TSVs to transfer the front side contact to the back side through the device could mitigate shading, dark current contribution, and resistive losses. Figure 2 presents schematics of a III-V multijunction solar cell with a TSV contact (Figure 2B) and with cross-fingers TSV contact (X-TSV; Figure 2C). The shading factors of each architecture are presented in the table in Figure 2D. The shading factor depends on the device size for standard contacts, as it varies from 6% for large device

(~1 × 1 cm^2) to 68% for small devices, whereas it is constant for a 3D architecture. Simulations of 3D interconnects on multijunction solar cells demonstrated a conversion efficiency increase up to 3% absolute and a power yield enhancement per wafer of 20%.[26,44] The first TSV multijunction solar cell was fabricated on an inverted dual-junction heterostructure, demonstrating the proof of concept.[24,25]

In this study, we demonstrate a proof of concept of 3D interconnects on micro-scale triple-junction solar cells to miniaturize, reduce the shading, reduce the parasitic dark current, increase the power density, and improve the power yield per wafer.

RESULTS

Characterization

The X-TSV triple-junction solar cells were characterized on their performance, their shading factor, and their wafer use for power generation. They were benchmarked to standard front and rear side contact triple-junction solar cells on all these metrics to assess the viability of the technology.

Ten X-TSV μcells were characterized, and Figure 3A presents the current density-voltage (J-V) characteristics of X-TSV μcells under 0.88 sun AM1.5G illumination. On average, the cells present an open-circuit voltage (V_{oc}) of 2.276 V, a short-circuit current density (J_{sc}) of 8.61 $\frac{mA}{cm^2}$, and a fill factor (FF) of 82.1%, which results in maximum power of 16.1 $\frac{mW}{cm^2}$ and efficiency of 18.3%. The spread of these parameters is depicted in Figure 3B. These results are reproducible over several devices, as low variability was observed among the characterized devices. All the measured parameters are within 2.8% of the average over ten cells. However, the devices present a lower short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}) than state-of-the-art III-V/Ge triple-junction solar cells.[45] The lower J_{sc} can be explained by parasitic absorption and additional reflections from the polydimethylsiloxane (PDMS) and quartz on the front side. These losses will be suppressed once the quartz and PDMS are replaced with an optimized antireflection coating, such as a SiN_xH_y/SiO_xH_y bilayer[37] or microstructured antireflection coating.[46] As for the V_{oc}, increased edge recombination from a large perimeter-to-area ratio $\frac{P}{A}$ can explain the lower values, as previously shown on micro cells with standard metallization.[36,37] Previous work has shown that surface recombination at the edge of the solar cell becomes important by adding via holes and at micrometric scales.[36,37,47–52] This phenomenon can be mitigated by efficient surface passivation methods.[23,37] The devices studied have a small area (180 × 180 μm^2) and a hole in the middle, which increases $\frac{P}{A}$ to 232 cm^{-1}, almost twice the value of their micro cells with standard metallization counterparts.[36,37] Albert et al[37] previously reported a lower V_{ox} (2.1 V) for a smaller $\frac{P}{A}$ (80 cm^{-1}) despite the fact that a similar III-V/Ge triple-junction heterostructure was used. This difference is caused by the use of standard contacts, which creates a larger shaded area than the X-TSV design. It increases the parasitic dark current, which lowers the open-circuit voltage. Such a mechanism was recently put in light by Wiesenfarth et al.[36] The results show that a 3D interconnection scheme can successfully reduce parasitic dark current losses on miniaturized device.

Performance improvement

To assess the improvement from the X-TSV architecture, the front metallization needs to be compared with that of a standard contact architecture. Figure 4A presents a top view optical microscope image of an X-TSV μcell. To compare the front side contact design, those images are compared with standard contact μcells fabricated by Albert et al.[37] (Figure 4B) and a standard 5.5 × 5.5 mm cell (Figure 4C). On

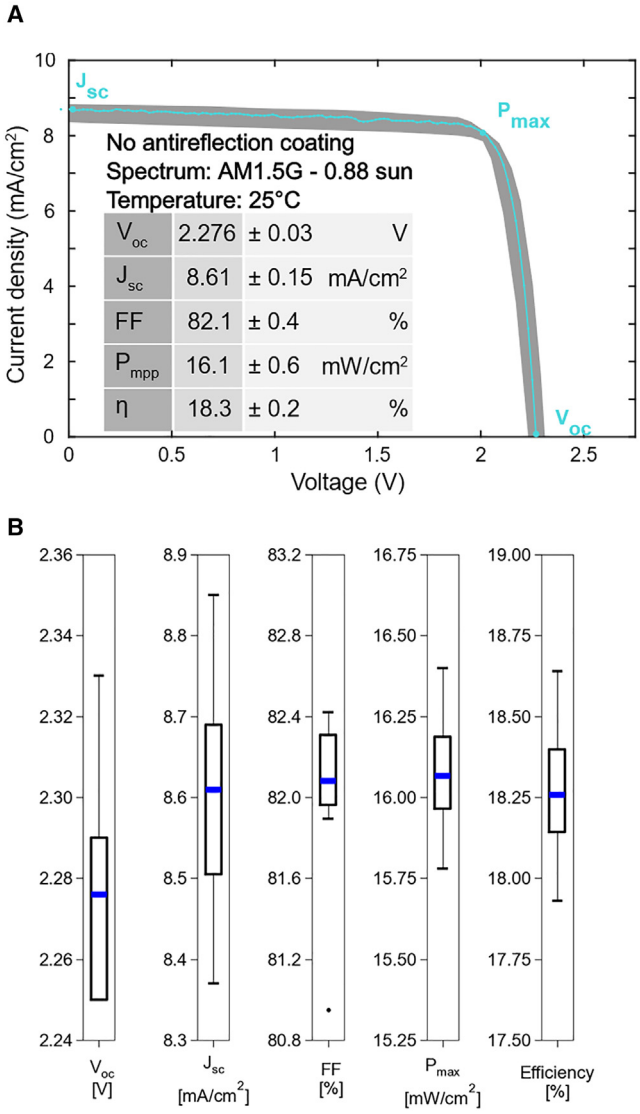

Figure 3. Electrical characterization

(A) Current density-voltage characteristics of X-TSV micro solar cells averaged over 10 cells. The gray area along the curve is the variability between all devices.

(B) Boxplots presenting the data spread of the V_{oc}, J_{sc}, FF, maximum power (P_{max}), and efficiency over all 10 devices. The mean is depicted in blue.

the schematics of Figures 4A–4C, the active region, the metallization, and mesa isolation trenches are represented in blue, gold, and purple, respectively. The trends of the shading factor as a function of the device area for various architecture are depicted in Figure 4D. The shading factor is defined as the ratio between the metallized area (Figures 4A–4C, gold area) and the device area (Figures 4A–4C, sum of blue and gold areas). The wafer use for power generation is also studied as a function of the device area, as shown in Figure 4E. We define the wafer use for power generation as the ratio between active area (Figures 4A–4C, blue area) over the total wafer area (Figures 4A–4C, sum of blue, gold, and purple areas).

It is possible to notice that the metallization area is 15 times larger on standard µcells (Figure 4B; ~14,400 μm^2) than X-TSV cells (Figure 4A; ~910 μm^2). This is mainly

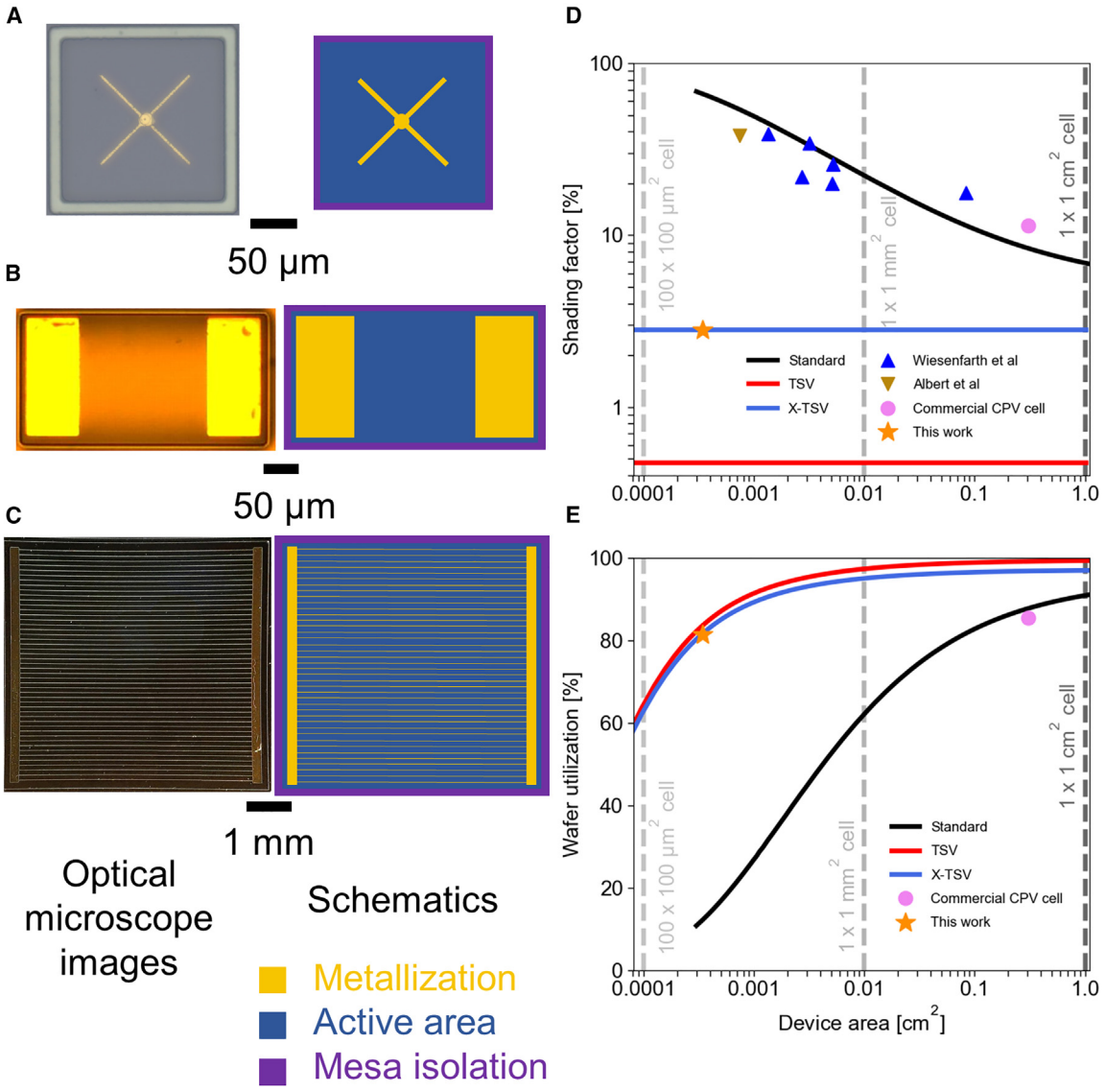

Figure 4. Device schematics and area comparisons

(A–C) Optical microscope images (left) and schematics (right) of (A) X-TSV µcells (50 µm scale bar), (B) standard contact µcells reported in another study (50 µm scale bar),[37] and (C) a 5.5 × 5.5 mm standard cell (1 mm scale bar). The schematics of all three devices with the regions of interest are identified. The active region is presented in blue, the metallization is shown in gold, and the mesa isolation is presented in purple.

(D) Shading factor presented as a function of the device area for standard cells, TSV cells, and X-TSV cells. Several experimental results from the literature[36,37] are also presented.

(E) Wafer use for power generation presented as a function of the device area for standard cells, X-TSV cells, and TSV cells.

caused by the busbar dimension as it is bound by the wire bonding and packaging techniques. This result confirms that the shaded area can be reduced by using a TSV architecture instead of grid lines and busbars. Figure 4D indicates that as the size of a device with standard contacts is reduced from a centimeter size down to a submillimetric size, the metallization ratio jumps from 7% to ~68%. The standard µcells previously reported by Wiesenfarth et al.[36] and Albert et al.[37] follow the standard contact trend quite well. The shading factor for a commercial 5.5 × 5.5 mm^2 cell is also shown in Figure 4D, and it is also consistent with the trend as it has a metallization ratio of 11%. Using X-TSVs enables to break this trend and to maintain the

metallization ratio down to 2.8%. More importantly, this ratio does not vary with device area, as this architecture is unrestricted by busbars on the front side. This demonstrates the relevance of the X-TSV contact architecture for multijunction solar cell for a wide range of device sizes. It enables the fabrication of submillimetric solar cells without having the majority of the active area shaded by the metallization. The cross-finger ohmic contact is determined by the photolithography mask design. For example, the cross-fingers could be removed to only keep a concentric ohmic contact aligned with the via (baseline TSV architecture). In this case, the metallization ratio is further reduced to a value of 0.5%.

As for the wafer use (Figure 4E), the standard contact solar cells trend drops precipitously from 91% for a 1 × 1 cm^2 down to 11% for submillimetric devices. The 5.5 × 5.5 mm^2 commercial concentrator photovoltaic (CPV) cell also follows this trend. However, submillimetric standard contact cells present a dramatically low wafer use (<60%), which suggests that they may not be industrially viable. Again, both X-TSVs and TSVs make it possible to break this trend. For centimeter-scale devices, the wafer use is 99% and 97% for the TSV and X-TSV designs, respectively, representing 9% and 7% increases, respectively, compared with standard contact devices. The major improvement comes from the increased useful area use at a submillimetric scale. In this case, the wafer use drops respectively to 82% and 80% for the TSV and X-TSV designs. Substituting standard contacts for TSV or X-TSV architectures on μcells could therefore increase this metric by respectively 645% and 627%. Considering the substrate and epitaxy costs,[53] using these architectures could be a great benefit to solar cells or other optoelectronic devices miniaturization.

DISCUSSION

The enhanced level of complexity from a 3D architecture has three main challenges: (1) increased failure risks, (2) increased manufacturing costs, and (3) requirement for specialized tools. The increased failure risks can be explained by the number of technological steps required as it is more than 10-fold to that required for standard contacts. Furthermore, adding vias creates an enhanced shunting risk. Despite the process complexity, 25% of the first generation prototypes had an excellent electrical performance in this study. Several technological steps such as plasma etching and atomic layer deposition (ALD) are already well known and used in the CMOS industry. Therefore, the knowledge of this mature industry can also mitigate the risk associated to device failure.

The increased manufacturing cost from the additional technological steps is unavoidable. It is currently difficult to assess the manufacturing cost of X-TSV μcells because no industrial transfer has occurred yet, but it is still possible to do some preliminary projections. The microfabrication steps required on standard multijunction solar cells represent approximately 10% over the total cost of the device. Assuming that the manufacturing cost increases linearly with the number of steps, TSV contact microfabrication would represent 100% of the current standard contact multijunction solar cell, since the number of fabrication steps is 10-fold higher. From this estimation, X-TSV cells would be 1.9 times the cost of a current standard contact multijunction solar cell. However, there are several mitigating factors to consider. The manufacturing cost increase must be considered in the context that it also comes with an active wafer use for power generation increase. For X-TSV μcells, it has been shown in the previous section that the active area can be increased 6-fold compared with miniaturized standard contact solar cells. This large improvement comes from the standard front metallization not being suited for miniaturized

device, whereas 3D interconnects are independent of the device area. Assuming an identical conversion efficiency can be realized with further development, these projections indicate that the cost per watt associated to this technology could be reduced 3-fold by using X-TSV μcells instead of standard contact μcells. Therefore, considering the projected pros and cons, using 3D interconnects would be a pathway toward reducing the cost per energy yield of miniaturized III-V cells. This is a positive projection considering the fact that the current challenge is to reduce the cost of III-V based solar cells.[53–55] Note that using 3D interconnects could also reduce the cost of cell assembly, as surface mounting technology assembly processes could be used instead of more expensive wirebonding interconnection processes.

Specialized tools that are not common in the multijunction photovoltaic industry will be required to manufacture TSV contacts. To name a few, plasma etching, ALD and chemical-mechanical planarization (CMP) are not currently used in multijunction solar cell manufacturing, which suggests that a paradigm shift will be required for X-TSV manufacturing. However, those three techniques have been well known for several decades in the CMOS industry. This aspect gives additional weight to the relevance of the CMOS industry in the scope of manufacturing these devices. Learning from the CMOS industry, could therefore mitigate the risks associated to this last challenge. This aspect is of significant importance considering the multiple challenges associated to TSV reliability.[3–5]

Several improvements could be made to increase the X-TSV device performance. The vias are not the limiting factor for series resistance. Under concentrated sunlight, the series resistance in the window and emitter layers become the limiting factor.[26] Therefore, for larger devices with via arrays, reducing the pitch between each via could improve the performance. With further process optimization, the via diameter could be reduced to 5 μm. This small change will reduce the shading factor by 24% compared with the values reported in this study. Last, no antireflection coating was used in this study and a quartz substrate was bonded on the front side to handle the thin heterostructure. These two aspects reduce the photogenerated current by more than 30%. These devices could be improved by adding an antireflection coating and by removing the quartz substrate. In that case, the device rear side will need to be bonded on another handling substrate, which will require additional processes.

The prototypes were developed on a III-V/Ge triple-junction heterostructure. However, the baseline process does not depend on a specific heterostructure, which means that it could be applied to four or more junction solar cells.[28,29] Photonic power converters can have a small active area, ranging from 0.054 cm^2,[39,40] down to 0.034 cm^2.[41,42] Thermophotovoltaic devices generate high current densities[16] and could benefit from this architecture to mitigate series resistance losses. Three-dimensional interconnects could thus benefit a wide range of III-V based devices that require miniaturization, improved power management or reduced production cost. For large-area devices, it would be feasible to add vias for applications such as thermophotovoltaics, large photonic power converters areas and betavoltaics. The back contacts could be interdigitated as shown in previous work.[56]

We demonstrated the proof of concept of the first μcell with a TSV contact architecture. X-TSV μcells presented excellent electrical performance with a high FF (82%) and a high V_{oc} (2.28 V), despite their large $\frac{P}{A}$ (232 cm^{-1}). The X-TSV architecture enables a large reduction of the metallized area on the front side of the solar cell. With standard grid line/busbar contacts, the metallized area can jump from 6% to 68%

from device miniaturization. Using X-TSV or TSV contacts break this trend by keeping metallized ratios of 2.8% and 0.5%, respectively, regardless of the device size. Furthermore, the baseline TSV process uses plasma mesa isolation, which, combined with the reduced metallized area, greatly enhances the wafer use for active area. The current design could increase the wafer use for power generation more than 6-fold for submillimetric solar cells. This aspect is quite relevant considering the fact that III-V semiconductors are expensive. This concept can be readily applied to other multijunction solar cell heterostructures, photonic power converters and thermophotovoltaic devices.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact

Further information and requests should be directed to and will be fulfilled by the lead contact, Mathieu de Lafontaine (mdelafon@uottawa.ca).

Materials availability

This study did not generate new unique materials. The III-V/Ge triple-junction heterostructures used in this study are commercially available. All microfabrication products used in this study are commercially available.

Data and code availability

Data reported in this paper can be provided by the lead contact upon reasonable request. This paper does not report original code.

Microfabrication process

The main fabrication steps are presented in Figure 5. The process starts from a commercial III-V/Ge triple-junction heterostructure with a InGaP top cell, a (In)GaAs middle cell and a Ge bottom cell. All devices presented in this study were fabricated from the same wafer. The first step consists in plasma etching a via hole through the active regions (Figure 5A). A SiO_2 hard mask was deposited by plasma-enhanced chemical vapor deposition (PECVD) in an STS PECVD system. The hard mask was patterned by contact photolithography and a $CF_4/He/H_2$ plasma in an STS inductively coupled plasma (ICP)-reactive ion etching (RIE) plasma etcher. The patterns were transferred into the heterostructure with a $SiCl_4/H_2/Cl_2$ plasma in an STS ICP-RIE plasma etcher to form a 10-μm-diameter via hole (Figure 5A). The vias are electrically isolated with a 50-nm-thick Al_2O_3 film deposited by ALD, as shown in Figure 5B. $Al_2(CH_3)_6$ cycled with H_2O were used as the precursors.

The via metallization is realized in two steps. A TiN film is deposited by plasma-enhanced ALD (PEALD) (Figure 5B), and the precursors used were $Ti[N(CH_3)_2]_4$ cycled with an $N_2/H_2/Ar$ plasma. TiN is used as a seed layer to metallize the vias by Au electroplating, as shown in Figure 5C. To improve gold adhesion to TiN within the via holes, the sample was cleaned using isopropanol under ultrasound and under rough vacuum. The sample was then deoxidized with buffered oxide etch and the TiN surface was treated with a $PdCl_2$ (0.28 mM)/HCl (36.5 mM)/HF (185.2mM) solution.[57] Electroplating was performed with commercial solution Elevate Gold 7990 with a constant current density of 1 $\frac{mA}{cm^2}$. After this step, the vias are metallized but there is an excess in Au, TiN, and Al_2O_3 on the front side. Figure 5D shows the next step, consisting in selectively removing the gold on the front side. It is performed by a gold CMP in a Alpsitec E460 tool. A gold etch slurry diluted in deionized (DI) water (1:10) was chosen to enhance the chemical aspect of this process. Then, both ALD layers are etched with a BCl_3/Ar plasma

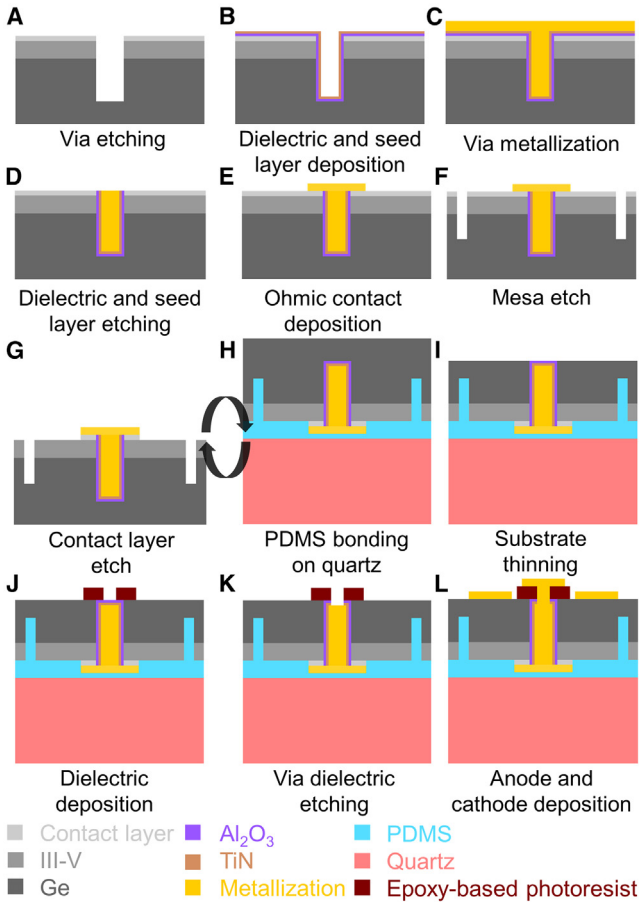

Figure 5. Microfabrication process

Schematics of the microfabrication process for cross-fingers through substrate via contact fabrication on a III-V/Ge triple-junction heterostructure.

performed in an STS ICP-RIE reactor, as illustrated in Figure 5D. After this step, the via is completely isolated and metallized and the contact layer is revealed on the front side. The cross-finger ohmic contact is patterned on both the via and the contact layer by contact photolithography, metal evaporation of Ni/Ge/Au/Ni/Au and lift-off (Figure 5E). To limit the shading, the cross-finger width is limited to 3 μm, and the concentric ohmic contact has a diameter of 14 μm. Then, a mesa isolation is performed by plasma etching with a $SiCl_4/H_2/Cl_2$ chemistry in an STS ICP-RIE plasma etcher. This step defines 10-μm-wide trenches around every single μcell (Figure 5F). This step also defines the individual device size to 180 × 180 μm^2. The samples are immersed in an $NH_4OH/H_2O_2/H_2O$ (9:9:240) solution to clean the mesa isolation sidewall and to etch the contact layer, in a self-aligned fashion with the ohmic contact, as shown in Figure 5G. The front side is then permanently bonded on a quartz substrate with PDMS, as shown in Figure 5H. The PDMS Sylgard 184 was used with a weight ratio of 10:1 between the elastomer base and curing agent. The PDMS is put in a vacuum chamber to outgas all the air bubbles. The bonding is performed at atmospheric pressure and on a hot plate at 100°C for one hour to cross-link PDMS. A pressure of 50 kPa was applied between the cell and the quartz during cross-linking. The substrate bonding keeps the mechanical integrity of the device after the substrate is thinned down to a thickness of 20 μm. This last step marks the end of the front side processing as no antireflecting

coating was deposited. For this study, it was not possible to accurately design an antireflection coating. The optical effect of the PDMS after wafer bonding on X-TSV solar cells are challenging to predict as the PDMS refractive index and the thickness may vary. Furthermore, PECVD processes used to deposit antireflection coatings are usually performed at temperatures higher than 200°C and thermal expansion can damage the via. Figure 5I illustrates the substrate thinning to reveal the via on the backside It is performed with an SF_6 plasma etching process in an STS ICP-RIE etcher. After the via is revealed on the rear side, an epoxy-based photoresist is deposited and patterned on the rear side, as shown in Figure 5J. This dielectric film has two purposes: (1) it electrically isolates the anode from the Ge substrate to prevent from any short circuit, and (2) it acts as an etching mask for the next step. The via dielectric at the bottom of the via is then opened with a BCl_3/Ar plasma in an STS ICP-RIE etcher. This step exposes the via metallization on the backside, as illustrated in Figure 5K. Finally, a last photolithography, a Ni/Al metal evaporation and lift-off are performed to pattern both contacts on the backside. As shown in Figure 5L, the anode is deposited on both the via metallization and the dielectric film, whereas the cathode is deposited on the Ge substrate.

Solar cell characterization

Fabricated X-TSV solar cells were characterized by J-V measurements under illumination. The solar simulator is a Newport Oriel Sol3A with an AM1.5D filter and it was calibrated to a power of 0.88 sun to minimize the current mismatch and have an accurate assessment of the FF. Calibration was performed using InGaP and (In)GaAs isotypes solar cells. Measurements were performed from −0.05 V up to 2.65 V with 0.01 V steps and ∼17 ms integration time in forward direction. A 1 × 1 cm aperture was used during the measurement.

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AUTHOR CONTRIBUTIONS

Conceptualization, M.d.L., A.J., V.A., and M.D.; methodology, M.d.L., T.B., E.P, C.P.-E., A.T., R.S., A.J., C.E.V., and M.D.; software, M.d.L. and T.B.; validation, M.d.L., T.B., A.T., R.S., S.E., and C.E.V.; formal analysis, M.d.L. and T.B.; investigation, M.d.L., T.B., R.S., S.E., and C.E.V.; resources, M.d.L., T.B., A.T., S.E., A.J., C.E.V., K.H., S.F., V.A., and M.D.; data curation, M.d.L. and T.B.; writing – original draft, M.d.L.; writing – review & editing, M.d.L., T.B., E.P., A.T., S.E., C.E.V., K.H., S.F., and M.D.; visualization, M.d.L., C.E.V., K.H., and M.D.; supervision, E.P., M.V., A.J., C.E.V., K.H., S.F., V.A., and M.D.; project administration, M.d.L., E.P., M.V., A.J., C.E.V., K.H., S.F., V.A., and M.D.; funding acquisition, M.d.L., E.P., M.V., A.J., S.F., V.A., and M.D.

DECLARATION OF INTERESTS

C.E.V. is a co-founder and chief technology officer of Enurgen. K.H. is a co-founder and president of Enurgen. S.F. is an employee of Broadcom Canada.

INCLUSION AND DIVERSITY

We support inclusive, diverse, and equitable conduct of research.

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