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Reconfigurable Multifunctional van der Waals Ferroelectric Devices and Logic Circuits

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ABSTRACT

Emerging reconfigurable devices are fast gaining in popularity in the search for next-generation computing hardware, while ferroelectric engineering of the doping state in semiconductor materials has the potential to offer alternatives to the traditional von-Neumann architecture. In this work, we combine these concepts and demonstrate the suitability of Reconfigurable Ferroelectric Field-Effect-Transistors (Re-FeFET) for designing non-volatile reconfigurable logic-in-memory circuits with multifunctional capabilities. Modulation of the energy landscape within a homojunction of a 2D tungsten diselenide (WSe_2) layer is achieved by independently controlling two split-gate electrodes made of a ferroelectric 2D copper indium thiophosphate ($CuInP_2S_6$) layer. Controlling the state encoded in the Program Gate enables switching between p, n and ambipolar FeFET operating modes. The transistors exhibit on-off ratios exceeding 10^6 and hysteresis windows of up to 10 V width. The homojunction can change from ohmic-like to diode behavior, with a large rectification ratio of 10^4 . When programmed in the diode mode, the large built-in p-n junction electric field enables efficient separation of photogenerated carriers, making the device attractive for energy harvesting applications. The implementation of the Re-FeFET for reconfigurable logic functions shows how a circuit can be reconfigured to emulate either polymorphic ferroelectric NAND/AND logic-in-memory or electronic XNOR logic with long retention time exceeding 10^4 seconds. We also illustrate how a circuit design made of just two Re-FeFETs exhibits high logic expressivity with reconfigurability at runtime to implement several key non-volatile 2-input logic functions. Moreover, the Re-FeFET circuit demonstrates remarkable compactness, with an up to 80% reduction in transistor count compared to standard CMOS design. The 2D van der Waals Re-FeFET devices therefore exhibit groundbreaking potential for both More-than-Moore and beyond-Moore future of electronics, in particular for an

energy-efficient implementation of in-memory computing and machine learning hardware, due to their multifunctionality and design compactness.

INTRODUCTION

Modern integrated circuits face significant challenges in the quest for continuous device miniaturization, pushing the boundaries of Moore's Law.^{1,2} Key concerns include device downscaling, circuit design and energy consumption. Conventional circuit design is based on elementary devices with fixed functionality such as Field Effect Transistors (FET), diodes, and memories. The prevailing technology in this domain is Complementary Metal Oxide Semiconductor (CMOS), which classically employs unipolar FETs that are fixed to either n-type or p-type operation based on their underlying fabrication process and chemical doping. However, as device downscaling progresses, this approach poses increasing complexity-related challenges.^{3,4}

To overcome some of the limitations of CMOS, an elegant emerging approach leverages the concept of Reconfigurable FETs (ReFET).^{5,6} Unlike conventional FETs, these devices offer a promising solution by providing the ability to adjust their functionality. A ReFET typically consists of two gate electrodes, either lateral or vertical, that independently control the energy band profile within the semiconductor channel. Specifically, the program gate (PG) determines the type of carrier, while the control gate (CG) toggles the transistor on and off. This disruptive FET concept allows for a reversible reconfiguration between n-type and p-type operating modes.⁷ The inclusion of these additional functionalities in a single device enhances logic capabilities and device versatility and potentially mitigates the challenges posed by miniaturization. For instance, a logic gate based on ReFETs can dynamically adjust its configuration during operation to implement a different truth table.⁸ Furthermore, this technology holds promise for next-generation hardware security applications by safeguarding against the direct reading of the layout of an integrated circuit and dramatically complicating reverse engineering through key protection strategies.^{9,10} Lastly, as inherently multifunctional systems, reconfigurable electronic devices find applications in various fields such as neuromorphics^{11,12}, in-memory computing¹³⁻¹⁵, energy harvesting,¹⁶⁻¹⁸ and nanoelectronics in general.¹⁹⁻²²

Integrating nanomaterials into the technological roadmap is a promising approach to surpass the limitations of Moore's Law.^{2,5,23} Among these nanomaterials, two-dimensional (2D) materials have emerged as viable candidates due to their favorable electrical performance, scalability, and compatibility with silicon platforms.^{4,24-26} The unique characteristic of 2D materials lies in their dangling bond-free interfaces, which offer unprecedented flexibility in combining different materials, thereby opening up possibilities for uncharted device concepts.^{27,28} Furthermore, their ultimate atomic thickness and high sensitivity to external electric fields enable efficient engineering of the energy band profiles.^{29,30} Consequently, certain 2D semiconductors, such as WSe₂, MoTe₂ or black phosphorus, can demonstrate ambipolar characteristics when used in conjunction with suitable metal contacts.³¹ These combined properties position van der Waals materials as an ideal platform for reconfigurable electronics.

However, the current implementation of ReFETs heavily relies on volatile external voltages to program their operating modes. The p- and n-conduction modes are configured by connecting the program gates to fixed voltage levels.^{6,9} This approach raises concerns regarding energy consumption and reliability, and limits the benefits of reconfigurability. To overcome these challenges, it is crucial to develop non-volatile ReFETs that can maintain their doping profile without the need to continuously maintain the gate voltages. One promising approach to introduce non-volatility in ReFETs is through the integration of ferroelectric materials as the gate medium. The ferroelectric

gate can retain non-volatile polarization states, which are then used to electrostatically dope the adjacent semiconductor layer. This working principle is a cornerstone of the field of ferroelectronics, which encompasses various novel device concepts such as ferroelectric memories, ferroelectric tunnel junctions, photodetectors, neuromorphic circuits and ferroelectric FETs (FeFET).^{32–39} In addition, novel circuit design concepts are being explored, where the internal polarization state of the FeFET serves as an input parameter for a new class of ferroelectric logic gates.^{15,40–43} Recent advancements in the field have introduced ferroelectric van der Waals systems,^{44–48} which include van der Waals ferroelectric heterostructures with tunable interfacial physics.^{22,37,38,49–53} These discoveries have brought novel approaches into the field and opened up new possibilities. However, the exploration of reconfigurable ferroelectric electronics and their potential for Logic-in-Memory remains mostly uncharted territory.

In this work, we demonstrate reconfigurable ferroelectric devices based on van der Waals ferroelectric heterostructures. Our device architecture is based on a split-gates geometry and employs a layer of the CuInP_2S_6 (CIPS) van der Waals material^{54,55} as the ferroelectric gate medium. This configuration enables precise, efficient, and remanent control of the energy band profile within the WSe_2 homojunction. Our reconfigurable Ferroelectric FET (Re-FeFET) exhibits three distinct operating electronic modes: ambipolar FeFET, unipolar n-FeFET, and unipolar p-FeFET. Furthermore, we evaluate the optoelectronic properties of the Re-FeFET. It demonstrates the capability for photodetection in both phototransistor and photodiode modes. When programmed in the photodiode mode, open-circuit voltages and short-circuit photocurrents are generated, highlighting its potential for photovoltaic applications.

Finally, we explore the versatility of these tunable electronic devices by designing reconfigurable ferroelectric logic gates, which can be programmed to implement several Boolean functions (such as NAND, NOR or XOR). We conduct a comprehensive logic gate design exploration based on structure consisting of two series-connected devices. Our results demonstrate the superiority of ferroelectric reconfigurable circuits over classical CMOS circuits. In addition, we introduce a simple model for the Re-FeFET, which facilitates further circuit design exploration and behavioral simulations, while also allowing for a deeper understanding and analysis of the device's behavior in various circuit configurations.

RESULTS AND DISCUSSION

Figure 1a depicts a schematic of the van der Waals Re-FeFET studied in this work, which is constructed from the CIPS/hBN/ WSe_2 heterostructure. The fabrication process involves mechanically exfoliating and sequentially transferring flakes of CIPS, h-BN, and WSe_2 onto pre-patterned metallic back-gate electrodes. The two back-gate electrodes were patterned beforehand with a split-gate geometry and an inter-electrode spacing of 3 μm . Source and drain electrodes are then fabricated by electron-beam lithography on top of the WSe_2 channel. **Figure 1b** provides an optical image of a typical Re-FeFET device. To optimize the ferroelectric polarization while minimizing leakage currents, few-layered h-BN is used as a dielectric spacer. It also improves the transport characteristics of WSe_2 with respect to defects and trap states.^{56,57} More detailed information on the fabrication process can be found in the **Supplementary Information Section 1**. In **Figure 1c**, the micro-Raman spectrum of the van der Waals heterostructure is shown, which was obtained from a typical Re-FeFET as described in the **Methods** section. The spectrum displays the first-order in-plane and out-of-plane Raman modes of the WSe_2 bilayer sample around 249 cm^{-1} and 251 cm^{-1} , respectively. The recorded spectra reveal a complete suppression of degeneracy, and the two modes exhibit a frequency

splitting of $\sim 2 \text{ cm}^{-1}$. The ratio of A_{1g} to E'_{2g} peak intensities is about 3. The peak observed at 308 cm^{-1} (labeled as B'_{2g}) is indicative of regions with a thickness of 2 monolayers. Based on the described Raman data, the intense B'_{2g} peak confirms the bilayer behavior of the deposited WSe_2 ,^{58,59} and the splitting of the two main out-of- and in-plane modes indicates a type of stacking that can be attributed to the 3R phase. Additional micro-Raman spectra, obtained from different regions of the heterostructures with varying distinct numbers of stacked van der Waals materials, are provided in **Supplementary Information Section 2**.

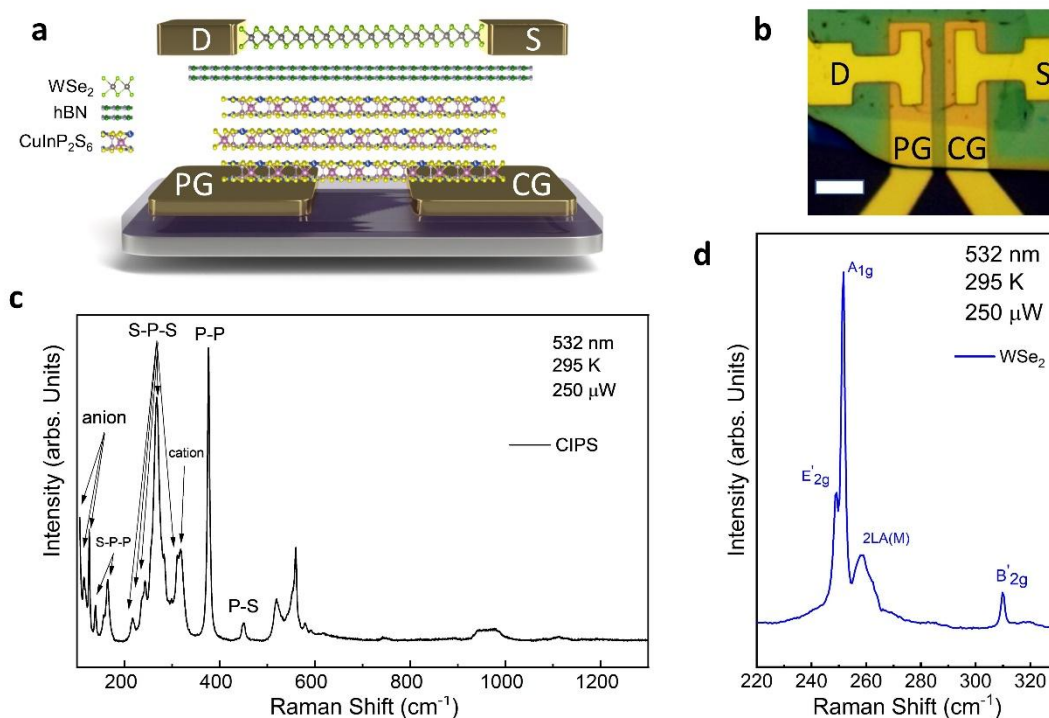


Figure 1. Van de Waals Reconfigurable Ferroelectric Field Effect Transistor. **a**, Schematic of the Re-FeFET, with split-gate architecture combined as two independent bottom gate control terminals (Program Gate and Control Gate). The van der Waals heterostructure is composed of a $\text{WSe}_2/\text{h-BN}/\text{CuInP}_2\text{S}_6$ stack. **b**, Optical microscope image of a typical FeFET device (scale bar= $10\mu\text{m}$). **c**, Micro-Raman spectra of the CuInP_2S_6 taken from a Re-FeFET device. **d**, Micro-Raman subtracted spectra of the WSe_2 channel taken from the $\text{WSe}_2/\text{hBN}/\text{CIPS}$ heterostructure region.

FERROELECTRIC FIELD EFFECT TRANSISTOR WITH RECONFIGURABLE POLARITIES

We first study how the split-gate architecture makes it possible to emulate different FeFET operating behavior depending on whether the device is operated in ambipolar or unipolar mode (cf. **Figure 2a**). Transconductance measurements under different Program Gate configurations are performed while sweeping the Control Gate bias with 10 ms long voltage pulses. The **Figure 2b** shows the transconductance of the Re-FeFET operating in a symmetric configuration while biasing both gates with the same voltage (cf. “Ambipolar FeFET mode” depicted in **Figure 2a**). This operating mode is mostly equivalent to the single-gate FeFET and is well-established.^{60,61} The remanent polarization state of the CIPS can be inverted by applying a gate voltage of opposite polarity, exceeding the ferroelectric coercive fields (V_{FE}^+ or V_{FE}^- respectively for the positive or negative sides). The polarization up (P_{up}) or down (P_{down}) leads to the accumulation of negative or positive mobile charges

within the WSe₂ channel. The Re-FeFET exhibits an ambipolar I_{ds} - V_{gs} transfer characteristic, enabling conduction in both the electron and hole accumulated regimes. Moreover, it exhibits a well-defined hysteresis loop that can be decomposed into an anti-clockwise and a clockwise hysteresis loop respectively for the n- and p- branches. Such characteristics show that the transconductance properties of the WSe₂ bilayer are driven by the CIPS ferroelectric polarization switching. The analysis of the transconductance demonstrates excellent performance, with the on/off current ratio exceeding 10⁵ (resp. 10⁴) in the p- (resp. n-) branch, and the ferroelectric window approaching a width of 10 V. These features attest to the efficient electrostatic coupling between the CIPS and the WSe₂, and the good interface quality of the van der Waals stack without dominating Fermi level pinning or trap states.⁶² Next, we investigate the reconfigurable properties of the Re-FeFET while operating it in asymmetric configurations (cf. the two “Unipolar FeFET modes” depicted in **Figure 2a**). Here, we firstly polarize the Program Gate either to the upward polarized state PG^\uparrow ($V_{PG} = +12 \text{ V} > V_{FE}^+$) or to the downward polarized state PG^\downarrow ($V_{PG} = -12 \text{ V} < -V_{FE}^-$). This enables the WSe₂ channel part positioned over the PG Gate to be set selectively to a predetermined doping state. Transconductance measurements are then performed while modulating only the Control Gate voltage V_{CG} . The Re-FeFET demonstrates now very different characteristics than those observed in the ambipolar mode: the device behaves in both asymmetric modes as unipolar-like FeFETs of opposite polarities. In the PG^\downarrow state (**Figure 2b**), the Re-FeFET mimics the behavior of a p-FeFET and shows a clockwise transconductance hysteresis with an on/off current ratio of six orders of magnitude. When programmed in the PG^\uparrow state, the device behaves as an n-FeFET, with a clockwise transconductance hysteresis with an on/off current ratio of four orders of magnitude (**Figure 2d**). For both unipolar modes, the high and low conductance states are obtained, respectively, when the homojunction is set to unipolar (p-p, or n-n) or ambipolar (p-n, or n-p) configurations.

To further illustrate the ambipolarity of the Re-FeFET, we perform density functional theory (DFT) calculations to find the relative alignment of the electronic energy levels of WSe₂ and the Ti metal contacts (see Methods for the computational details of the calculation). **Figure 2e** (left graph) depicts the WSe₂ and Ti slab components of the density of states (DOS) of a combined WSe₂-Ti system corresponding to the different states of the Re-FeFET. In **Figure 2e** (middle and right graphs), the effect of the finite surface charge of the CIPS is qualitatively illustrated by a sketch of the effective Fermi level. The WSe₂ and Ti slab components of the DOS are obtained by projecting the DFT orbitals onto atomic orbitals. In the absence of any surface charge in the CIPS, the Fermi level of the combined system lies in the middle of the WSe₂ electronic band gap (Left graph of **Figure 2e**), due to the presence of the partially filled metallic band of Ti within the gap. The choice of Ti as the contact material with its convenient level alignment to the WSe₂ bands thus allows for the efficient electrostatic doping of the WSe₂ layer with both p- and n-type carriers, leading to the achieved ambipolarity of the Re-FeFET.

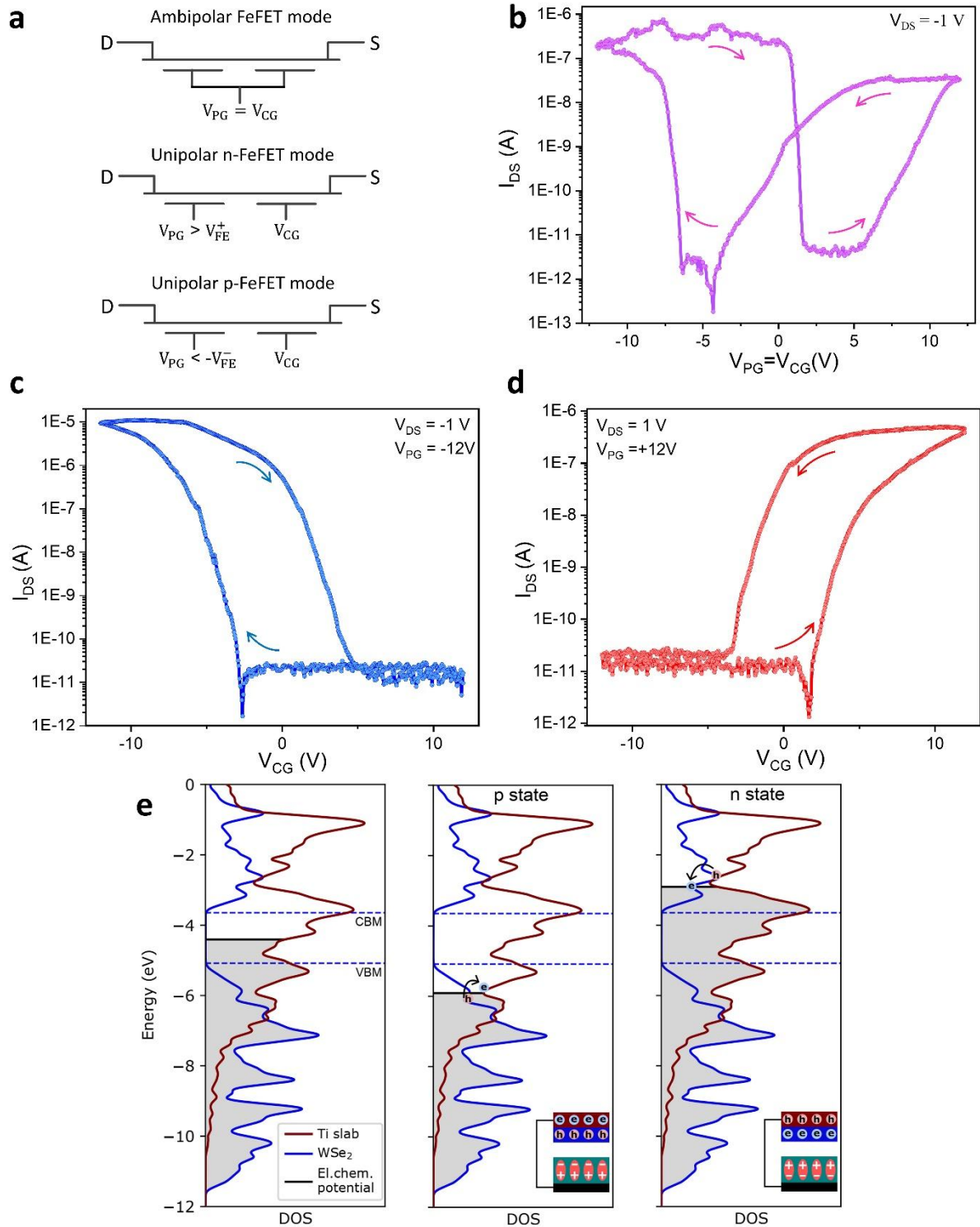


Figure 2. Ferroelectric Field Effect Transistor with reconfigurable polarities. **a**, Schematic of the various operating modes of the Re-FeFET. In the ambipolar mode, both gates are biased at the same sweeping voltage. In the unipolar n-FeFET (resp. p-FeFET) mode, the program gate V_{PG} is set above (resp. below) the positive (resp. negative) ferroelectric coercive voltage V_{FE} while the control gate voltage V_{CG} is swept. **b**, Transconductance loop of the Re-FeFET operating in the ambipolar mode and demonstrating ambipolar hysteresis with anticlockwise hysteresis in the n-branch and clockwise hysteresis in the p-branch. **c**, and **d**, show the transconductance loops of the Re-FeFET operating respectively in the p-FeFET and n-FeFET modes. The ferroelectric polarization switching of the CIPS is responsible for the anticlockwise (resp. clockwise) hysteresis of the n-FeFET (resp. p-FeFET) transconductance. **e**, Atom-projected density of states (DOS) of the combined

system of WSe_2 and Ti metal slab. (LEFT) The electrochemical potential lies within the Ti metallic band within the band gap of WSe_2 . (MIDDLE) Same as (LEFT) but for the p-doped state, illustrating the electrostatic doping of the WSe_2 layer, with the hole charge carriers supplied by the Ti reservoir. (RIGHT) same as (MIDDLE) but for the n-doped state. Inset: Sketch of the vertical stacking of the Ti contact layer (red), the WSe_2 layer, and the polarized CIPS layer (teal), which is connected to the Ti through a metal contact.

RECONFIGURABLE HOMOJUNCTION AND PHOTOVOLTAIC DIODE

We now fully explore the electrical and optoelectronic properties of the reconfigurable homojunction. We first characterize the tunability of the homojunction while investigating systematically the transport properties of the WSe_2 homojunction as a function of the drain-source (V_{DS}) and gate-source (V_{PG} , V_{CG}) bias voltages. **Figure 3a** shows the transconductance map $I_{DS}(V_{PG}, V_{CG})$ measured at fixed drain-source voltage of value 0.5V under a systematic sweep on the gate bias voltage parameters (V_{PG} , V_{CG}). Four distinct homojunction states can be identified, corresponding to the four quadrants labeled on the transconductance map: the p-p, n-n, p-n and n-p states (see corresponding energy band diagrams in **Supplementary Information Section 3**). We further characterize the rectifying capability of the homojunction with these four states and report their output characteristics in **Figure 3b**. In the unipolar states (n-n or p-p), the $I_{DS}(V_{DS})$ traces show quasi-linear behavior, while in the ambipolar states (n-p or p-n) the $I_{DS}(V_{DS})$ traces demonstrate clear non-linear rectifying characteristics. The rectification ratio (defined as the ratio of the forward current to the reverse current obtained for opposite polarities of V_{DS}) exceeds 10^4 at $V_{DS} = 1$ V in the n-p and p-n states, while it stays close to 1 in the unipolar cases (approaching respectively 1.5 and 2 for the n-n and p-p homojunctions). Such a high rectification ratio indicates the excellent quality of the p-n junction formed in WSe_2 and its efficient coupling with CIPS.

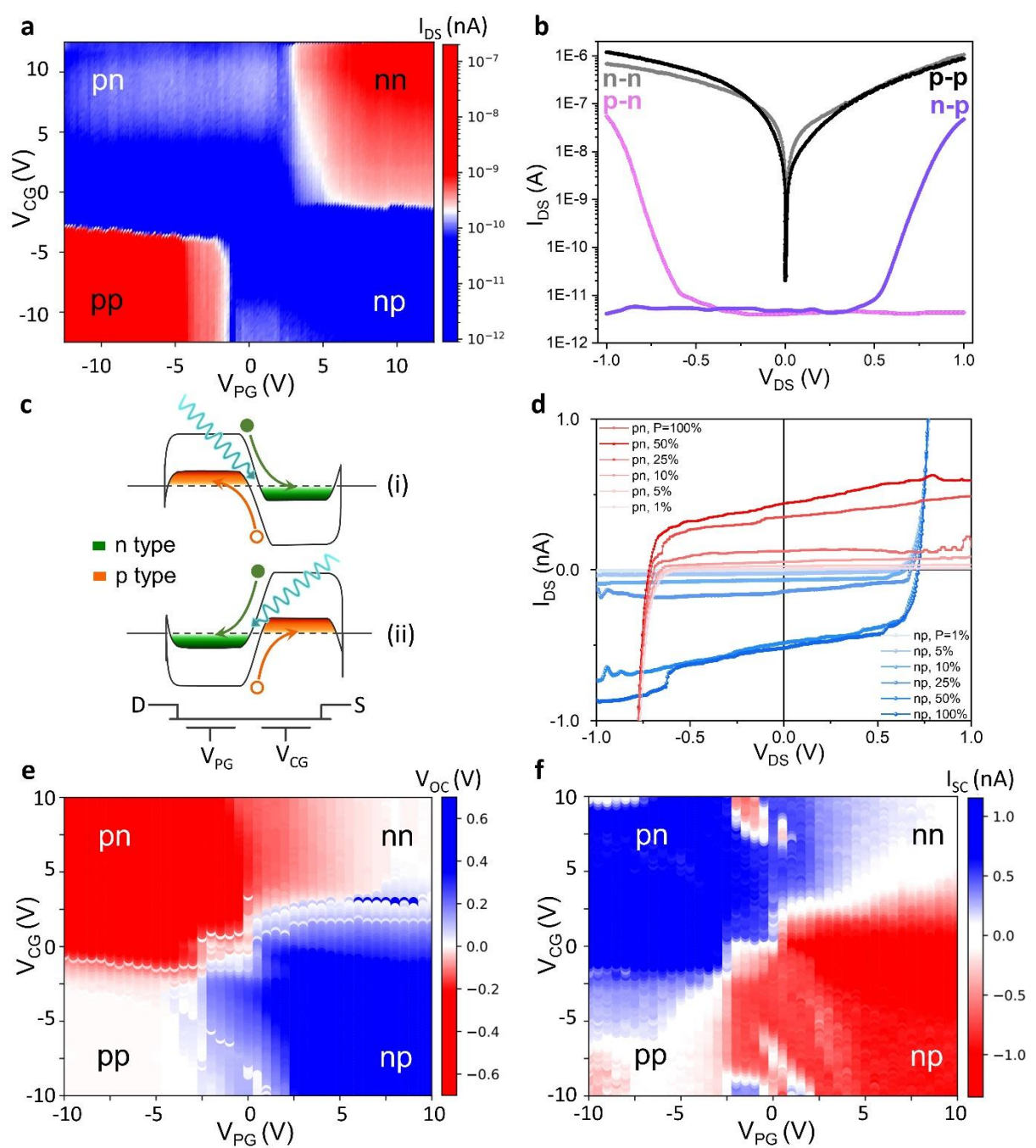


Figure 3. Electrical and optoelectronics tunable properties of the Re-FeFET. **a**, Contour map of the drain-source current I_{DS} as a function of the voltages applied to the program gate (V_{PG}) and the control gate (V_{CG}). **b**, I_{DS} - V_{DS} characteristics of the Re-FeFET programmed in the n-n (grey), p-p (black), p-n (pink) and n-p (purple) states. **c**, Energy band diagram illustrating the photovoltaic effect in (i) p-n and (ii) n-p homojunction configuration of the WSe_2 channel. **d**, Drain-source current vs voltage characteristics of the Re-FeFET programmed in p-n (red) and n-p (blue) configurations, under various light intensity “P” ($P = 0.1 \text{ mW}\cdot\text{mm}^{-2}$ at 100%, $\lambda = 522 \text{ nm}$). **e**, Color map of the open circuit voltage V_{OC} ($I_{DS} = 0 \text{ A}$) as the program (V_{PG}) and the control (V_{CG}) gates voltages are tuned independently. **f**, Color map of the short circuit photocurrent I_{SC} ($V_{DS} = 0 \text{ V}$) as the two side-gates are swept independently.

We then investigate the potential of the Re-FeFET to convert light energy into electricity by the photovoltaic effect, taking advantage of the large built-in electric field of the p-n junction to dissociate photoexcited carriers. **Figure 3c** illustrates the separation of photogenerated electron-hole pairs due to the built-in electric field formed within the WSe_2 bilayer. Upon illumination, the internal

built-in electric field dissociates the photogenerated carriers and gives rise to a photocurrent at zero applied voltage (short-circuit photocurrent, I_{SC}) and a photovoltaic voltage with zero current flow (open circuit voltage, V_{OC}). **Figure 3d** presents I–V curves under optical illumination ($\lambda = 522$ nm, $P = 0.001$ – 0.1 mW.mm⁻², see **Methods** for experimental details). When the Re-FeFET is set to a diode configuration p–n (resp. n–p), the I–V characteristics are shifted upward (resp. downward) compared to the dark characteristics. This demonstrates that the Re-FeFET operates as a photodiode. **Figure 3e** and **Figure 3f** report the color maps of the I_{SC} and the V_{OC} respectively, as a function of the split-gate parameters (V_{PG} , V_{CG}) measured under illumination conditions ($\lambda = 522$ nm, $P = 0.1$ mW.mm⁻²). The color maps precisely identify the existence of short-circuit photocurrents and open-circuit voltages with the diode states previously pinpointed in dark conditions (**Figure 3a**). When the Re-FeFET is set to a unipolar state (n–n or p–p-), no I_{SC} or V_{OC} is detected (see **Supplementary Information Section 4**). Consistently, we observe in the p–n (n–p) configuration the apparition of a large negative (positive) V_{OC} (**Figure 3d** and **Figure 3e**) and a positive (negative) I_{SC} (**Figure 3d** and **Figure 3f**). The fact that I_{SC} and V_{OC} change sign while flipping the diode polarities is a clear indication that the photoresponse does not originate from the Schottky contacts.^{17,21,63} For an optimally engineered junction profile, the maximum short-circuit photocurrent detected reaches 1.2 nA (resp. -1.3 nA) in p–n (resp. n–p) configuration, while the open circuit voltage created reaches +0.7 V (resp. -0.7 V). The photovoltaic voltages produced are among the best reported so far for WSe₂,^{17,21,64,65} and outperform alternative van der Waals doping strategies such as superionic gating⁶⁶ and contact engineering.^{67,68} This demonstrates that the Re-FeFET can also be used for energy harvesting. Moreover, the non-volatile ferroelectric control of the photodiode properties opens new prospects for in-memory sensing and computing.⁶⁹

POLYMORPHIC FERROELECTRIC AND ELECTRONIC LOGIC GATES

As mentioned before, the Re-FeFET architecture enables the programming of distinct homojunction states with different conduction levels. This naturally hints at reconfigurable Boolean logic operations. The schematic of **Figure 4a** shows a simple logic circuit built from a Re-FeFET in series with a passive load. We now investigate the reconfigurability of this logic circuit while operating it either as an electronic or a ferroelectric logic gate. In the *electronic mode*, the parameters (V_{CG} , V_{PG}) define the two input variables (schematic of **Figure 4a**). Here, V_{CG} and V_{PG} are set independently to the "1" state (resp. the "0" state) while polarizing the CIPS to the upward (resp. downward) polarization with V_{CG} or $V_{PG} > V_{FE}^+$ (resp. V_{CG} or $V_{PG} < -V_{FE}^-$). As shown in the measured output voltage V_{out} in **Figure 4a**, the Re-FeFET circuit operated in the electronic logic mode allows emulation of the XNOR logic function. In the case of the *ferroelectric mode*, the logic state is now set by the input pair (FE_{Branch} , V_{CG}). The program gate (V_{PG}) is pre-set to a fixed polarized state (either in the PG^\uparrow state or the PG^\downarrow state) as detailed in the schematics of **Figure 4b** and **Figure 4c**. The new variable FE_{Branch} is specific to ferroelectric logic.^{15,43} It is set to the "0" state (resp. the "1" state) when the FeFET is operating in the low (resp. high) threshold voltage branch of the transconductance hysteresis that transits at the negative (resp. positive) coercive field V_{FE}^- (resp. V_{FE}^+). As shown in **Figure 4b** and **Figure 4c** (see also **Supplementary Information Section 5**), the Re-FeFET logic can switch between a ferroelectric NAND (FE-NAND) and a ferroelectric AND (FE-AND) function respectively, depending on the pre-programmed FeFET state (either p- or n- type, respectively). Hence, various ferroelectric logic functions can be obtained, providing polymorphic logic functionality, which is of interest for hardware security, custom operations, and circuit design. It is important to underline that the logic gate inputs can be provided by voltage pulses. In this case, the I_{DS} current is measured after applying the various gate pulses, in open-circuit gate conditions, and the ferroelectric logic states correspond

to remanent states. The retention properties of the four homojunction states are reported in **Figure 4d** and **Figure 4e**. The Program and Control Gates have been programmed independently either in the up or down state, and subsequently grounded. The output voltage is presented as a function of time, and demonstrates successful retention after more than 10^4 seconds for each state, comparable to the best values reported so far on van der Waals ferroelectric heterostructures.⁷⁰ Such remanence is a major added value when compared with traditional CMOS-based circuits that rely on a constant supply of external voltages to maintain the desired doping levels. This represents a paradigm shift with respect to conventional von Neumann architectures, as the information processing and storing are combined in a single device. This demonstrates the promise of van der Waals ferroelectric circuits for Logic-In-Memory hardware.¹⁵

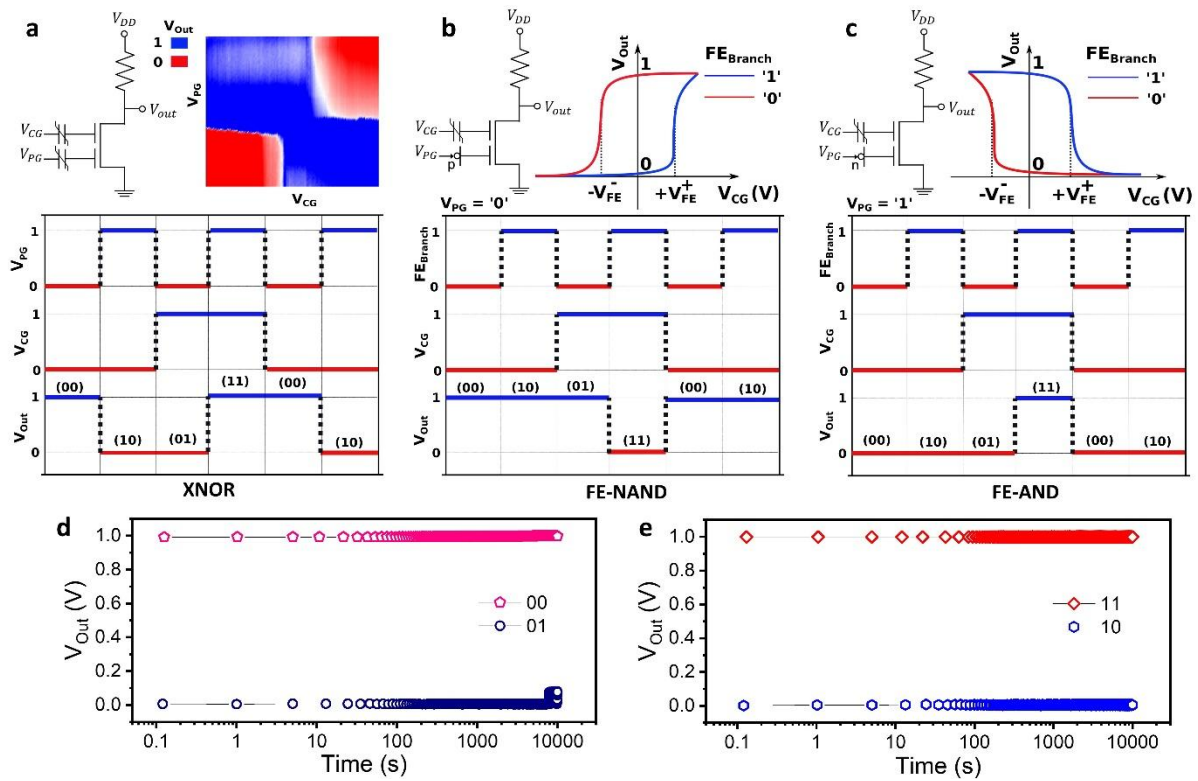


Figure 4. Polymorphic ferroelectric logic gate. **a**, Ferroelectric circuit (cf. circuit schematic) based on Re-FeFET operating in ambipolar mode, and demonstrating XNOR logic. **b**, Same circuit with the Re-FeFET programmed to the n-FeFET mode, demonstrating NAND logic. **c**, Same circuit with the Re-FeFET operating in the p-FeFET mode and showing AND logic. When used as a polymorphic ferroelectric logic gate (**a,b**), both inputs represent the in-memory state corresponding to the FE_{Branch} (cf. top schemes $V_{out}(V_{CG})$ hysteresis traces in **a**, and **b**, and the V_{CG} voltage (state '1' for $V_{FE}^+ > V_{CG} > 0$ V, state '0' for $V_{CG} > V_{FE}^+$). When operating as an electric logic gate, both inputs are provided by V_{CG} and V_{PG} terminals (cf. color plot scheme in **c**). Waveforms V_{out} vs. logic state are traced based on experimental data, with $V_{DD} = 1$ V. **d**, and **e**, show the retention properties of the four ferroelectric logic states of the Fe-XNOR gate. The output voltage (normalized respect to V_{DD} set at 0.5 Volt) was measured after the Program and Control Gates have been programmed independently either in the up or down state, and subsequently grounded.

In this section, we assess the potential of ferroelectric reconfigurable logic circuits based on Re-FeFETs through a circuit design exploration and modeling study. In order to set a framework and terminology for the analysis, we abstract the single device to a set of parameters $\{\{t, PG\}, \{X, CG\}\}$ where:

- 1- t represents the non-volatile configured type of the transistor, where $t = 0$ indicates p-type operation and $t = 1$ indicates n-type operation.
- 2- PG represents the volatile voltage applied to the program gate (also referred as polarity gate) after type configuration, causing a shift of the threshold voltage.
- 3- X represents the non-volatile polarization of the second part of the ferroelectric layer within the Re-FeFET. Here, $X = 0$ (resp. 1) corresponds to a negative (resp. positive) polarization.
- 4- CG represents the volatile voltage applied to the control gate after polarization configuration.

This parameter set for the Re-FeFET allows us to establish conditions that determine when the device is in the *On* state or the *Off* state. These conditions are summarized in the conduction table, as presented in **Figure 5a**. For more detailed explanations regarding the axioms and underlying principles used to construct this conduction table, the reader is referred to the **Supplementary Information Section 6**.

With this formalization of the Re-FeFET functionality, it becomes possible to explore the diverse logical functionalities that can be achieved with simple circuit structures. Let us consider a specific case where the circuit consists of two series-connected Re-FeFETs (shown in **Figure 5c**). By leveraging the conduction table, non-volatile logic operations can be implemented using this circuit. The process involves searching for solutions within the table that satisfy the constraints imposed by the truth table of the desired logical operation. Each solution corresponds to a unique parameter set for each Re-FeFET in the circuit ($Re-FeFET_1 = \{\{t_1, PG_1\}\{X_1, CG_1\}\}$ and $Re-FeFET_2 = \{\{t_2, PG_2\}\{X_2, CG_2\}\}$).

To create any logical or computing function, six elementary logic gates are needed: *NAND*, *NOR*, *AND*, *OR*, *NOT* and *XOR*. The conduction table provides direct implementations for *NAND* and *NOR* functions. However, the *XOR* function requires a more complex implementation. Detailed information on the implementation of *NAND*, *NOR*, and *XOR* functions are given in the **Supplementary Information Section 6**. From the *XOR* truth table, it is possible to find solutions within the conduction table by setting $n_1 = V_{dd}$ and $n_2 = gnd$, given by:

- $Re-FeFET_1 \in \{\{\bar{B}, 0\}, \{1, A\}\}, \{\{\bar{B}, A\}, \{0, 1\}\}, \{\{\bar{B}, A\}, \{1, 0\}\}\},$
- $Re-FeFET_2 \in \{\{\{B, 0\}, \{1, A\}\}, \{\{B, A\}, \{0, 1\}\}, \{\{B, A\}, \{1, 0\}\}\}.$

It is worth noting that these solutions only utilize A as the volatile operand. This implies that there is no need for an additional inverter to physically implement this circuit, unlike conventional implementations of 2-input XOR gates. Additionally, the non-volatile operand B is linked to the *type* of the Re-FeFET. Consequently, B and \bar{B} are set within each Re-FeFET using an external shared programming circuit and it is not necessary to generate \bar{B} with a local inverter. In some cases, when an n-type device is used to pass V_{dd} to the output, there can be a logic '1' degradation. To mitigate logic degradation, it is common practice to regenerate the output voltage level (usually via an inverter and/or a level restorer), either for each logic gate or for a set of cascaded logic gates.

Finally, it is demonstrated that all six elementary logic gates can be accessed using the single series-connected Re-FeFET (**Figure 5c**) circuit configuration, while keeping $n_1 = V_{dd}$ and $n_2 = gnd$. An example configuration for each logic gate implementation is depicted in **Figure 5b**. As shown in **Figure 5**, Re-FeFETs offer the advantage of very compact logic gates compared to CMOS circuits. In the case of the inverter, the same transistor-count is required for both Re-FeFET and CMOS

implementations. However, **Figure 5d** and **Figure 5e** show that for *NAND* and *NOR* gates, the Re-FeFET based circuit requires only two devices, while the equivalent CMOS circuits necessitate four transistors. In the case of the *XOR* operation presented in **Figure 5f**, the CMOS implementation typically requires 12 transistors, considering the two additional inverters required to convert *A* and *B* to their complemented forms (\bar{A} and \bar{B}). On the other hand, the Re-FeFET based *XOR* can be implemented with just two devices. This results in a significant reduction in transistor count by a factor of 6. Consequently, Re-FeFET devices offer the potential for compact circuits, which can be beneficial in a wide range of applications such as reconfigurable circuits with systematic and regular structures (such as FPGAs), or obfuscated circuits aimed at preventing reverse engineering, among others. The use of an identical basic circuit element for all logic gates provides additional advantages. Fabrication constraints are alleviated, leading to more compact and reliable chip designs. Furthermore, hardware security can be enhanced as the time-dependent power consumption of each logic gate remains identical, making it more challenging to derive information from power measurements. This inherent resilience to side channel attacks adds to the appeal of Re-FeFET-based circuits in terms of hardware security.

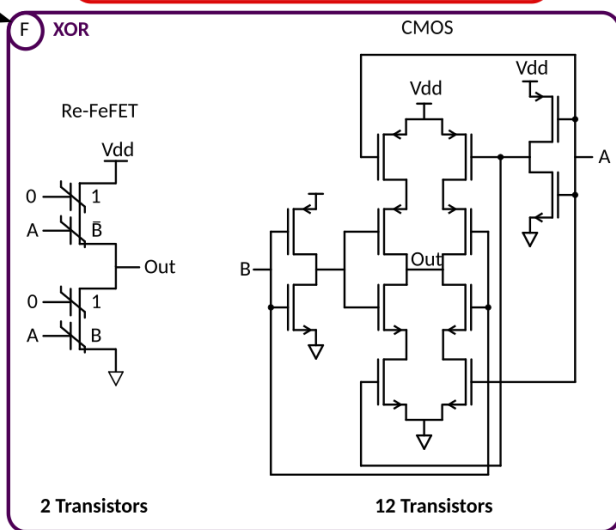
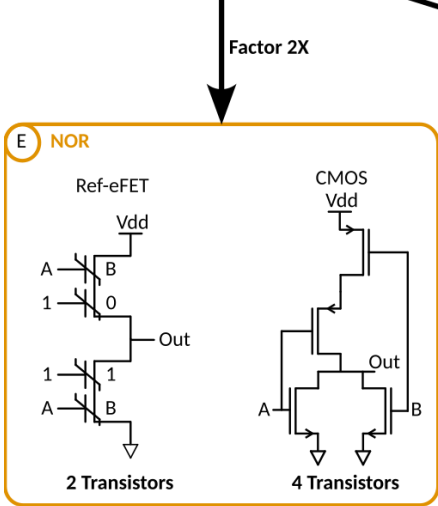
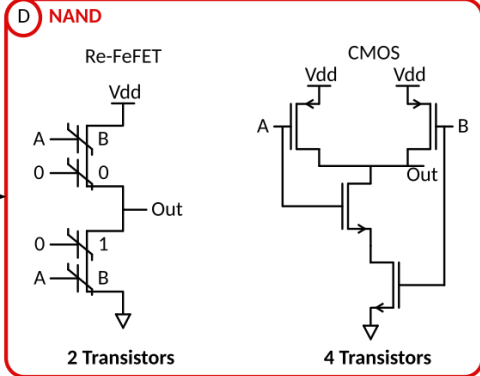
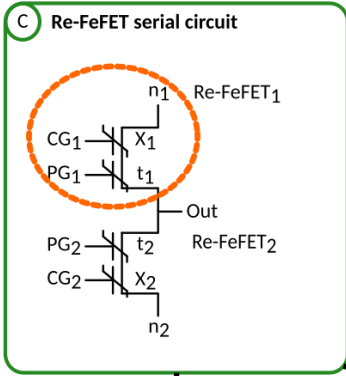
To facilitate further design considerations and enable device simulation, an equivalent circuit is created in the *Cadence* software. The details of this circuit can be found in the **Supplementary Information Figure S5**. Using this equivalent circuit, behavioral simulations of the three main logical operations (*NAND*, *NOR*, and *XOR*) are conducted. The simulation results are presented in **Figure 5g**.

A Re-FeFET conduction table

X	CG	t = 0 (p-type)		t = 1 (n-type)	
		PG = 0	PG = 1	PG = 0	PG = 1
0	0	On	On	Off	Off
0	1	On	Off	Off	On
1	0	On	Off	Off	On
1	1	Off	Off	On	On

B Re-FeFET serial circuit configuration for elementary logic gates implementation

Operation	Re-FeFET ₁				Re-FeFET ₂			
	t ₁	PG ₁	X ₁	CG ₁	t ₂	PG ₂	X ₂	CG ₂
NOT	0	1	0	A	1	1	0	A
NAND	0	0	B	A	1	0	B	A
OR	0	0	\bar{B}	\bar{A}	1	0	\bar{B}	\bar{A}
NOR	0	1	B	A	1	1	B	A
AND	0	1	\bar{B}	\bar{A}	1	1	\bar{B}	\bar{A}
XOR	\bar{B}	A	1	0	B	A	1	0



G Cadence simulation of the equivalent circuit for the 2-input NAND, NOR, and XOR

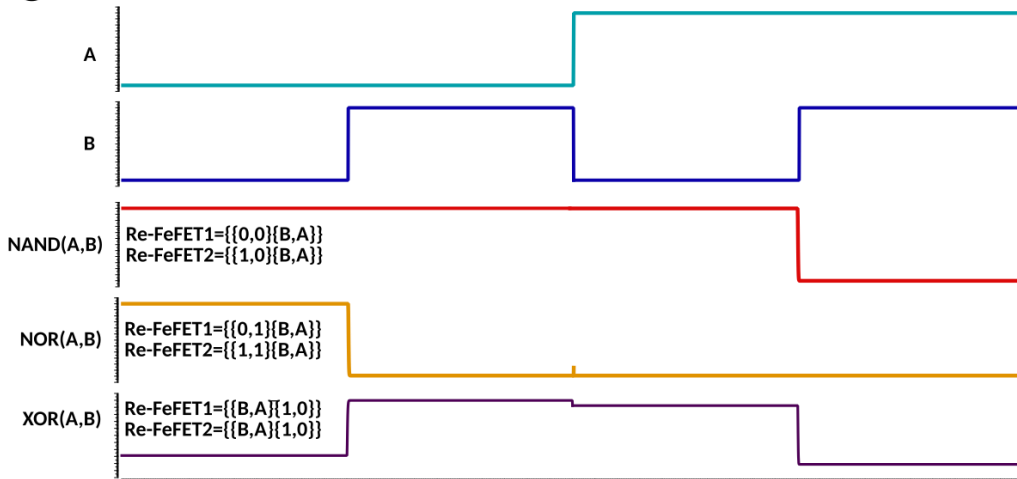


Figure 5. Implementation of NAND, NOR and XOR functions using Re-FeFETs as compared to conventional CMOS circuits. **a**, Re-FeFET conduction table specifying when the Re-FeFET is conducting (“On”) or not (“Off”) depending on the set of parameters. **b**, Table of series-connected Re-FeFET circuit (**c**,) configurations for six different logic functions (NOT, NAND, OR, NOR, AND and XOR). **c**, Ferroelectric circuit consisting of two series-connected Re-FeFETs and detailed configurations to the logic functions NAND (**d**), NOR (**e**), and XOR (**f**). For each logic function, the ferroelectric logic demonstrate superiority in terms of circuit compactness with a factor between 2 and 6. **f**, Behavioral simulations (created with the Cadence software) of the three main logic operations (NAND, NOR, XOR) performed by the in-series Re-FeFET circuit.

CONCLUSION

In conclusion, our exploration of reconfigurable ferroelectric devices based on a WSe₂ semiconducting channel controlled by split-gates and the CuInP₂S₆ van der Waals material has revealed significant properties and functionalities. We demonstrate full electrostatic control of the device by means of the split-gate electrodes. This architecture enables the precise tuning of the energy band profile along the WSe₂ channel from unipolar (n-n or p-p) to ambipolar (n-p or p-n) homojunction configurations. The Re-FeFET can be switched between p-FeFET, n-FeFET, and ambipolar-FeFET modes. Using DFT-level electronic structure calculations, we showed that the favorable alignment of the Fermi level of the Ti contacts within the band gap of the WSe₂ layer allows its electrostatic doping with both p-type and n-type carriers. With careful device engineering, the Re-FeFET demonstrates an on-off ratio of 10⁶ (10⁴) for the p-branch (n-branch), clear carrier-polarity clockwise/anticlockwise reversal of ferroelectric hysteresis and a wide memory window of up to 10 V. Additionally, the Re-FeFET can be configured as a diode (pn or np) to provide photovoltaic functionalities. The diode homojunction configurations demonstrate an excellent rectification ratio exceeding 4 order of magnitude. The observed photocurrent and large open-circuit photovoltage are attributed to the efficient electron-hole separation facilitated by the built-in electric field at the PN junction. Furthermore, we have demonstrated a proof-of-concept reconfigurable logic unit that can function either as a polymorphic ferroelectric logic or as an electronic logic unit. In the ferroelectric mode, the reconfigurable logic unit can be switched from a Fe-NAND gate to a Fe-AND gate based on the state stored in the Program Gate, and demonstrate long retention capability exceeding 10⁴ s. Such promising characteristics call for future works to explore the endurance of Re-FeFET for data-intensive applications and the effect of device downsizing. When operated in the electronic mode, the independent control of the Program and Control Gates allows for encoding the XNOR logic. We have also explored the further potential of the Re-FeFET for reconfigurable logic circuit design purposes by first formalizing the device as a set of parameters, then proposing a structure composed of two series-connected Re-FeFETs. By applying the formalized parameter set, we have analyzed various configurations of the structure to implement 2-input NOT, NAND, OR, NOR, AND, and XOR logic functions.

Our findings demonstrate that the Re-FeFET based structure enables significantly more compact circuit implementations compared to conventional CMOS circuit implementations, resulting in up to 80% reduction in transistor count. However, it will be necessary to reduce the voltages used to program and operate the Re-FeFET in future work in order to compare fairly with conventional CMOS platforms. Identified pathways include reducing the thickness of the ferroelectric layer^{46,71} and contact engineering.^{67,68} Nevertheless, the high logic expressivity enabled by the simple Re-FeFET-based circuit under study will help to reduce complexity and increase logic circuit compactness through reconfigurability. We have also validated the behavior of our logic gate using equivalent circuit-based simulations, further confirming the feasibility and performance of the Re-FeFET in logic circuit applications. This work thus establishes the foundations for future research on reconfigurable

ferroelectric devices and circuits, showcasing their potential in logic functions, reconfigurable circuits, in-memory computing, and photodetection. Our proof-of-concept device is thus a step toward the fabrication of non-volatile reconfigurable electronic circuits. We envision that ferroelectric circuits represent a large playground for heterostructure engineering with 2D materials and for nanoelectronics systems design. Hence, while the gate overlap scheme was engineered in our device, the Re-FeFET operating mechanism is also fully compatible with the gate underlap geometry. This comes with anticipated added benefits in terms of device performance and upscaling.⁷² Also, alternative ambipolar van der Waals semiconductors with smaller bandgap energy, such as black phosphorus or molybdenum ditelluride, should be investigated with expected smaller ferroelectric operating window.³¹ Furthermore, the fascinating van der Waals sliding ferroelectrics are promising candidates to enable the ferroelectric gate control down to thin layer of just few atoms.^{73,74} Finally, our results highlights the promising nature of van-der-Waals materials as a platform for engineering high-performance beyond-Moore devices. The ability of the Re-FeFET to offer multiple functionalities in a single unit (electronic, memory, optoelectronic, and photovoltaic), with reconfigurability at runtime, holds promise for both More-than-Moore and beyond-Moore strategies in the field of advanced electronics.

METHODS/EXPERIMENTAL

Optical spectroscopy measurements

Micro-Raman spectroscopy measurements were conducted at room temperature using a commercial confocal Horiba Labram Raman spectrometer operating with a laser of wavelength $\lambda = 532$ nm. The laser beam was focused onto a small spot with diameter of about 1 μm on the sample and incident power of about 250 μW . All measurements are acquired at room temperature.

Opto-electrical measurements

The high precision source meters K2634B were used for electrical characterization and gate pulse control. For the ferroelectric logic circuit, the K2182A nanovoltmeter was used to extract the voltage output parameter, while measuring the voltage drop across a resistance connected in series with the device. Voltage pulses, or combination of voltage pulses and voltage sweeps, were applied to the PG (Program Gate) and CG (Control Gate) inputs to produce different states to characterize the different gate logics (XNOR, NAND, AND). In-situ optical fiber was used for photoexcitation together with COHERENT OBIS LS/LX 522 nm source in CW-power mode.

Circuit modeling and simulation

Circuit modeling and simulation are performed using an equivalent circuit implemented in Cadence software for behavioral simulations.

DFT modeling

The DFT calculations for the level alignment of WSe_2 and the Ti contact are performed with the *PWscf* program of the *QuantumESPRESSO* suite^{75,76}. A plane-wave basis for the single-electron wave functions is used, truncated at a kinetic energy cutoff of 60 Ry. The interaction of the ionic core with the valence electrons is modeled using ultrasoft pseudopotentials from the PS library⁷⁷. The plane-wave basis for the electronic density is truncated at 540 Ry. The exchange and correlation interactions are described using the Perdew-Burke-Ernzerhof parametrization of the generalized gradient approximation.⁷⁸ The spin-orbit interaction is neglected in the interest of computational efficiency, as the density of states of WSe_2 is only marginally effected. The structures of the individual

materials were fully optimized, yielding in-plane lattice constants of 3.32 Å and 2.93 Å for WSe₂ and Ti, respectively.

To get the absolute level alignment with respect to a common vacuum level, a commensurate hexagonal supercell of a monolayer WSe₂ ($\sqrt{7} \times \sqrt{7}$), rotated by 18°, and a 10-atom thick Ti (0001) slab (3 × 3) is constructed using the CellMatch package⁷⁹ to achieve a minimal strain of 0.01%. As we are interested in finding the relative electronic level alignment of the metal and freestanding 2D semiconductor, rather than the complex potential landscape at their interface,^{80,81} the WSe₂ layer and Ti slab are separated in our simulation by a vacuum distance of 12.5 Å. For integrations over the first Brillouin zone, we use a non-shifted Monkhorst-Pack grid of 6×6×1 points. We use a Gaussian smearing for the metallic Ti states with a smearing energy of 50 meV. The Ti slab is structurally relaxed to obtain the ground state geometry of the surface. The band energies obtained using DFT are aligned by setting the electrostatic potential (ionic+Hartree) to zero at a point in the vacuum region of the supercell, equidistant from the WSe₂ layer and the Ti slab.

SUPPORTING INFORMATION

Device Fabrication and AFM characterization; Raman characterization; Reconfigurable Energy band profiles; Reconfigurable FeFET operating in Phototransistor mode; Ferroelectric logic gate measurements; Circuit design exploration with Re-FeFETs.

AUTHOR CONTRIBUTIONS

J.F.D. planned the experiments and supervised the project. A.R. fabricated the samples, lead and performed electrical measurements under the supervision of J.F.D. C.M. and I.O.C developed the ferroelectric circuit design and simulations. K.M set-up the electrical measurement bench under supervision of J.F.D and B.D. A.M. and A.O. did Raman analysis. A.R.K. and S.R. performed the first-principles calculations. T.T. and K.W. provided *h*-BN crystals. M.S. contributed to sample fabrication and electrical measurements. A.R., K.M., C.M., I.O.C. and J.F.D. analyzed the experimental and circuit design data. All authors discussed the results and their implications and commented on the manuscript. J.F.D., I.O.C. and C.M. supervised the manuscript writing.

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REFERENCES

- (1) Moore, G. E. Cramming More Components onto Integrated Circuits. *Proc. IEEE* **1998**, *86* (1), 82–85. <https://doi.org/10.1109/JPROC.1998.658762>.
- (2) Skotnicki, T.; Hutchby, J. A.; King, T. J.; Wong, H. S. P.; Boeuf, F. The End of CMOS Scaling: Toward the Introduction of New Materials and Structural Changes to Improve MOSFET Performance. *IEEE Circuits Devices Mag.* **2005**, *21* (1), 16–26. <https://doi.org/10.1109/MCD.2005.1388765>.
- (3) *IRDSTM 2022: More Moore - IEEE IRDSTM*. <https://irds.ieee.org/editions/2022/more-moore> (accessed 2023-06-16).
- (4) Ahopelto, J.; Ardila, G.; Baldi, L.; Balestra, F.; Belot, D.; Fagas, G.; De Gendt, S.; Demarchi, D.; Fernandez-Bolaños, M.; Holden, D.; Ionescu, A. M.; Meneghesso, G.; Mocuta, A.; Pfeffer, M.; Popp, R. M.; Sangiorgi, E.; Sotomayor Torres, C. M. NanoElectronics Roadmap for Europe: From Nanodevices and Innovative Materials to System Integration. *Solid. State. Electron.* **2019**, *155*, 7–19. <https://doi.org/10.1016/J.SSE.2019.03.014>.
- (5) *IRDSTM 2022: Beyond CMOS and Emerging Research Materials - IEEE IRDSTM*. <https://irds.ieee.org/editions/2022/irdsTM-2022-beyond-cmos-and-emerging-research-materials> (accessed 2023-06-16).
- (6) Mikolajick, T.; Galderisi, G.; Simon, M.; Rai, S.; Kumar, A.; Heinzig, A.; Weber, W. M.; Trommer, J. 20 Years of Reconfigurable Field-Effect Transistors: From Concepts to Future Applications. *Solid. State. Electron.* **2021**, *186*, 108036. <https://doi.org/10.1016/J.SSE.2021.108036>.
- (7) De Marchi, M.; Sacchetto, D.; Frache, S.; Zhang, J.; Gaillardon, P. E.; Leblebici, Y.; De Micheli, G. Polarity Control in Double-Gate, Gate-All-around Vertically Stacked Silicon Nanowire FETs. *Tech. Dig. - Int. Electron Devices Meet. IEDM* **2012**. <https://doi.org/10.1109/IEDM.2012.6479004>.
- (8) Raitza, M.; Kumar, A.; Völp, M.; Walter, D.; Trommer, J.; Mikolajick, T.; Weber, W. M. Exploiting Transistor-Level Reconfiguration to Optimize Combinational Circuits. *Proc. 2017 Des. Autom. Test Eur. DATE 2017* **2017**, 338–343. <https://doi.org/10.23919/DATE.2017.7927013>.
- (9) Wu, P.; Reis, D.; Hu, X. S.; Appenzeller, J. Two-Dimensional Transistors with Reconfigurable Polarities for Secure Circuits. *Nat. Electron.* **2020**, *41* (1), 45–53. <https://doi.org/10.1038/s41928-020-00511-7>.
- (10) *Securing Hardware through Reconfigurable Nano-structures (Invited Paper) | IEEE Conference Publication | IEEE Xplore*. <https://ieeexplore.ieee.org/document/10069280> (accessed 2023-04-11).
- (11) Pan, C.; Wang, C. Y.; Liang, S. J.; Wang, Y.; Cao, T.; Wang, P.; Wang, C.; Wang, S.; Cheng, B.; Gao, A.; Liu, E.; Watanabe, K.; Taniguchi, T.; Miao, F. Reconfigurable Logic and Neuromorphic Circuits Based on Electrically Tunable Two-Dimensional Homo Junctions. *Nat. Electron.* **2020**, *3* (7), 383–390. <https://doi.org/10.1038/S41928-020-0433-9>.
- (12) Tian, H.; Deng, B.; Chin, M. L.; Yan, X.; Jiang, H.; Han, S. J.; Sun, V.; Xia, Q.; Dubey, M.; Xia, F.; Wang, H. A Dynamically Reconfigurable Ambipolar Black Phosphorus Memory Device. *ACS Nano* **2016**, *10* (11), 10428–10435. https://doi.org/10.1021/ACSNANO.6B06293/SUPPL_FILE/NN6B06293_SI_001.PDF.
- (13) Sun, X.; Zhu, C.; Yi, J.; Xiang, L.; Ma, C.; Liu, H.; Zheng, B.; Liu, Y.; You, W.; Zhang, W.; Liang, D.; Shuai, Q.; Zhu, X.; Duan, H.; Liao, L.; Liu, Y.; Li, D.; Pan, A. Reconfigurable Logic-in-Memory Architectures Based on a Two-Dimensional van Der Waals Heterostructure Device. *Nat.*

- Electron.* 2022 511 **2022**, 5 (11), 752–760. <https://doi.org/10.1038/S41928-022-00858-Z>.
- (14) Huang, X.; Liu, C.; Tang, Z.; Zeng, S.; Wang, S.; Zhou, P. An Ultrafast Bipolar Flash Memory for Self-Activated in-Memory Computing. *Nat. Nanotechnol.* 2023 **2023**, 1–7. <https://doi.org/10.1038/s41565-023-01339-w>.
- (15) Marchand, C.; O'Connor, I.; Cantan, M.; Breyer, E. T.; Slesazek, S.; Mikolajick, T. FeFET Based Logic-in-Memory: An Overview. In *Proceedings - 2021 16th International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2021*; Institute of Electrical and Electronics Engineers Inc., 2021. <https://doi.org/10.1109/DTIS53253.2021.9505078>.
- (16) Gréboval, C.; Dabard, C.; Konstantinov, N.; Cavallo, M.; Chee, S. S.; Chu, A.; Dang, T. H.; Khalili, A.; Izquierdo, E.; Prado, Y.; Majjad, H.; Xu, X. Z.; Dayen, J. F.; Lhuillier, E. Split-Gate Photodiode Based on Graphene/HgTe Heterostructures with a Few Nanosecond Photoresponse. *ACS Appl. Electron. Mater.* **2021**, 3 (11), 4681–4688. <https://doi.org/10.1021/acsaelm.1c00442>.
- (17) Pospischil, A.; Furchi, M. M.; Mueller, T. Solar-Energy Conversion and Light Emission in an Atomic Monolayer p–n Diode. *Nat. Nanotechnol.* 2014 94 **2014**, 9 (4), 257–261. <https://doi.org/10.1038/nnano.2014.14>.
- (18) Buscema, M.; Groenendijk, D. J.; Steele, G. A.; Van Der Zant, H. S. J.; Castellanos-Gomez, A. Photovoltaic Effect in Few-Layer Black Phosphorus PN Junctions Defined by Local Electrostatic Gating. *Nat. Commun.* **2014**, 5 (1), 1–6. <https://doi.org/10.1038/ncomms5651>.
- (19) Fei, W.; Trommer, J.; Lemme, M. C.; Mikolajick, T.; Heinzig, A. Emerging Reconfigurable Electronic Devices Based on Two-Dimensional Materials: A Review. *InfoMat* **2022**, 4 (10), e12355. <https://doi.org/10.1002/INF2.12355>.
- (20) Noubé, U. N.; Gréboval, C.; Livache, C.; Chu, A.; Majjad, H.; Parra López, L. E.; Mouafo, L. D. N.; Doudin, B.; Berciaud, S.; Chaste, J.; Ouerghi, A.; Lhuillier, E.; Dayen, J. F. Reconfigurable 2D/0D p-n Graphene/HgTe Nanocrystal Heterostructure for Infrared Detection. *ACS Nano* **2020**, 14 (4), 4567–4576. <https://doi.org/10.1021/acsnano.0c00103>.
- (21) Baugher, B. W. H.; Churchill, H. O. H.; Yang, Y.; Jarillo-Herrero, P. Optoelectronic Devices Based on Electrically Tunable p–n Diodes in a Monolayer Dichalcogenide. *Nat. Nanotechnol.* 2014 94 **2014**, 9 (4), 262–267. <https://doi.org/10.1038/nnano.2014.25>.
- (22) Zhao, Z.; Rakheja, S.; Zhu, W. Nonvolatile Reconfigurable 2D Schottky Barrier Transistors. *Nano Lett.* **2021**, 21 (21), 9318–9324. <https://doi.org/10.1021/acs.nanolett.1c03557>.
- (23) Franklin, A. D. Nanomaterials in Transistors: From High-Performance to Thin-Film Applications. *Science (80-.)*. **2015**, 349 (6249). https://doi.org/10.1126/SCIENCE.AAB2750/ASSET/6C98D3B5-47CD-47D8-A4EF-923165ED786B/ASSETS/GRAPHIC/349_AAB2750_FA.JPEG.
- (24) Liu, C.; Chen, H.; Wang, S.; Liu, Q.; Jiang, Y. G.; Zhang, D. W.; Liu, M.; Zhou, P. Two-Dimensional Materials for next-Generation Computing Technologies. *Nature Nanotechnology*. Nature Research July 1, 2020, pp 545–557. <https://doi.org/10.1038/s41565-020-0724-3>.
- (25) Fiori, G.; Bonaccorso, F.; Iannaccone, G.; Palacios, T.; Neumaier, D.; Seabaugh, A.; Banerjee, S. K.; Colombo, L. Electronics Based on Two-Dimensional Materials. *Nat. Nanotechnol.* 2014 910 **2014**, 9 (10), 768–779. <https://doi.org/10.1038/nnano.2014.207>.
- (26) Akinwande, D.; Huyghebaert, C.; Wang, C. H.; Serna, M. I.; Goossens, S.; Li, L. J.; Wong, H. S. P.; Koppens, F. H. L. Graphene and Two-Dimensional Materials for Silicon Technology. *Nature*. Nature Publishing Group September 26, 2019, pp 507–518. <https://doi.org/10.1038/s41586->

019-1573-9.

- (27) Jariwala, D.; Marks, T. J.; Hersam, M. C. Mixed-Dimensional van Der Waals Heterostructures. *Nat. Publ. Gr.* **2016**, *16*. <https://doi.org/10.1038/NMAT4703>.
- (28) Novoselov, K. S.; Mishchenko, A.; Carvalho, A.; Castro Neto, A. H. 2D Materials and van Der Waals Heterostructures. *Science (80-.)*. **2016**, *353* (6298). https://doi.org/10.1126/SCIENCE.AAC9439/ASSET/4B54077E-F0A2-4BB2-BFA1-BC557DC78A9D/ASSETS/GRAPHIC/353_AAC9439_F6.JPEG.
- (29) Briggs, N.; Subramanian, S.; Lin, Z.; Li, X.; Zhang, X.; Zhang, K.; Xiao, K.; Geohegan, D.; Wallace, R.; Chen, L. Q.; Terrones, M.; Ebrahimi, A.; Das, S.; Redwing, J.; Hinkle, C.; Momeni, K.; Van Duin, A.; Crespi, V.; Kar, S.; Robinson, J. A. A Roadmap for Electronic Grade 2D Materials. *2D Mater.* **2019**, *6* (2), 022001. <https://doi.org/10.1088/2053-1583/AAF836>.
- (30) Yang, H.; Valenzuela, S. O.; Chshiev, M.; Couet, S.; Dieny, B.; Dlubak, B.; Fert, A.; Garello, K.; Jamet, M.; Jeong, D. E.; Lee, K.; Lee, T.; Martin, M. B.; Kar, G. S.; S  n  or, P.; Shin, H. J.; Roche, S. Two-Dimensional Materials Prospects for Non-Volatile Spintronic Memories. *Nat.* **2022**, *606* (7915), 663–673. <https://doi.org/10.1038/s41586-022-04768-0>.
- (31) Hu, W.; Sheng, Z.; Hou, X.; Chen, H.; Zhang, Z.; Zhang, D. W.; Zhou, P. Ambipolar 2D Semiconductors and Emerging Device Applications. *Small Methods* **2021**, *5* (1), 2000837. <https://doi.org/10.1002/SMTD.202000837>.
- (32) Martin, L. W.; Rappe, A. M. Thin-Film Ferroelectric Materials and Their Applications. *Nature Reviews Materials*. Nature Publishing Group November 15, 2016. <https://doi.org/10.1038/natrevmats.2016.87>.
- (33) Chanthbouala, A.; Garcia, V.; Cherifi, R. O.; Bouzouane, K.; Fusil, S.; Moya, X.; Xavier, S.; Yamada, H.; Deranlot, C.; Mathur, N. D.; Bibes, M.; Barth  l  my, A.; Grollier, J. A Ferroelectric Memristor. *Nat. Mater.* **2012**, *11* (10), 860–864. <https://doi.org/10.1038/nmat3415>.
- (34) Khan, A. I.; Keshavarzi, A.; Datta, S. The Future of Ferroelectric Field-Effect Transistor Technology. *Nature Electronics*. Nature Research October 1, 2020, pp 588–597. <https://doi.org/10.1038/s41928-020-00492-7>.
- (35) Garcia, V.; Fusil, S.; Bouzouane, K.; Enouz-Vedrenne, S.; Mathur, N. D.; Barth  l  my, A.; Bibes, M. Giant Tunnel Electroresistance for Non-Destructive Readout of Ferroelectric States. *Nature* **2009**, *460* (7251), 81–84. <https://doi.org/10.1038/nature08128>.
- (36) Gruverman, A.; Wu, D.; Lu, H.; Wang, Y.; Jang, H. W.; Folkman, C. M.; Zhuravlev, M. Y.; Felker, D.; Rzchowski, M.; Eom, C. B.; Tsymbal, E. Y. Tunneling Electroresistance Effect in Ferroelectric Tunnel Junctions at the Nanoscale. *Nano Lett.* **2009**, *9* (10), 3539–3543. https://doi.org/10.1021/NL901754T/ASSET/IMAGES/MEDIUM/NL-2009-01754T_0005.GIF.
- (37) Soliman, M.; Maity, K.; Gloppe, A.; Mahmoudi, A.; Ouerghi, A.; Doudin, B.; Kundys, B.; Dayen, J.-F. Photoferroelectric All-van-Der-Waals Heterostructure for Multimode Neuromorphic Ferroelectric Transistors. *ACS Appl. Mater. Interfaces* **2023**, *15* (12), 15732. https://doi.org/10.1021/ACSAMI.3C00092/SUPPL_FILE/AM3C00092_SI_001.PDF.
- (38) Luo, Z. D.; Xia, X.; Yang, M. M.; Wilson, N. R.; Gruverman, A.; Alexe, M. Artificial Optoelectronic Synapses Based on Ferroelectric Field-Effect Enabled 2D Transition Metal Dichalcogenide Memristive Transistors. *ACS Nano* **2020**, *14* (1), 746–754. <https://doi.org/10.1021/acsnano.9b07687>.
- (39) Cavallo, M.; Bossavit, E.; Matzen, S.; Maroutian, T.; Alchaar, R.; Dang, T. H.; Khalili, A.; Dabard, C.; Zhang, H.; Prado, Y.; Abadie, C.; Utterback, J. K.; Dayen, J. F.; Silly, M. G.; Dudin, P.; Avila, J.;

- Lhuillier, E.; Pierucci, D. Coupling Ferroelectric to Colloidal Nanocrystals as a Generic Strategy to Engineer the Carrier Density Landscape. *Adv. Funct. Mater.* **2023**, *33* (34), 2300846. <https://doi.org/10.1002/adfm.202300846>.
- (40) Chen, X.; Ni, K.; Niemier, M. T.; Reis, D.; Sun, X.; Wang, P.; Datta, S.; Hu, X. S.; Yin, X.; Jerry, M.; Yu, S.; Laguna, A. F. The Impact of Ferroelectric FETs on Digital and Analog Circuits and Architectures. *IEEE Des. Test* **2020**, *37* (1), 79–99. <https://doi.org/10.1109/MDAT.2019.2944094>.
- (41) Breyer, E. T.; Mulaosmanovic, H.; Mikolajick, T.; Slesazek, S. Reconfigurable NAND/NOR Logic Gates in 28 Nm HKMG and 22 Nm FD-SOI FeFET Technology. In *Technical Digest - International Electron Devices Meeting, IEDM*; Institute of Electrical and Electronics Engineers Inc., 2018; pp 28.5.1-28.5.4. <https://doi.org/10.1109/IEDM.2017.8268471>.
- (42) Mikolajick, T.; Schroeder, U.; Slesazek, S. The Past, the Present, and the Future of Ferroelectric Memories. *IEEE Trans. Electron Devices* **2020**, *67* (4), 1434–1443. <https://doi.org/10.1109/TED.2020.2976148>.
- (43) Yin, X.; Chen, X.; Niemier, M.; Hu, X. S. Ferroelectric FETs-Based Nonvolatile Logic-in-Memory Circuits. *IEEE Trans. Very Large Scale Integr. Syst.* **2019**, *27* (1), 159–172. <https://doi.org/10.1109/TVLSI.2018.2871119>.
- (44) Ryu, H.; Xu, K.; Li, D.; Hong, X.; Zhu, W. Empowering 2D Nanoelectronics via Ferroelectricity. *Applied Physics Letters*. American Institute of Physics Inc. August 24, 2020. <https://doi.org/10.1063/5.0019555>.
- (45) Si, M.; Saha, A. K.; Gao, S.; Qiu, G.; Qin, J.; Duan, Y.; Jian, J.; Niu, C.; Wang, H.; Wu, W.; Gupta, S. K.; Ye, P. D. A Ferroelectric Semiconductor Field-Effect Transistor. *Nat. Electron.* **2019**, *2* (12), 580–586. <https://doi.org/10.1038/s41928-019-0338-7>.
- (46) Liu, F.; You, L.; Seyler, K. L.; Li, X.; Yu, P.; Lin, J.; Wang, X.; Zhou, J.; Wang, H.; He, H.; Pantelides, S. T.; Zhou, W.; Sharma, P.; Xu, X.; Ajayan, P. M.; Wang, J.; Liu, Z. Room-Temperature Ferroelectricity in CuInP2S6 Ultrathin Flakes. *Nat. Commun.* **2016**, *7*, 12357. <https://doi.org/10.1038/ncomms12357>.
- (47) Qi, L.; Ruan, S.; Zeng, Y. Review on Recent Developments in 2D Ferroelectrics: Theories and Applications. *Adv. Mater.* **2021**, *33* (13), 2005098. <https://doi.org/10.1002/adma.202005098>.
- (48) Sun, Y.; Niu, G.; Ren, W.; Meng, X.; Zhao, J.; Luo, W.; Ye, Z. G.; Xie, Y. H. Hybrid System Combining Two-Dimensional Materials and Ferroelectrics and Its Application in Photodetection. *ACS Nano*. American Chemical Society July 27, 2021, pp 10982–11013. <https://doi.org/10.1021/acsnano.1c01735>.
- (49) Jin, T.; Mao, J.; Gao, J.; Han, C.; Loh, K. P.; Wee, A. T. S.; Chen, W. Ferroelectrics-Integrated Two-Dimensional Devices toward Next-Generation Electronics. *ACS Nano* **2022**. <https://doi.org/10.1021/acsnano.2c07281>.
- (50) Wang, C. C. Y. C. C. Y.; Wang, C. C. Y. C. C. Y.; Meng, F.; Wang, P.; Wang, S.; Liang, S. J.; Miao, F. 2D Layered Materials for Memristive and Neuromorphic Applications. *Adv. Electron. Mater.* **2020**, *6* (2). <https://doi.org/10.1002/AELM.201901107>.
- (51) Cao, G.; Meng, P.; Chen, J.; Liu, H.; Bian, R.; Zhu, C.; Liu, F.; Liu, Z. *2D Material Based Synaptic Devices for Neuromorphic Computing*; Wiley-VCH Verlag, 2021; Vol. 31, p 2005443. <https://onlinelibrary.wiley.com/doi/10.1002/adfm.202005443> (accessed 2022-08-24).
- (52) Wang, X.; Yu, P.; Lei, Z.; Zhu, C.; Cao, X.; Liu, F.; You, L.; Zeng, Q.; Deng, Y.; Zhu, C.; Zhou, J.; Fu, Q.; Wang, J.; Huang, Y.; Liu, Z. Van Der Waals Negative Capacitance Transistors. *Nat. Commun.*

2019, 10 (1), 1–8. <https://doi.org/10.1038/s41467-019-10738-4>.

- (53) Wu, J.; Chen, H. Y.; Yang, N.; Cao, J.; Yan, X.; Liu, F.; Sun, Q.; Ling, X.; Guo, J.; Wang, H. High Tunnelling Electroresistance in a Ferroelectric van Der Waals Heterojunction via Giant Barrier Height Modulation. *Nat. Electron.* **2020**, 3 (8), 466–472. <https://doi.org/10.1038/s41928-020-0441-9>.
- (54) Belianinov, A.; He, Q.; Dziaugys, A.; Maksymovych, P.; Eliseev, E.; Borisevich, A.; Morozovska, A.; Banyas, J.; Vysochanskii, Y.; Kalinin, S. V. CuInP_2S_6 Room Temperature Layered Ferroelectric. *Nano Lett.* **2015**, 15 (6), 3808–3814. <https://doi.org/10.1021/acs.nanolett.5b00491>.
- (55) Brehm, J. A.; Neumayer, S. M.; Tao, L.; O’Hara, A.; Chyasnavichus, M.; Susner, M. A.; McGuire, M. A.; Kalinin, S. V.; Jesse, S.; Ganesh, P.; Pantelides, S. T.; Maksymovych, P.; Balke, N. Tunable Quadruple-Well Ferroelectric van Der Waals Crystals. *Nat. Mater.* **2020**, 19 (1), 43–48. <https://doi.org/10.1038/s41563-019-0532-z>.
- (56) Rhodes, D.; Chae, S. H.; Ribeiro-Palau, R.; Hone, J. Disorder in van Der Waals Heterostructures of 2D Materials. *Nature Materials*. Nature Publishing Group June 1, 2019, pp 541–549. <https://doi.org/10.1038/s41563-019-0366-8>.
- (57) Illarionov, Y. Y.; Knobloch, T.; Jech, M.; Lanza, M.; Akinwande, D.; Vexler, M. I.; Mueller, T.; Lemme, M. C.; Fiori, G.; Schwierz, F.; Grassler, T. Insulators for 2D Nanoelectronics: The Gap to Bridge. *Nature Communications*. Nature Research December 1, 2020, pp 1–15. <https://doi.org/10.1038/s41467-020-16640-8>.
- (58) Mahmoudi, A.; Bouaziz, M.; Chiout, A.; Di Berardino, G.; Ullberg, N.; Kremer, G.; Dudin, P.; Avila, J.; Silly, M.; Derycke, V.; Romanin, D.; Pala, M.; Gerber, I. C.; Chaste, J.; Oehler, F.; Ouerghi, A. Electronic Properties of Rhombohedrally Stacked Bilayer WSe₂ Obtained by Chemical Vapor Deposition. *Phys. Rev. B* **2023**, 108 (4), 045417. <https://doi.org/10.1103/PhysRevB.108.045417>.
- (59) Li, Z.; Förste, J.; Watanabe, K.; Taniguchi, T.; Urbaszek, B.; Baimuratov, A. S.; Gerber, I. C.; Högele, A.; Bilgin, I. Stacking-Dependent Exciton Multiplicity in WSe₂ Bilayers. *Phys. Rev. B* **2022**, 106 (4), 045411. <https://doi.org/10.1103/PhysRevB.106.045411>.
- (60) Miller, S. L.; McWhorter, P. J. Physics of the Ferroelectric Nonvolatile Memory Field Effect Transistor. *J. Appl. Phys.* **1992**, 72 (12), 5999–6010. <https://doi.org/10.1063/1.351910>.
- (61) Kim, J. Y.; Choi, M. J.; Jang, H. W. Ferroelectric Field Effect Transistors: Progress and Perspective. *APL Mater.* **2021**, 9 (2). <https://doi.org/10.1063/5.0035515>.
- (62) Liu, X.; Choi, M. S.; Hwang, E.; Yoo, W. J.; Sun, J. Fermi Level Pinning Dependent 2D Semiconductor Devices: Challenges and Prospects. *Adv. Mater.* **2022**, 34 (15), 2108425. <https://doi.org/10.1002/adma.202108425>.
- (63) Fontana, M.; Deppe, T.; Boyd, A. K.; Rinzan, M.; Liu, A. Y.; Paranjape, M.; Barbara, P. Electron-Hole Transport and Photovoltaic Effect in Gated MoS₂ Schottky Junctions. *Sci. Rep.* **2013**, 3, 1634. <https://doi.org/10.1038/srep01634>.
- (64) Long, M.; Wang, P.; Fang, H.; Hu, W. Progress, Challenges, and Opportunities for 2D Material Based Photodetectors. *Adv. Funct. Mater.* **2018**, 1803807. <https://doi.org/10.1002/adfm.201803807>.
- (65) Groenendijk, D. J.; Buscema, M.; Steele, G. A.; Michaelis De Vasconcellos, S.; Bratschitsch, R.; Van Der Zant, H. S. J.; Castellanos-Gomez, A. Photovoltaic and Photothermoelectric Effect in a Double-Gated WSe₂ Device. *Nano Lett.* **2014**, 14 (10), 5846–5852. <https://doi.org/10.1021/nl502741k>.

- (66) Lee, S. J.; Lin, Z.; Huang, J.; Choi, C. S.; Chen, P.; Liu, Y.; Guo, J.; Jia, C.; Wang, Y.; Wang, L.; Liao, Q.; Shakir, I.; Duan, X.; Dunn, B.; Zhang, Y.; Huang, Y.; Duan, X. Programmable Devices Based on Reversible Solid-State Doping of Two-Dimensional Semiconductors with Superionic Silver Iodide. *Nat. Electron.* **2020**, *3* (10), 630–637. <https://doi.org/10.1038/s41928-020-00472-x>.
- (67) Du, J.; Liao, Q.; Liu, B.; Zhang, X.; Yu, H.; Ou, Y.; Xiao, J.; Kang, Z.; Si, H.; Zhang, Z.; Zhang, Y. Gate-Controlled Polarity-Reversible Photodiodes with Ambipolar 2D Semiconductors. *Adv. Funct. Mater.* **2021**, *31* (8), 2007559. <https://doi.org/10.1002/adfm.202007559>.
- (68) Kim, K. H.; Andreev, M.; Choi, S.; Shim, J.; Ahn, H.; Lynch, J.; Lee, T.; Lee, J.; Nazif, K. N.; Kumar, A.; Kumar, P.; Choo, H.; Jariwala, D.; Saraswat, K. C.; Park, J. H. High-Efficiency WSe₂ Photovoltaic Devices with Electron-Selective Contacts. *ACS Nano* **2022**, *16* (6), 8827–8836. <https://doi.org/10.1021/acsnano.1c10054>.
- (69) Wu, G.; Zhang, X.; Feng, G.; Wang, J.; Zhou, K.; Zeng, J.; Dong, D.; Zhu, F.; Yang, C.; Zhao, X.; Gong, D.; Zhang, M.; Tian, B.; Duan, C.; Liu, Q.; Wang, J.; Chu, J.; Liu, M. Ferroelectric-Defined Reconfigurable Homojunctions for in-Memory Sensing and Computing. *Nat. Mater.* **2023**, 1–8. <https://doi.org/10.1038/s41563-023-01676-0>.
- (70) Wang, X.; Zhu, C.; Deng, Y.; Duan, R.; Chen, J.; Zeng, Q.; Zhou, J.; Fu, Q.; You, L.; Liu, S.; Edgar, J. H.; Yu, P.; Liu, Z. Van Der Waals Engineering of Ferroelectric Heterostructures for Long-Retention Memory. *Nat. Commun.* **2021**, *12* (1). <https://doi.org/10.1038/s41467-021-21320-2>.
- (71) Wang, C. I.; Chen, H. Y.; Wang, C. Y.; Chang, T. J.; Jiang, Y. Sen; Chang, C. S.; Chen, M. J. Evolution of Pronounced Ferroelectricity in Hf_{0.5}Zr_{0.5}O₂ thin Films Scaled down to 3 Nm. *J. Mater. Chem. C* **2021**, *9* (37), 12759–12767. <https://doi.org/10.1039/d1tc01778k>.
- (72) Trivedi, V.; Fossum, J. G.; Chowdhury, M. M. Nanoscale FinFETs with Gate-Source/Drain Underlap. *IEEE Trans. Electron Devices* **2005**, *52* (1), 56–62. <https://doi.org/10.1109/TED.2004.841333>.
- (73) Wu, M.; Li, J. Sliding Ferroelectricity in 2D van Der Waals Materials: Related Physics and Future Opportunities. *Proceedings of the National Academy of Sciences of the United States of America*. National Academy of Sciences December 14, 2021, p e2115703118. <https://doi.org/10.1073/pnas.2115703118>.
- (74) Bian, R.; Cao, G.; Pan, E.; Liu, Q.; Li, Z.; Liang, L.; Wu, Q.; Ang, L. K.; Li, W.; Zhao, X.; Liu, F. High-Performance Sliding Ferroelectric Transistor Based on Schottky Barrier Tuning. *Nano Lett.* **2023**, *23* (10), 4595–4601. <https://doi.org/10.1021/acs.nanolett.3c01053>.
- (75) Giannozzi, P.; Baroni, S.; Bonini, N.; Calandra, M.; Car, R.; Cavazzoni, C.; Chiarotti, G. L.; Cococcioni, M.; Dabo, I.; Corso, A. D.; Gironcoli, S. de; Fabris, S.; Fratesi, G.; Gebauer, R.; Gerstmann, U.; Gougoussis, C.; Lazzeri, M.; Martin-Samos, L.; Marzari, N.; Mauri, F.; Mazzarello, R.; Pasquarello, A.; Paulatto, L.; Sbraccia, C.; Scandolo, S.; Sclauzero, G.; Seitsonen, A. P.; Smogunov, A.; Umari, P.; Wentzcovitch, R. M. QUANTUM ESPRESSO: A Modular and Open-Source Software Project for Quantum Simulations of Materials. *J. Phys. Condens. Matter* **2009**, *21* (39), 395502. <https://doi.org/10.1088/0953-8984/21/39/395502>.
- (76) Giannozzi, P.; Andreussi, O.; Brumme, T.; Bunau, O.; Nardelli, M. B.; Calandra, M.; Car, R.; Cavazzoni, C.; Ceresoli, D.; Cococcioni, M.; Colonna, N.; Carnimeo, I.; Corso, A. D.; de Gironcoli, S.; Delugas, P.; DiStasio, R. A.; Ferretti, A.; Floris, A.; Fratesi, G.; Fugallo, G.; Gebauer, R.; Gerstmann, U.; Giustino, F.; Gorni, T.; Jia, J.; Kawamura, M.; Ko, H.-Y.; Kokalj, A.; Küçükbenli, E.; Lazzeri, M.; Marsili, M.; Marzari, N.; Mauri, F.; Nguyen, N. L.; Nguyen, H.-V.; Otero-de-la-Roza, A.; Paulatto, L.; Poncé, S.; Rocca, D.; Sabatini, R.; Santra, B.; Schlipf, M.; Seitsonen, A. P.; Smogunov, A.; Timrov, I.; Thonhauser, T.; Umari, P.; Vast, N.; Wu, X.; Baroni, S. Advanced

- Capabilities for Materials Modelling with Quantum ESPRESSO. *J. Phys. Condens. Matter* **2017**, 29 (46). <https://doi.org/10.1088/1361-648X/aa8f79>.
- (77) Dal Corso, A. Pseudopotentials Periodic Table: From H to Pu. *Comput. Mater. Sci.* **2014**, 95, 337–350. <https://doi.org/10.1016/j.commatsci.2014.07.043>.
- (78) Perdew, J. P.; Burke, K.; Ernzerhof, M. Generalized Gradient Approximation Made Simple. *Phys. Rev. Lett.* **1996**, 77 (18), 3865–3868. <https://doi.org/10.1103/PhysRevLett.77.3865>.
- (79) Lazić, P. CellMatch: Combining Two Unit Cells into a Common Supercell with Minimal Strain. *Comput. Phys. Commun.* **2015**, 197, 324–334. <https://doi.org/10.1016/j.cpc.2015.08.038>.
- (80) Kang, J.; Liu, W.; Sarkar, D.; Jena, D.; Banerjee, K. Computational Study of Metal Contacts to Monolayer Transition-Metal Dichalcogenide Semiconductors. *Physical Review X*. American Physical Society July 14, 2014, p 031005. <https://doi.org/10.1103/PhysRevX.4.031005>.
- (81) Chen, J.; Zhang, Z.; Guo, Y.; Robertson, J. Metal Contacts with Moire Interfaces on WSe₂ for Ambipolar Applications. *Appl. Phys. Lett.* **2022**, 121 (5). <https://doi.org/10.1063/5.0091504>.