



High-efficiency GaAs solar cells grown on porous germanium substrate with PEELER technology

Valentin Daniel, Thomas Bidaud, Jérémie Chretien, Nicolas Paupy, Ahmed Ayari, Thierno Mamoudou Diallo, Tadeáš Hanuš, Jonathan Henriques, Abdelatif Jaouad, Jean-François Lerat, et al.

► To cite this version:

Valentin Daniel, Thomas Bidaud, Jérémie Chretien, Nicolas Paupy, Ahmed Ayari, et al.. High-efficiency GaAs solar cells grown on porous germanium substrate with PEELER technology. Solar RRL, 2023, 10.1002/solr.202300643 . hal-04298914

HAL Id: hal-04298914

<https://hal.science/hal-04298914>

Submitted on 13 Dec 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

High-Efficiency GaAs Solar Cells Grown on Porous Germanium Substrate with PEELER Technology

Valentin Daniel,* Thomas Bidaud, Jérémie Chretien, Nicolas Paupy, Ahmed Ayari, Thieno Mamoudou Diallo, Tadeáš Hanuš, Jonathan Henriques, Abdelatif Jaouad, Jean-François Lerat, Bouraoui Ilahi, Jinyoun Cho, Kristof Dessein, Christian Dubuc, Gwenaelle Hamon,* Abderraouf Boucherif,* and Maxime Darnon*

III–V solar cells are mainly grown on GaAs or Ge substrate, which significantly contributes to the final cost and affects the sustainable use of these rare materials. A so-called PEELER process is developed, in which a porosification technique is used to create a weak layer between a Ge substrate and the epitaxial layers. This method enables the separation of the grown layers, allowing for the subsequent reuse of germanium and a reduction in the environmental and economic cost of optoelectronic devices. Technology validation using the device performance is important to assess the technology interest. For this purpose, the performance of 22 nondetached single-junction GaAs photovoltaic cells grown and manufactured on porousified 100 mm Ge wafer without antireflection coating is fabricated and compared. All the cells exhibit comparable performance to state-of-the-art GaAs solar cells (grown on Ge or GaAs) with high efficiency ($21.8\% \pm 0.78\%$) and thereby demonstrate the viability of growing high-performance optoelectronic devices on detachable Ge films.

achieved by separating the substrate and the functional layers, reducing the amount of material used in the final device. Different processes have already been developed with this aim such as spalling,^[2,3] selective etching,^[4–7] reactive ion etching (RIE)-based porosification,^[8] or van der Waals epitaxy.^[9] First developed on silicon,^[10,11] another promising low-cost approach consists of electrochemical porosification of the substrate followed by epitaxy and annealing (porous germanium efficient epitaxial layer release: PEELER)^[12,13] allowing for epilayers separation and reconditioning of the substrate.^[14–16] Using this method, as detailed in **Figure 1**, we present in this work the fabrication of III–V (GaAs) single-junction solar cells grown by metal organic chemical vapor

deposition (MOCVD) on a 100 mm wide porousified germanium substrate.

1. Introduction

Top-performing industrial solar cells are composed of a stack of groups III–V and group IV materials (InGaP, GaInAs, Ge, GaAs, etc.) on germanium substrates. These devices are costly because the component elements are rare. The substrate itself accounts for more than 30% of the cost of cell fabrication.^[1] Thus, to reduce the overall cost of these III–V and germanium-based devices, the Ge thickness must be reduced. This can be

2. Methodology

2.1. Porosification and Epitaxy

A bipolar electrochemical etching has been applied to create a few hundred nanometers-thick “sponge-like” porous structure

V. Daniel, T. Bidaud, J. Chretien, N. Paupy, A. Ayari, T. M. Diallo, T. Hanuš, J. Henriques, A. Jaouad, J.-F. Lerat, B. Ilahi, G. Hamon, A. Boucherif, M. Darnon

Institut Interdisciplinaire d’Innovation Technologique (3IT)
Université de Sherbrooke
3000 boulevard de l’Université, Sherbrooke, Québec J1K 0A5, Canada
E-mail: valentin.daniel@usherbrooke.ca;
gwenaelle.hamon@usherbrooke.ca;
abderraouf.boucherif@usherbrooke.ca; maxime.darnon@usherbrooke.ca

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/solr.202300643>.

© 2023 The Authors. Solar RRL published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: [10.1002/solr.202300643](https://doi.org/10.1002/solr.202300643)

V. Daniel, T. Bidaud, J. Chretien, N. Paupy, A. Ayari, T. M. Diallo, T. Hanuš, J. Henriques, A. Jaouad, J.-F. Lerat, B. Ilahi, G. Hamon, A. Boucherif, M. Darnon

Laboratoire Nanotechnologies Nanosystèmes (LN2) - CNRS IRL-3463
Institut Interdisciplinaire d’Innovation Technologique (3IT)
Université de Sherbrooke
3000 boulevard de l’Université, Sherbrooke, Québec J1K 0A5, Canada

J. Cho, K. Dessein
Umicore Electro-Optic Materials
Watertorenstraat 33, 2250 Olen, Belgium

C. Dubuc
Saint-Augustin Canada Electric Inc.
75 rue d’Anvers, Saint-Augustin, Québec G3A 1S5, Canada

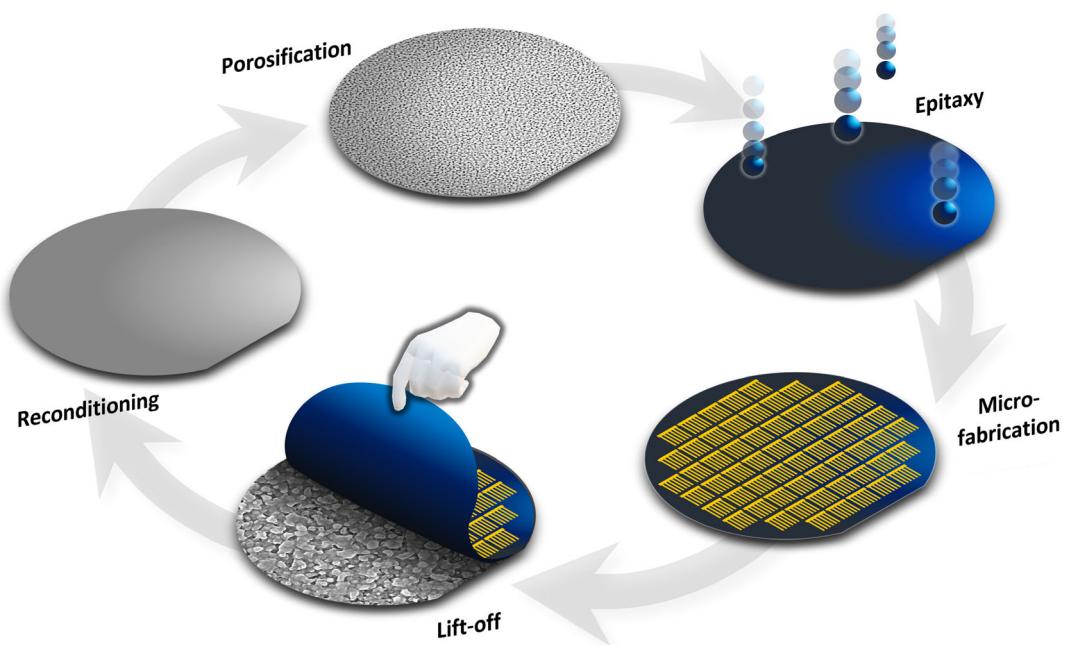


Figure 1. Illustration of the main steps of the PEELER substrate reuse technique.

on the top of a 100 mm Ge wafer (substrate). The characteristics (porosity, thickness, morphology) of this porous layer have been chosen such that the structural integrity of the stack is maintained during epitaxy in a high-temperature MOCVD reactor and during microfabrication processes for solar cells, e.g., photolithography, metallization, plasma etching, and so on.^[16]

A monocrystalline Ge epitaxial layer ($\text{Ge}_{\text{buffer}}$) has then been grown on the porous Ge surface. The growth has been performed following a two-step method yielding high-crystalline quality Ge membrane on a weak layer (further details on the growth process and Ge epilayer properties of this so-called PEELER process can be found elsewhere^[13]). A single-junction GaAs structure (including a 2 μm thick GaAs buffer layer) has been grown by MOCVD on this $\text{Ge}_{\text{buffer}}/\text{Ge}_{\text{porous}}/\text{Ge}$ wafer. In **Figure 2**, we can observe (a) a mirror-like surface on the monocrystalline GaAs/ $\text{Ge}_{\text{buffer}}/\text{Ge}_{\text{porous}}/\text{Ge}$ structure with no visible deterioration or self-delamination. Figure 2b shows a cross-sectional view of the III-V stack on the Ge template and (c) a zoom on the weak layer created after the coalescence of the pores, inducing the possibility of detaching the GaAs/ $\text{Ge}_{\text{buffer}}$ membrane.^[14,15] The diffractogram presented in Figure 2d shows Ge and GaAs epilayers are both monocrystalline and comparable on bulk and porous structures.

2.2. Microfabrication and Characterization

After the porosification of the germanium substrate and the epitaxial growth of the GaAs solar structure, we cleaved the wafer and extracted $1.5 \times 1.5 \text{ cm}^2$ samples originally located at the edge and the center of the wafer. Front-contacted solar cells (represented in **Figure 3a**) were fabricated via three levels using our own designed photolithographic mask. The main steps include the creation of a mesa structure down to the GaAs buffer^[17] using

low-damage plasma etching (a similar design reported in ref. [18]) and electrode metal depositions. The lift-off evaporation process for the creation of these metallic contacts has been executed by the association of different procedures. For the front-top contact, a negative photoresist deposited by spin coating is baked and exposed to UV through the first level of the mask. After development, a stack of metallic layers Ni/Ge/Au/Ni/Au (45/30/90/30/100 nm) is then deposited in the vacuum chamber of an Edward Electron Gun Evaporator, and the remaining resist is finally lifted off by a chemical remover (base solution). For the mesa process, a thick positive photoresist layer deposited by spin coating is baked, and exposed to UV through the second level of the mask to protect the front top contact and define the area of the cells. After the development of the resist, a plasma etching step using SiCl_4 , Cl_2 , and H_2 is applied in a STS—Multiplex Inductively Coupled Plasma (ICP) SR III-V system down to the middle of the 2 μm thick GaAs buffer layer. The protective resist is then stripped by a specific chemical remover (acid solution). Finally, for the front-base-contact in the bottom of the mesa structures, the same procedures as the front-top-contact are used but with a thicker negative photoresist layer patterned through the third level of the photolithographic mask and the evaporation of a Pt/Ti/Pt/Au (40/40/40/100 nm) contact structure without passivation. The metallic stacks were chosen to form ohmic contacts with the n- and p-type GaAs without the need for an annealing step. On each sample, 80 cells of $1 \times 1 \text{ mm}^2$ and four cells of $3 \times 3 \text{ mm}^2$ active surface are fabricated. Antireflective coating (ARC) was not deposited. Figure 3b shows the top-view SEM image taken for $1 \times 1 \text{ mm}^2$ cells fabricated on our samples. The final devices are then characterized ($I-V$ curves) by a solar simulator under 1 sun AM1.5 G. The sun illumination condition has been calibrated with two-terminal GaInP/GaInAs/Ge commercial solar cells with an active cell area of 9.16 mm^2 .

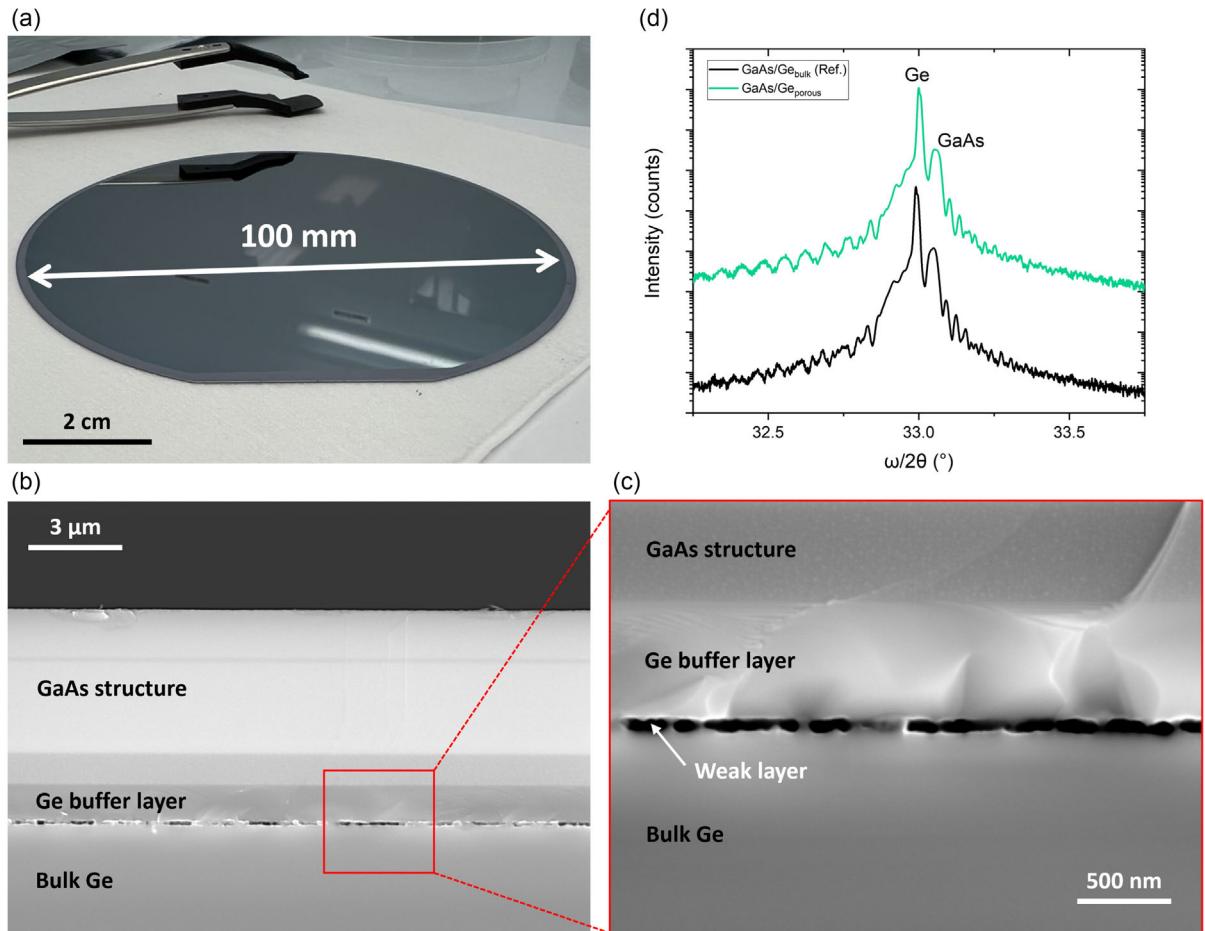


Figure 2. a) Macroscopic and b) scanning electron microscopy (SEM) images with zoom c) of the 100 mm GaAs solar structure on Ge_{porous} restructured (weak layer) after epitaxy at high temperature, and d) the XRD $\omega/2\theta$ diffractogram associated.

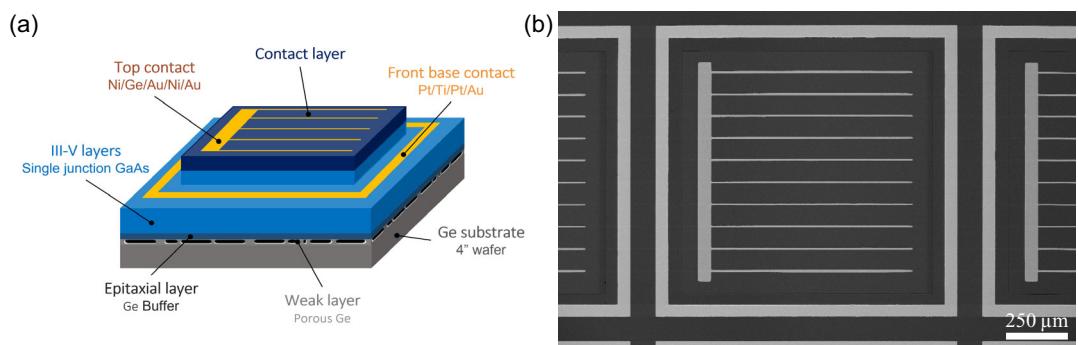


Figure 3. a) Illustration and b) SEM top-view of the microfabrication process applied on the PEELER wafers (GaAs/Ge/Ge_{porous}/Ge structures).

3. Results

A total of 250 solar cells are fabricated on different parts (center and edge) of the same wafer. 10% of them, randomly selected in various locations, have been characterized to validate the reproducibility of the process and the homogeneity of the solar cells' performances on the whole wafer. Three cells of the batch are shunted, meaning that our process has a yield of 88%. Note that

the cells are not detached yet and the detachment may degrade this yield. The *I*-*V* curves of 22 functional cells on the 25 measured are presented in **Figure 4a**. The average cell open-circuit voltage is $V_{oc,\text{mean}} = 1.012 \pm 0.014$ V, the average short circuit current is $J_{sc,\text{mean}} = 26.28 \pm 0.58$ mA.cm⁻², and the average fill factor is $FF_{\text{mean}} = 81.98 \pm 2.58\%$. These values are close to those expected for GaAs structures grown and fabricated on conventional Ge wafers.^[19] There is little dispersion in the solar cells

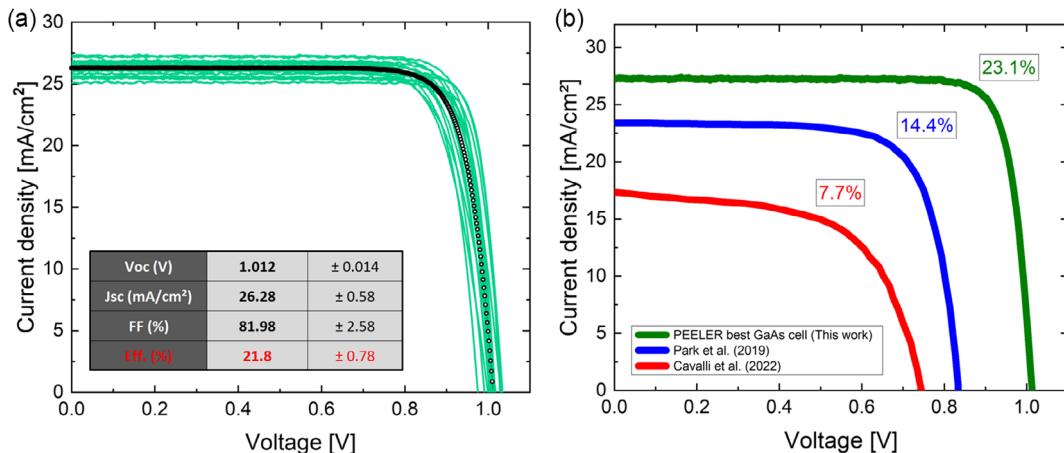


Figure 4. a) I - V measurement of single-junction GaAs cells designed (without ARC) with mean value and b) comparison of the best one (eff. = 23.1%) with III-V single-junction solar cell fabricated on Ge wafer nanostructured with analogous techniques in the literature.

characteristics attributed both to the nonuniformity of our sun simulator and slight nonuniformity of the epitaxial structure. In Figure 4b, we compare the I - V characteristics of the most efficient nondetached GaAs cell on a PEELER substrate (presented in this study) with state-of-the-art GaAs and GaInAs single-junction solar cells fabricated on weak layers created using analogous nanostructuring methods: the electrochemical etching^[20] and the RIE.^[8] Our best device demonstrates efficiency of 23.1%, surpassing the reported efficiencies of the best Ga(In)As cells fabricated on a detached Ge membrane through the “germanium-on-nothing” RIE-based process (eff. ref. 1 = 14.4%^[8]) or on a nondetached (bilayer) electroporosified Ge substrate (eff. ref. 2 = 7.7%^[20]). Regardless of the differences in the cells’ structures and fabrication details that may alter the overall devices’ performances, the III-V single-junction solar cells using the PEELER process show the highest reported efficiency to date.

4. Conclusion

We have developed a low-cost technique for the fabrication of wafer-scale detachable optoelectronic devices on a germanium substrate (PEELER process) by using a bipolar electrochemical etching process. With this work, we demonstrate the potential of engineered substrates and their application on a 100 mm wafer for industrial compatibility (large-volume production). To validate the reproducibility of the process, the homogeneity of the material quality and the possibility of using the porosification technique for III-V photovoltaic device fabrication were investigated. $1 \times 1 \text{ mm}^2$ GaAs single-junction cells of 22 fabricated on porousified germanium substrates showed high performance and small deviation ($V_{oc,\text{mean}} = 1.012 \pm 0.014 \text{ V}$, $J_{sc,\text{mean}} = 26.28 \pm 0.58 \text{ mA.cm}^{-2}$, and $FF_{\text{mean}} = 81.98 \pm 2.58\%$). These values are consistent with those expected for GaAs solar cells on conventional Ge substrate nonporosified. The best cell of this batch has an efficiency of 23.1%, higher than the reported values of the current literature on detachable germanium films. This demonstrates experimentally that the PEELER process can yield materials with device quality. These results also

demonstrate the compatibility of the porous structure with MOCVD growth and thus confirming the industrial potential of this method, opening the path toward detachable multijunction solar cells and other applications. Further development for the detachment of thin solar cells will be continued to enable multiple reuses of the Ge substrates.^[13,14,21]

Acknowledgements

The authors thank Pascal Bérubé and the 3IT’s clean room staff for technical support, and the Natural Sciences and Engineering Research Council of Canada (NSERC), Innovation en énergie électrique (InnovÉE), Mitacs, and Umicore and Saint-Augustin Canada Electric (Stace) for financial support. LN2 is a joint International Research Laboratory (IRL 3463) funded and co-operated in Canada by Université de Sherbrooke and in France by CNRS as well as ECL, INSA Lyon, and Université Grenoble Alpes (UGA). It was also supported by the Fonds de Recherche du Québec Nature et Technologie (FRQNT). A.B. is grateful for a Discovery grant supporting this work.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrochemical etching, GaAs single-junctions, III-V, nanostructures, porous germanium, solar cells

Received: August 14, 2023

Revised: November 6, 2023

Published online:

- [1] K. A. Horowitz, T. W. Remo, B. Smith, A. J. Ptak, A Techno-Economic Analysis and Cost Reduction Roadmap for III-V Solar Cells, No. NREL/TP-6A20-72103, 1484349, **2018**.
- [2] S. W. Bedell, D. Shahrjerdi, B. Hekmatshoar, K. Fogel, P. A. Lauro, J. A. Ott, N. Sosa, D. Sadana, *IEEE J. Photovoltaics* **2012**, 2, 141.
- [3] J. Chen, C. E. Packard, *Sol. Energy Mater. Sol. Cells* **2021**, 225, 111018.
- [4] A. Van Geelen, P. R. Hageman, G. J. Bauhuis, P. C. Van Rijsingen, P. Schmidt, L. J. Giling, *Mater. Sci. Eng., B* **1997**, 45, 162.
- [5] J. Yoon, S. Jo, I. S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J. J. Coleman, U. Paik, J. A. Rogers, *Nature* **2010**, 465, 329.
- [6] C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, D. K. Sadana, *Nat. Commun.* **2013**, 4, 1577.
- [7] P. Ramu, A. Aho, V. Polojärvi, T. Aho, A. Tukiainen, T. Hakkarainen, J. Reuna, J. Lyttikäinen, R. Hytönen, M. Guina, *Sol. Energy Mater. Sol. Cells* **2022**, 248, 111982.
- [8] S. Park, J. Simon, K. L. Schulte, A. J. Ptak, J.-S. Wi, D. L. Young, J. Oh, *Joule* **2019**, 3, 1782.
- [9] Y. Kim, S. S. Cruz, K. Lee, B. O. Alawode, C. Choi, Y. Song, J. M. Johnson, C. Heidelberger, W. Kong, S. Choi, K. Qiao, I. Almansouri, E. A. Fitzgerald, J. Kong, A. M. Kolpak, J. Hwang, J. Kim, *Nature* **2017**, 544, 340.
- [10] I. Mizushima, T. Sato, S. Taniguchi, Y. Tsunashima, *Appl. Phys. Lett.* **2000**, 77, 3290.
- [11] J. Govaerts, C. Trompoukis, H. S. Radhakrishnan, L. Tous, S. N. Granata, E. G. Carnemolla, R. Martini, A. Marchegiani, M. Karim, I. Sharlandziev, T. Bearda, V. Depauw, K. Van Nieuwenhuysen, I. Gordon, J. Szlufczik, J. Poortmans, *Energy Procedia* **2015**, 77, 871.
- [12] A. Boucherif, G. Beaudin, V. Aimez, R. Arès, *Appl. Phys. Lett.* **2013**, 102, 011915.
- [13] N. Paupy, Z. Oulad Elhmaidi, A. Chapotot, T. Hanuš, J. Arias-Zapata, B. Ilahi, A. Heintz, A. B. Poungoué Mbeunmi, R. Arvinte, M. R. Azizyan, V. Daniel, G. Hamon, J. Chrétien, F. Zouaghi, A. Ayari, L. Mouchel, J. Henriques, L. Demoulin, T. M. Diallo, P.-O. Provost, H. Pelletier, M. Volatier, R. Kurstjens, J. Cho, G. Courtois, K. Dessein, S. C. Dubuc, A. Jaouad, N. Quaegebeur, et al. *Nanoscale Adv.* **2023**, 5, 4696.
- [14] V. Daniel, J. Chretien, G. Hamon, M. De Lafontaine, N. Paupy, Z. O. El Hmaidi, B. Ilahi, T. Hanus, M. Darnon, A. Boucherif, in *2022 IEEE 49th Photovoltaics Specialists Conf. (PVSC)*, IEEE, Philadelphia, PA **2022**, pp. 0770–0772.
- [15] T. Hanuš, B. Ilahi, A. Chapotot, H. Pelletier, J. Cho, K. Dessein, A. Boucherif, *Mater. Today Adv.* **2023**, 18, 100373.
- [16] T. Hanuš, J. Arias-Zapata, B. Ilahi, P. Provost, J. Cho, K. Dessein, A. Boucherif, *Adv. Mater. Interfaces* **2023**, 10, 2202495.
- [17] M. De Lafontaine, F. Ayari, E. Pargon, G. Gay, C. Petit-Etienne, A. Turala, G. Hamon, A. Jaouad, M. Volatier, S. Fafard, V. Aimez, M. Darnon, *Sol. Energy Mater. Sol. Cells* **2022**, 239, 111643.
- [18] P. Albert, A. Jaouad, G. Hamon, M. Volatier, Y. Deshayes, L. Béchou, V. Aimez, M. Darnon, *Prog. Photovoltaics* **2021**, 29, 603.
- [19] B. M. Kayes, H. Nie, R. Twist, S. G. Spruytte, F. Reinhardt, I. C. Kizilyalli, G. S. Higashi, in *2011 37th IEEE Photovoltaic Specialists Conf.*, IEEE, Seattle, WA **2011**, pp. 000004–000008.
- [20] A. Cavalli, N. Alkurd, S. Johnston, D. R. Diercks, D. M. Roberts, B. E. Ley, J. Simon, D. L. Young, C. E. Packard, A. J. Ptak, *IEEE J. Photovoltaics* **2022**, 12, 337.
- [21] A. Chapotot, J. Arias-Zapata, T. Hanus, B. Ilahi, N. Paupy, V. Daniel, Z. O. E. Hmaidi, J. Chretien, G. Hamon, M. Darnon, A. Boucherif, in *2022 IEEE 49th Photovoltaics Specialists Conf. (PVSC)*, IEEE, Philadelphia, PA **2022**, pp. 0530–0530.