



HAL
open science

Evidence of trapping and electrothermal effects in vertical junctionless nanowire transistors

Y. Wang, Mukherjee Chhandak, H. Rezgui, M. Deng, Jonas Müller, S. Pelloquin, Guilhem Larrieu, C. Maneux

► **To cite this version:**

Y. Wang, Mukherjee Chhandak, H. Rezgui, M. Deng, Jonas Müller, et al.. Evidence of trapping and electrothermal effects in vertical junctionless nanowire transistors. *Solid-State Electronics*, 2024, 211, pp.108805. 10.1016/j.sse.2023.108805 . hal-04297709

HAL Id: hal-04297709

<https://hal.science/hal-04297709>

Submitted on 21 Nov 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Evidence of Trapping and Electrothermal Effects in Vertical Junctionless Nanowire Transistors

Y. Wang¹, C. Mukherjee¹, H. Rezgui¹, M. Deng¹, J. Müller², S. Pelloquin², G. Larrieu², and C. Maneux¹

¹IMS Laboratory, University of Bordeaux, UMR CNRS 5218, Cours de la libération, 33405 Talence, France

²LAAS CNRS, University of Toulouse, UPR CNRS 8001, Av. du Colonel Roche, 31400 Toulouse, France

Abstract

Understanding trap dynamics and formation of localized temperature hot-spots due to self-heating is crucial for the design optimization of emerging vertical junctionless nanowire transistors (VNWFET). This work investigates the operation of an 18nm VNWFET technology, for the first time, leveraging pulsed current-voltage measurements. Results indicate increased trap activity as well as electrothermal effects with increasing pulse width. Multiphysics simulations are then used to provide a deeper insight into the nanoscale transport of the VNWFETs. We then incorporated these effects into the SPICE-compatible VNWFET compact model and further investigated the behaviors of trapping and electrothermal effects in basic logic circuits based on the compact model simulation.

1. Introduction

The potential applications of "deep learning" have gathered significant interest in various areas of computing systems, such as natural language processing, image classification, and speech recognition leading to an increasing demand for data processing capacity along with the need for breakthrough technologies to support innovations in low power and latency in-memory computing hardware [1]. In addition, to face the process challenges of continuous scaling of the classical planar MOSFETs, emerging 3D technologies, such as vertical junctionless nanowire transistors (VNWFET), are recently being explored as beyond-CMOS alternatives [2]. Along with their gate-all-around architectures to enhance gate voltage control and immunity against short channel effects [3], one of the key advantages of VNWFETs is their inherent 3D structures which offer area benefits when stacked to increase the number of integrated transistors per unit area for designing more compact, faster and power-efficient hardware targeting neuromorphic computing. However, integrating GAA VNWFETs as a future mainstream solution would require reinventing the value chain for design technology co-optimization [4]. Considering different conduction mechanisms at the nanoscale in aggressively scaled transistors, the impact of electrothermal phenomena is one of the critical issues that needs to be carefully considered for design optimization. With that in mind, this paper investigates electrothermal and trapping effects in VNWFETs leveraging pulse measurements followed by subsequent compact model development incorporating these effects to evaluate electrothermal performances at device and circuit levels.

The devices studied in this work consist of multiple parallel vertical silicon nanowires arranged on silicon substrate (Fig. 1). The silicon nanowires are highly doped to form a junctionless device structure. Concentration gradients and metallurgical junction formation need not be considered, which simplifies the fabrication process. In addition, junctionless transistors have better electrostatic integrity and immunity to short-channel effects (SCE). Due to reduced carrier mobility in highly doped junctionless devices, electrothermal optimizations represent a key design aspect for the VNWFET technology. Another important factor that influences its electrical behavior is the trapping effect which is mainly related to the interface between the gate oxide and the Si nanowire [5]. Trap charges can be classified into two types: donor (positive) and acceptor (negative), which have different effects on the transistor I-V characteristics depending on their energy levels [6]. Moreover, at sub-20nm gate lengths, thermal confinement can significantly impact carrier transport. Therefore, it is an important prerequisite to understand and dissociate electrothermal and charge trapping effects in VNWFETs.

To investigate these effects, in this work, we perform pulsed I-V measurements on different geometries of p-type VNWFET devices with different pulse widths. Pulsed I-V measurements are particularly useful to dissociate pure electrical characteristics from thermal and trapping effects and to extract associated parameters of the VNWFETs. To analyze the experimental observations, we compare the pulsed measurements with multi-physics simulations. Next, we formulate analytical expressions to account for these effects and implement them within the VNWFET compact model. Subsequently, the impact of these effects at circuit level is studied through simulations of inverter and XOR logic gates.

The rest of the paper is organized as follows: In section 2, we present the pulsed I-V measurement setup for all available geometries. In section 3, we analyze the results using finite elements method and compact modeling. In section 4, we explore the performances of logic cells through circuit simulation based on the modified VNWFET compact model. Finally, section 5 is devoted to the conclusion.

2. Pulsed I-V measurements

The principle of pulsed I-V measurements relies on applying very short gate pulses on the device terminals so as not to allow sufficient time for its internal temperature to change significantly or activate any charge trapping. Fig. 2 shows the experimental setup used for characterizing the VNWFET technology with a gate length of 18nm from Laboratory for Analysis and Architecture of Systems (LAAS) [3]. Ultra-fast pulse measure unit (SMU8) in Fig. 2 applied a short square-wave pulse voltage with varying amplitude in the -1V to -2.2V range and a pulse width varying between 1 μ s and 10ms with a duty cycle of 10% at the gate, and a staircase pulse stepping voltage at the drain to minimize the charging effect [7]. To avoid distortion of I_D - V_D measurements due to oscillating regions of V_G and V_D after the rise time, the drain current was measured within the 90% to 95% time range of the pulse width. The I_D - V_D measurement data for all available geometries (nanowire diameters of 22 or 34 nm with 16 or 25 NWs in parallel over the entire bias range showed a constant increase in the drain current with pulse width and gradually approaching the characteristics obtained under DC operating conditions. On the contrary, for conventional transistors, the reduction in mobility with increasing pulse width leads to a decrease in drain current. In contrast, a much weaker mobility variation can be observed in junctionless devices [8] and the threshold voltage is the principal device parameter which is dominantly affected by electrothermal effects [9]. As an example, Fig. 3 shows the I_D - V_D curves under pulsed and DC operating conditions at -1V and -2.2V gate voltage bias for different pulses. The self-heating and trapping effects are expected to be activated at high gate voltages, which might explain why the difference in the drain current for different pulse widths becomes more pronounced. It has been hypothesized that this phenomenon is a combined effect of both (1) trapping and (2) electrothermal and self-heating effects. For further analyses, the VNWFET with 25 NWs with a diameter of 22 nm is selected as a representative device with the highest reproducibility and measurement stability.

3. Results and discussion

To understand the experimental observations under different pulse widths, we performed numerical simulations of the VNWFET structure using finite element method (FEM) [10] based on COMSOL Multiphysics simulation considering the same pulsed conditions as the measurements. The simulations are carried out using the partial differential equation (PDE) package in COMSOL governing the carrier transport equations by coupling thermal and electrical characteristics and solving the non-Fourier heat equation and the drift-diffusion model with interface trapping effects [11]. This finite element method (COMSOL) pulsed simulations results show a good agreement with the measurements results (Fig. 4(a)).

We used a novel hydrodynamic equation of the Guyer and Krumhansl (GKE) to predict non-Fourier heat dissipation. The governing equation of the GKE is written as [11],

$$q_x(r) = -\kappa \frac{dT}{dx} + l^2 \frac{d^2 q_x(r)}{dr^2} + l^2 \frac{1}{r} \frac{dq_x(r)}{dr} \quad (1)$$

where q is the heat flux, κ is the thermal conductivity, l is the phonon MFP, c is the heat capacity, T is the temperature. To consider the electro-thermal effect we use the energy-conservation equation:

$$c \frac{dT}{dt} + \nabla \cdot \mathbf{q}_x(\mathbf{r}) = P \quad (2)$$

where P is the dissipated power defined as $P = V_d I_d$. The extracted thermal conductivity, κ_{eff} , can be obtained as [12]

$$\kappa_{\text{eff}} = \frac{\int \mathbf{q}_x(\mathbf{r}) d\Gamma}{\frac{S\Delta T}{L}} \quad (3)$$

where S is the surface area, L is the distance between the source and drain and ΔT is the internal temperature increase. As revealed from the numerical simulations, a steady increase in the trap density was observed with increasing pulse widths which resulted in an equivalent shift of the device threshold voltage. The thermal conductivity and the rise of internal temperature extracted from COMSOL simulations are shown in Fig. 4(b). Subsequently, the VNWFET compact model [9] was also modified to integrate the threshold voltage (V_{TH}) shift due to trapping.

3.1. Electrothermal effects

To investigate the electrothermal behavior under pulsed conditions, COMSOL simulations are used to extract the thermal conductivity and the rise of internal temperature between the source and drain of a single nanowire for different pulse widths as shown in Fig. 4(b). A trap-assisted model is considered to capture the effect of charge trapping in the VNWFET device. It can be observed that the device temperature also increases due to phonon accumulation near the drain region at high bias conditions and larger pulse widths indicating the onset of self-heating phenomena. Consequently, the temperature hot-spots are formed due to the reduction of thermal conductivity caused by phonon confinement in the 22nm nanowire. Nevertheless, at room temperature, the internal temperature reduction after the peak value indicates good heat evacuation in VNWFET. A similar study with varying pulsed width was conducted on a vertical III-V nanowire technology [13], which shows a different behavior under varying pulse conditions compared to our case. In particular, this work demonstrates an increase in the drain current for smaller pulse widths due to the suppression of self-heating whereas no V_{th} shift was observed with pulse width, contrary to the pronounced V_{TH} -shift observed in our results. [14] presents a study on the extraction of interface trap density through transient measurements in junctionless transistors which reveals similar behavior of the transient drain current under gate pulse corresponding to different trap densities. In this study, a correlation between the increase of drain current and trap density is indicated and the extracted trap density is in agreement with theoretical data as well as of the same order of magnitude as in our case. Apart from these prior studies, correlating trap activation, and therefore V_{TH} -shift, with drain current variation using pulsed I-V method in junctionless devices is quite scarce in the literature. Our study is therefore one such first detailed investigation into the trap dynamics where we hypothesized that the trapped charges under varying pulse width are primarily responsible for the threshold voltage shift and thus an increase in the drain current. In addition to self-heating, phonon confinement can also lead to carrier trapping at the silicon-oxide interface [2]. Moreover, under higher bias conditions, scattering mechanisms increase which have a significant impact on trapping mechanisms. The self-heating effect is implanted into the compact model of VNWFET and activated by a FLAG parameter during the simulations.

3.2. Trapping effects

Trapped charge at the SiO_2 -Si interface, represented by the trap density N_T , alters the surface states of the nanowire leading to a modification of its surface potential and energy levels, which in turn, directly affects the V_{TH} . However, trapped charge is not the only factor that affects V_{TH} . In short channel devices, consistent with the characteristics of our VNWFET devices, the drain-induced barrier lowering (DIBL) causes an additional V_{TH} drift. Due to the weak mobility variation and sensitivity of the threshold voltage to a combination of electrothermal and trapping effects, the increase in the drain current in the junctionless transistor is reflected by an equivalent temperature change inside the device. From the pulse measurement data for all devices under test, at low V_D bias we use the transconductance gm/id- V_G method to extract the V_{TH} [15] and compare the V_{TH} (Fig. 5(a)) for different pulse widths to ensure that trapping induced V_{TH} shift follows the same trend in all available geometries.

From the evolution of the V_{TH} extracted under pulsed conditions, a clear trend can be observed for all device's geometries: as the pulse width continues to increase the V_{TH} values eventually saturate towards the

values obtained under DC operating conditions. To describe the relationship between the trap density (N_T) and the observed V_{TH} drift (ΔV_{TH}), we refer to the following expression

$$\Delta V_{TH} = \frac{\alpha q N_T}{C_{OX}}, \quad (4)$$

where α is a constant, q is the electronic charge and C_{OX} is the gate oxide capacitance. Fig. 5(b) plots the trap density N_T extracted from COMSOL and the extracted values of ΔV_{TH} for different measurements pulse widths. We observed that N_T can be described by an analytical expression with the following equation:

$$N_T = N_{SS} \left(1 - \exp\left(\frac{-t_w}{\tau}\right) \right), \quad (5)$$

here N_{SS} is the maximum number of available traps, t_w is the pulse width, τ is a time constant associated with the trap activation. Fig. 5(b) clearly shows the N_T and ΔV_{TH} present the same trend as a function of the pulse width. This affirms N_T dominates the V_{TH} shift and results the increase of drain current. Through transient analysis, we confirm the time-domain nature of the trap activation, which disappears at DC operating conditions when the trapping is considered all activated and $N_T=N_{SS}$. The effect of charge trapping has been implemented within the VNWFET compact Verilog-A model, through an additional contribution to the threshold voltage expression, ΔV_{TH} , which is dynamically calculated as the voltage of an additional fictitious node, similar to the implementation of the self-heating effects in conventional compact models. Depending on the type of analysis, a FLAG parameter is used to activate or deactivate the dynamic effect in order to distinguish the trapping behavior under transient and static conditions. The transient analysis for studying trapping effect in the time domain makes use of the equivalent RC filter-like circuit [16] (Fig. 6) and recalculates the ΔV_{TH} from the node voltage through the following relation implemented in the model:

$$\Delta V_{TH_max} = \Delta V_{TH} + \tau \frac{d\Delta V_{TH}}{dt}, \quad (6)$$

where ΔV_{TH_MAX} indicates the maximum threshold voltage shift due to trapping, and τ is the trapping time constant which is the same value as in equation (5). Using time derivatives (ddt) in Verilog-A is an efficient way to implement capacitive effect through a branch current. In the equivalent circuit of Fig. 6, a current source ΔV_{TH_MAX} and two parallel R-C branches with a 1Ω resistance and a capacitance of value τ are implemented and through Kirchhoff's current rule, the node voltage effectively gives the value of ΔV_{TH} under dynamic conditions. By adding Eqs. (4), (5) and (6) to the V_{TH} expression that exists for the compact model to more accurately characterize the drain current with drift pulse width variation. Both finite element method (COMSOL) and compact model accurately account for the ΔV_{TH} drift and thereby show good agreement with I-V measurements results shown in Fig. 4(a). These models have been used to extract the trap density that we estimated $N_T=4 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ under DC operating conditions.

4. Impact of electrothermal and trapping effects at circuit level

Following the validation of the VNWFET compact model with electrothermal and trapping effects at transistor level, in this section we explored the impact of these effects on the performances of different logic circuit topologies. We first studied a simple inverter circuit consisting of a p-type VNWFET for the pull-up network and an n-type VNWFET for the pull-down network, with a 1V supply voltage (V_{DD}) applied to the source of the p-MOS and a load capacitance C_{load} connected to the output for the simulation, as illustrated in the schematic of Fig. 7(a). The two transistors feature the same geometrical characteristics with NW diameters of 22 nm and 25 nanowires in parallel. Fig. 7(b) shows both the input (V_{IN}), applied to the gates of the two transistors, and the output (V_{OUT}) waveforms. The inverter circuit was then simulated considering the electrothermal and trapping effects corresponding to the DC and pulse conditions with a $1\mu\text{s}$ gate pulse. From the zoomed view of the output transient waveform in Fig. 7(b), both a logic-level degradation and an increased delay can be observed for the DC condition in contrast with when using a $1\mu\text{s}$ pulse width. Fig. 7(c) shows the typical inverter transfer curves for these two cases. The results indicate a symmetric inverter functionality, even though a steeper transition is observed for the pulsed case implying a circuit performance degradation at the onset of electrothermal and trapping effects under DC conditions. More specifically, the off-state current (I_{OFF}) increases significantly due to the threshold voltage drift caused by these effects under DC conditions. The increase in I_{ON} is not sufficient to compensate for the impact of the reduction in the I_{ON}/I_{OFF} ratio thereby

affecting the switching characteristics of the inverter logic cell. In more complex circuits, such as a XOR logic circuit consisting of eight VNWFETs shown in the Fig. 8(a), the outputs Fig. 8(b) indicate a classical XOR operation, but the output logic level degradation under DC operating conditions becomes more pronounced, compared to the pulsed case, due to the combined influence of the trapping and electrothermal effects.

5. Conclusion

In this work, we present, for the first time, a comprehensive analysis of pulsed I-V characteristics of VNWFETs. Experimental results are analyzed with physical simulations indicating the activation of trapping and self-heating with increasing pulse widths. The increase of drain current with larger pulse width has been attributed to an increasing activated trap density which results in an equivalent shift of the threshold voltage. This directly affects the performance of logic circuits based on the VNWFET technology. The effects become more pronounced as the complexity of the circuit increases leading to degradation of their performance metrics. As suggested by the evidences presented in this work, dissociating the trapping and electrothermal phenomena in junctionless transistors remains a challenging task and will be the subject of our future analysis.

Acknowledgments

This work was supported by the project FVLLMONTI funded by European Union's Horizon 2020 research and innovation program under grant agreement N°101016776 and by the LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech French national network.

References

- [1] The International Roadmap for Devices and Systems: 2022 Update.
- [2] JP. Colinge, CW. Lee, A. Afzalian, ND. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, AM. Kelleher, B. McCarthy, R. Murphy. "Nanowire transistors without junctions". *Nat Nanotechnol.* 2010 Mar;5(3), 225-229. Epub 2010 Feb 21.
- [3] Y. Guerfi, G. Larrieu "Vertical silicon nanowire field effect transistors with nanoscale gate-all-around" *Nanoscale Res Lett* 11, 210 (2016).
- [4] C. Maneux, C. Mukherjee, M. Deng, M. Dubourg, L. Reveil, G. Bordea, A. Lecestre, G. Larrieu, J. Trommer, E.T. Breyer, S. Slesazek, T. Mikolajick, O. Baumgartner, M. Karner, D. Pirker, Z. Stanojevic, David Atienza, A. Levisse, G. Ansaloni, A. Poittevin, A. Bosio, D. Deleruyelle, C. Marchand, I. O'Connor. "Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence" (Invited). 67th Annual IEEE IEDM, Dec. 11-15, 202.
- [5] C. Mukherjee, C. Maneux, J. Pezard and G. Larrieu, "1/f Noise in 3D vertical gate-all-around junctionless silicon nanowire transistors," 2017 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 2017, pp. 34-37
- [6] R.S. Bonilla, I. Al-dhahir, M. Yu, P. Hamer, P.P. Altermatt, "Charge fluctuations at the Si – SiO₂ interface and its effect on surface recombination in solar cells", *Sol. Energy Mater. Sol. Cells.* 215 (2020) 110649.
- [7] B. Hai, Y.V. Tolmachev, K.A. Loparo, C. Zanelli, D. Scherson, "Cyclic versus Staircase Voltammetry in Electrocatalysis: Theoretical Aspects". *J. Electrochem. Soc.* 2011, 158, F15.
- [8] A. K. Goel and T. H. Tan, "High-temperature and self-heating effects in fully depleted SOI MOSFETs," *Microelectronics Journal (Elsevier)*, vol. 37, p. 963–975, 2006.
- [9] C. Mukherjee, A. Poittevin, I. O'Connor, G. Larrieu, C. Maneux, "Compact modeling of 3D vertical junctionless gate-all-around silicon nanowire transistors towards 3D logic design", *Solid-State Electronics*, vol. 183, pp. 108125, Sep. 2021.
- [10] C. Mukherjee, H. Rezgou, M. Deng, A. Kumar, J. Muller, G. Larrieu, C. Maneux, "Nanoscale Thermal Transport in Vertical Gate-all-around Junction-less Nanowire Transistors- Part I: Experimental Methods", *IEEE Trans. Electron Dev.* 2023.
- [11] H. Rezgou, F. Nasri, G. Nastasi, M.F.B. Aissa, S. Rahmouni, V. Romano, H. Belmabrouk, A.A. Guizani, "Design optimization of nanoscale electrothermal transport in 10 nm SOI FinFET technology node", *J. Phys. D: Appl. Phys.*, vol. 53, 2020.
- [12] Y. Guo and M. Wang, "Phonon hydrodynamics for nanoscale heat transport at ordinary temperatures", *Phys. Rev. B*, vol. 97, pp. 035421–27, Jan. 2018.

- [13] G. Rangasamy, M. S. Ram, L. O. Fhager and L. -E. Wernersson, "Self-Heating in Gate-All-Around Vertical III-V InAs/InGaAs MOSFETs," in IEEE Electron Device Letters, vol. 44, no. 7, pp. 1212-1215, July 2023.
- [14] E. Teixeira da Fonte, R. Trevisoli, S. Barraud, R. T. Doria, "Interface traps density extraction through transient measurements in junctionless transistors", Solid-State Electronics, Volume 194, 2022, 108302.
- [15] R. Trevisoli, R. T. Doria, M. de Souza and M. A. Pavanello, "A physically based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors" Solid-State Electron. Vol. 90 pp. 12–7, 2013.
- [16] G. J. Coram, "How to (and how not to) write a compact model in Verilog-A," Proceedings of the 2004 IEEE International Behavioral Modeling and Simulation Conference, pp. 97-106.

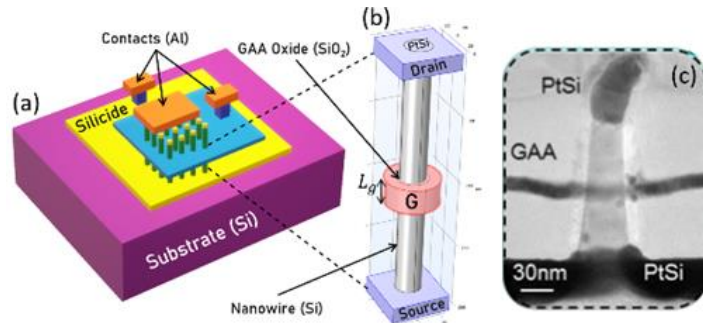


Fig. 1. Schematic representation of (a) Vertical array of GAA nanowires. (b) A single nanowire. (c) SEM image of a fabricated nanowire [3].

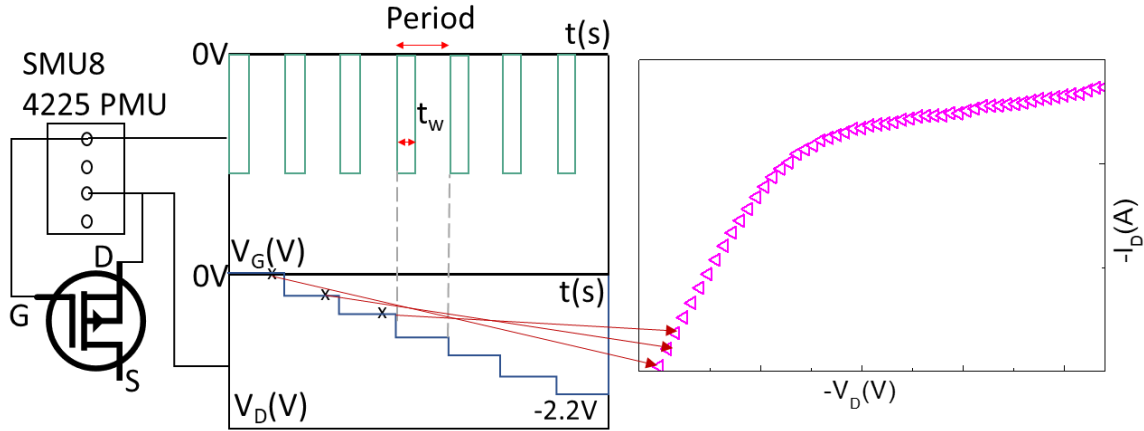


Fig. 2. Pulsed measurements setup to transient measurements of VNWFETs.

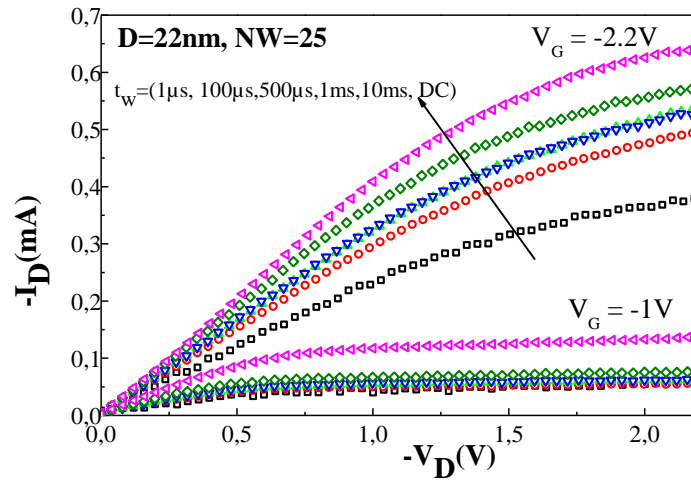


Fig. 3. I_D-V_D results under DC measurements and pulsed measurements with pulse widths varying from 1μs to 10ms at V_G=-1V and -2.2V.

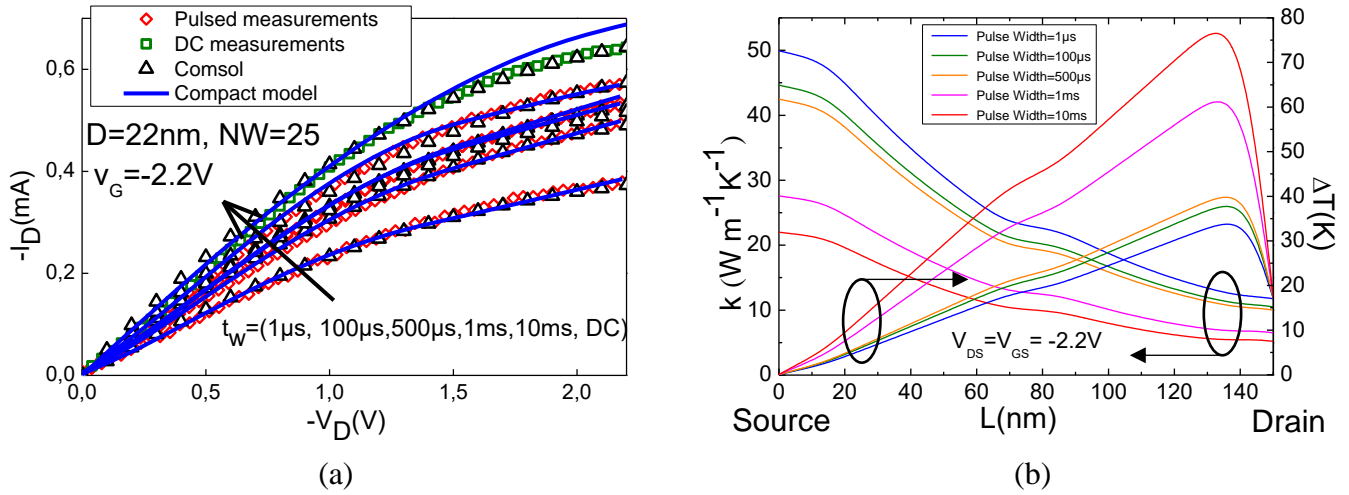


Fig. 4. (a) Pulsed I_D - V_D measurements and DC measurements are compared with compact model and COMSOL simulations. (b) Thermal conductivity and internal device temperature of the VNWFET.

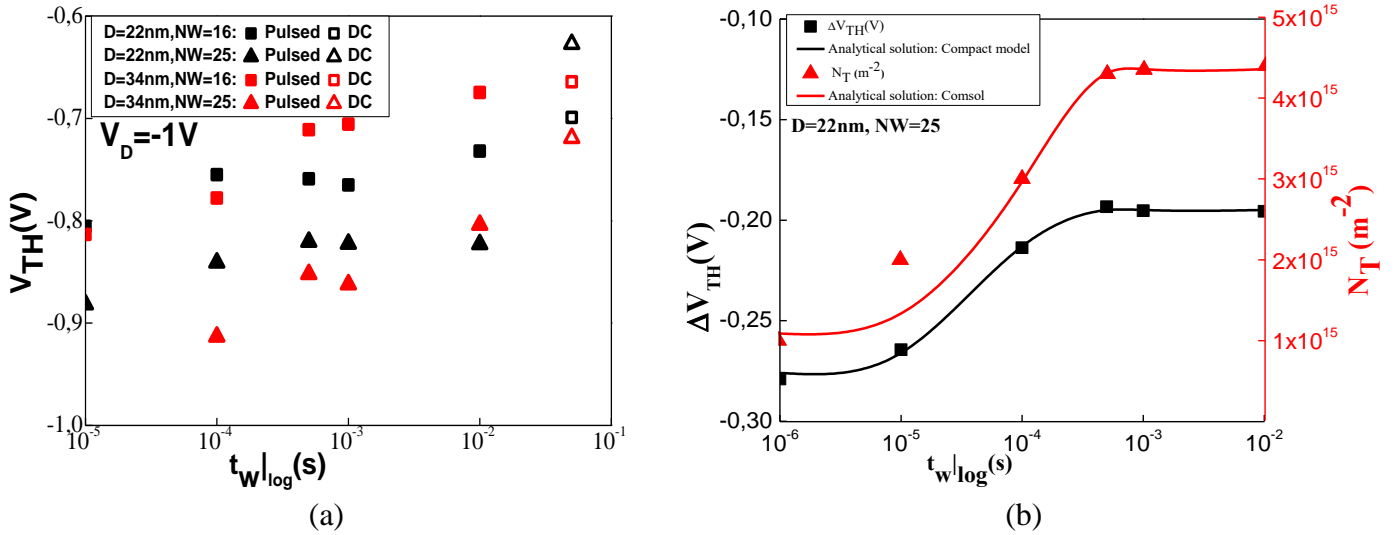


Fig. 5. (a) V_{TH} - t_w of different VNWFET geometries extracted from DC and pulsed measurements. (b) ΔV_{TH} - t_w , N_T - t_w of the device with NW diameter 22nm and 25 NWs in parallel compared with analytical solutions.

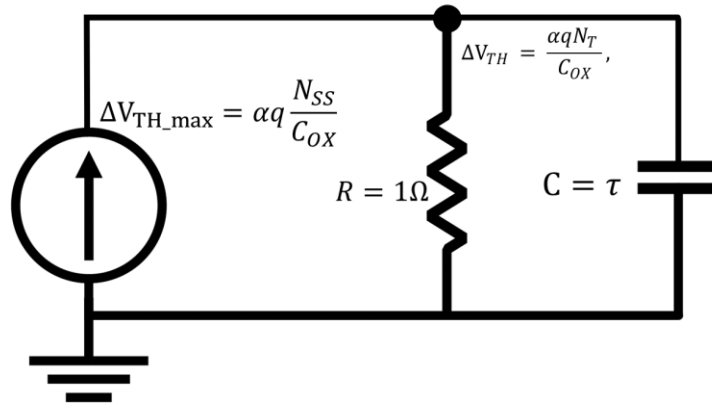


Fig. 6. Equivalent circuit for trap effect in compact model.

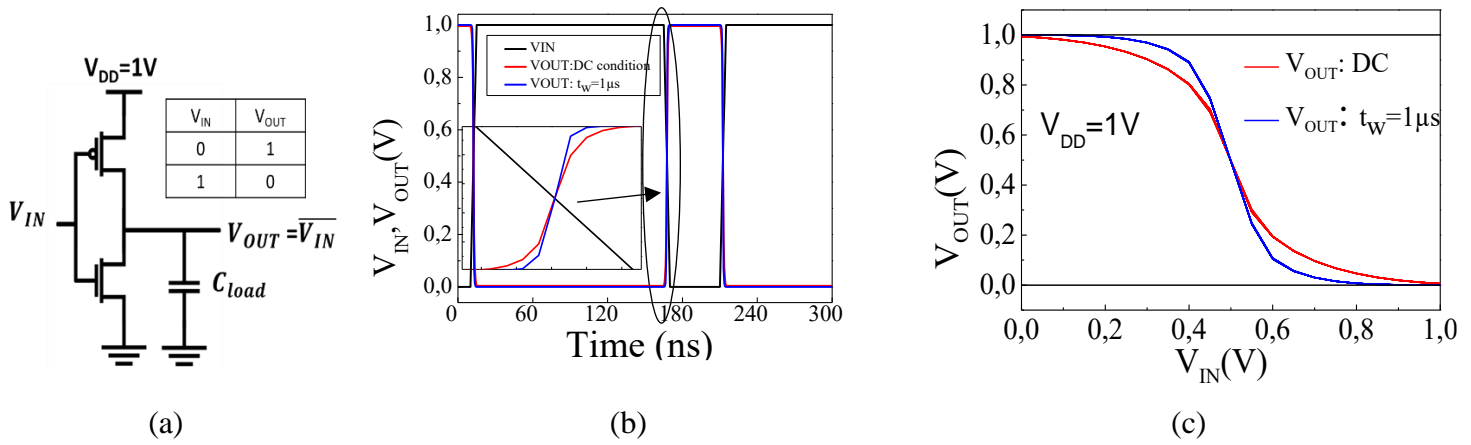


Fig. 7. (a) Inverter Logic circuit (b) inverter logic circuit input (V_{IN}) and output (V_{OUT}) waveform. (c) V_{IN} - V_{OUT} simulation results.

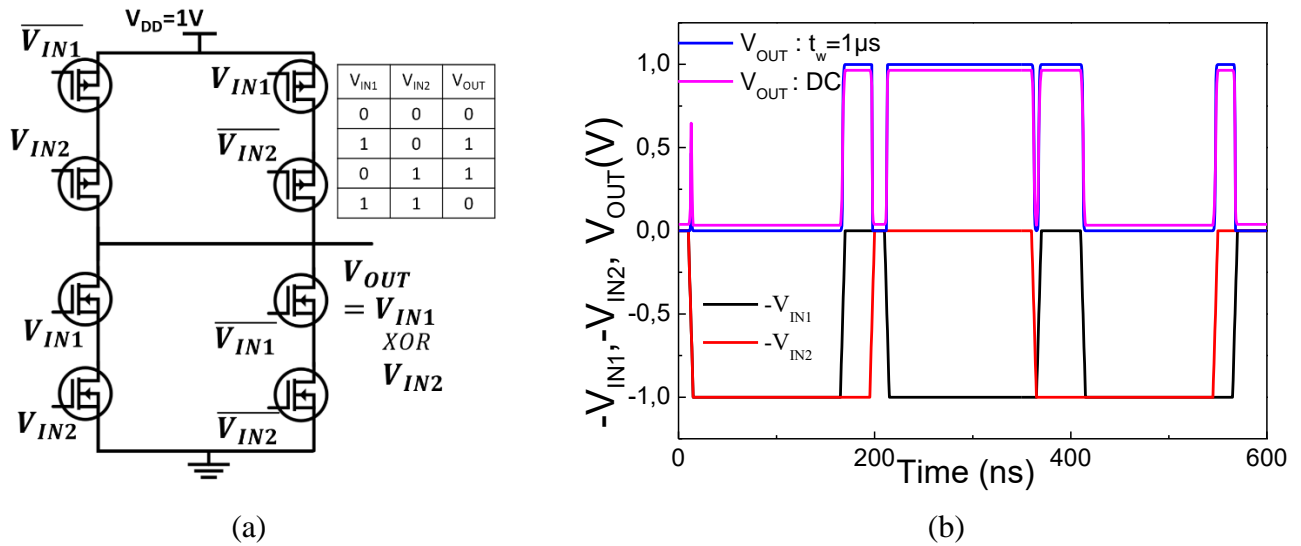


Fig. 8. (a) XOR Logic circuit (a) XOR logic circuit inputs (V_{IN1} , V_{IN2}) and output (V_{OUT}) waveform. (b) V_{IN1} , V_{IN2} and V_{OUT} simulation results.