



**HAL**  
open science

# Nanoscale Thermal Transport in Vertical Gateall-around Junction-less Nanowire Transistors-Part II: Multiphysics Simulation

H. Rezgui, Mukherjee Chhandak, Y. Wang, M. Deng, A. Kumar, J. Müller, G. Larrieu, C. Maneux

► **To cite this version:**

H. Rezgui, Mukherjee Chhandak, Y. Wang, M. Deng, A. Kumar, et al.. Nanoscale Thermal Transport in Vertical Gateall-around Junction-less Nanowire Transistors-Part II: Multiphysics Simulation. IEEE Transactions on Electron Devices, 2023, 70 (12), pp.6505 - 6511. 10.1109/TED.2023.3321280 . hal-04296531

**HAL Id: hal-04296531**

**<https://hal.science/hal-04296531>**

Submitted on 20 Nov 2023

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

---

# Nanoscale Thermal Transport in Vertical Gate-all-around Junction-less Nanowire Transistors- Part II: Multiphysics Simulation

H. Rezgui, *Member, IEEE*, C. Mukherjee, *Member, IEEE*, Y. Wang, *Member, IEEE*, M. Deng, *Member, IEEE*, A. Kumar, J. Müller, G. Larrieu, *Member, IEEE*, C. Maneux, *Member, IEEE*

**Abstract**—Today, extensive research has focused on heat propagation in emerging nanoelectronic devices. With advances in fabrication of nanowire transistors, thermal management has become a critical issue in cooling strategies and conducting materials. In this paper, we present a novel multiphysics analysis of the nanoscale thermal transport in 18 nm vertical junctionless gate-all-around silicon nanowire transistors. Based on this multiphysics analysis, we developed a new computational model derived from the Guyer-Krumhansl equation for describing heat transport within the nanoscale device. Our simulation results agree well with available theoretical approaches as well as measurement data.

**Index Terms**—Junctionless nanowire transistors, nanoscale thermal transport, Guyer-Krumhansl equation (GKE), thermal resistance, heat dissipation.

## I. Introduction

DUe to miniaturization of device dimensions, metal-oxide-semiconductor field-effect transistors (MOSFETs) continue to scale down to sub-20 nm technology nodes [1]. In modern transistors, the charge density within the channel region is mostly controlled by a gate electrode rather than the source/drain junctions. As most of the CMOS transistors are still manufactured based on the fabrication process for drain and source junction alignment, high doping concentration is regarded as a major technological challenge for the semiconductor industry [2]. Both planar FETs, such as fully depleted (FD), and nonplanar FETs (e.g., FinFETs), suffer from self-heating effects (SHEs) due to intrinsic resistive scattering and random dopant fluctuations [3]. In contrast, junctionless nanowire transistors (JLNTs) can be fabricated without requiring steep gradients in doping concentration, and are therefore suitable for reducing the impact of SHE [4]. Moreover, JLNTs devices can be scaled down to 14 nm technology node satisfying Moore's law [5–7]. Therefore, the emerging vertical gate-all-around (GAA) JLNTs technologies have the potential to offer long-term reliability and enhanced thermal stability.

This work was supported by the project FVLLMONTI funded by European Union's Horizon 2020 research and innovation program under grant agreement N°101016776 and by the LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech French national network.

The authors would like to thank Prof. Masahiro Nomura for critical reading of the manuscript.

At the nanoscale, thermal management has drawn significant interest owing to its increased physical presence in small dimensional systems [8-10]. Moreover, next generations transistors are expected to feature very small channel regions, making the analysis of the thermal phenomena a significantly important technological factor [8]. Therefore, to fully anticipate the physical behavior of these emerging devices, understanding of nanoscale heat transport has become imperative, especially for controlling thermal energy with the development of next-generation transistors [9]. In modern semiconductor manufacturing process, characteristic lengths have already reached 20 nm and below [10]. Therefore, thermal analyses at nanoscale could offer several strategies to optimize heat propagation and improve device lifetime. In classical regime, Fourier's law has long been used to describe the heat response of bulk materials at equilibrium state (diffusive regime) [11]. In small dimensional semiconductor systems (i.e., sub-20 nm), when the characteristic length becomes comparable to the average mean free path (MFP) of the phonons, which are the major heat carriers [12], the classical Fourier's law fails to predict the thermal transport [12–14]. As the size of the transistor reduces, boundary effects become more significant which influences the thermal conductivity. In most cases, phonon boundary scattering causes a large reduction of the thermal conductivity. Indeed, in nanoscale dimensions, the heat flux can propagate within a nanowire structure without heating the device in the event of ballistic transport [13]. In general, nanoscale heat transport can be described by the phonon Boltzmann transport equations (BTE). Due to the complexity of the nanotransistors geometries, several analytical solutions of BTE are available with respect to extended irreversible thermodynamics (EIT) [16].

In emerging nanoelectronics, the efficiency of heat spreading is directly related to the thermal conductivity and interfacial energy transport. Particularly, low thermal conductance can lead to small thermal conductivities due to the phonon confinement near the interface between two different materials [17]. For nanoscale transistors, high thermal conductivity materials are therefore desirable in order to reduce the SHEs and thermal degradation [18]. To study the phonon dynamics in

H. Rezgui, C. Mukherjee, Y. Wang, M. Deng and C. Maneux are with IMS laboratory, University of Bordeaux, France. (e-mail: [chhandak.mukherjee@ims-bordeaux.fr](mailto:chhandak.mukherjee@ims-bordeaux.fr)).

A. Kumar, J. Müller and G. Larrieu are with LAAS CNRS, UPR 8001, CNRS, Université de Toulouse, France. (e-mail: [guilhem.larrieu@laas.fr](mailto:guilhem.larrieu@laas.fr))

these devices, accurate models for the prediction of heat propagation are thus crucial compared to empirical models with fitting parameters. A first approach using a local equilibrium method based on the classical Fourier's law may lead to incorrect predictions about the heat propagation. Therefore, non-Fourier analyses based on mesoscopic methods are more suitable for investigating heat flow in small dimensional systems [12-13, 19]. For instance, the Guyer-Krumhansl equation (GKE) was derived from the BTE based on the Chapman-Enskog expansion for the description of wavelike heat flow at low temperatures when phonon normal (N) scattering dominate [20]. Recently, the application of GKE has been demonstrated for probing non-Fourier heat transport at room temperature [21]. In the context of vertical nanowire transistors and in general for extremely small systems, GKE can thus be used to capture the phonon transport where confinement effects appear to be significant.

Following the experimental methods for studying electro-thermal effects in JLNTs demonstrated in part –I of this work [22], in this paper, we focus on nanoscale thermal transport in 18 nm JLNTs with a wide range of nanowire diameters and number of nanowires in parallel. We refer to the finite-element method for solving thermal transport equations. The present work offers a deeper understanding of nanoscale heat transport in emerging nanoscale systems. The paper is organized as follows: In the section II, we present the computational model and boundary conditions. In addition, we validate our proposed GKE based model by comparing the effective thermal conductivity of Si NWs with experimental data and theoretical models. Section III describes the device geometry and test structures and discusses the validation of our proposed modeling framework by comparing the thermal resistance extracted using our model and measurement data from both of experimental JLNT and FinFET technologies. Finally, section IV is devoted to conclusions and perspectives.

## II. THEORETICAL BACKGROUND

### A. COMPUTATIONAL MODEL

In order to predict the hydrodynamic phonon transport at low temperature, Guyer and Krumhansl proposed a solution to the linearized BTE for nonequilibrium heat transfer [20]. Many of the past works have focused on phonon hydrodynamics when both normal (N) and resistive (R) scattering processes have strong contributions to the physical origin of the heat response [23]. In recent studies, the GKE was developed based on macroscopic hydrodynamic equation for nanoscale heat transport at room temperature [12, 24] where most nanoelectronic devices commonly operate. The governing equations are the GKE and the energy-conservation equation, respectively [12-13, 19] written as,

$$q + \tau_R \frac{\partial q}{\partial t} = -\kappa \nabla T + \ell^2 (2\nabla \nabla \cdot q + \Delta q) \quad (1)$$

$$c \frac{dT}{dt} + \nabla \cdot q = 0 \quad (2)$$

where  $q$  is the heat flux,  $\tau_R$  is the phonon relaxation time,  $\kappa$  is the bulk thermal conductivity,  $\ell$  is the phonon MFP,  $c$  is the heat capacity and  $T$  is the temperature. Equation (1) gives a simple analytical solution of the phonon BTE as well as a better understanding of non-Fourier heat-flow modeling. As device size decreases, non-local effects included in the Laplacian term

$\Delta q$ , become dominant. In general, the nonlocality of the heat flux gradient originates from the phonon-boundary scattering and confinement effects. According to the average phonon MFP,  $\ell$ , heat transport regimes are classified into three regimes: (1) ballistic regime (external boundary scattering); (2) quasi-ballistic regime and (3) bulk-like (diffusive) regime. In sub-30 nm silicon devices, ballistic transport governs heat flow, and it is expected that phonon-boundary scattering contributes to the reduction of the thermal conductivity [14]. For steady-state phonon transport, the GKE is expressed as

$$q = -\kappa \nabla T + \ell^2 \Delta q \quad (3)$$

The present GKE provides an enhanced formulation for investigating nanoscale heat transport beyond the classical

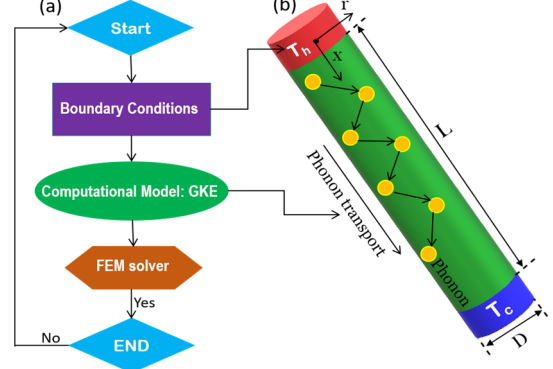


Fig. 1. (a) Numerical simulation scheme for nanoscale thermal transport. (b) Schematic of phonon transport within a nanowire.

Fourier's law.

### B. Boundary conditions

At room temperature, slip boundary conditions is mandatory for the description of phonon transport in small dimensional materials [12]. Particularly, two macroscopic mechanisms occur during non-equilibrium phonon distribution: (1) the tangential heat flux close to the boundary and (2) the non-continuous temperature variation (i.e. temperature jump) due to phonon-boundary collision [12]. Based on the Maxwell model, the slip boundary condition for the tangential heat flux at the boundary is given by [21]

$$q_t = -C_w \ell \nabla q_t \cdot n \quad (4)$$

$$q \cdot n = 0 \quad (5)$$

where,  $n$  is the interface normal vector and  $C_w$  is a constant which is expressed in terms of the specularity of the surface. In most cases, solving the GKE and slip boundary conditions requires an accurate value of the thermal conductivity, average mean free path and heat capacity that are obtained from microscopic approaches such as *ab initio* calculations. The computational model presented in this paper is described by the numerical scheme detailed in Fig. 1(a). Here, the GKE is solved based on the finite-element method (FEM) using *COMSOL MULTIPHYSICS* simulator [25]. For the steady state phonon transport, we consider that the nanowires are initially at a constant temperature,  $T_c$ , and then one end of the nanowire comes in contact with the heat-source  $T_h = T_c + \Delta T$ , where  $\Delta T$  is the temperature difference as shown in Fig. 1(b).

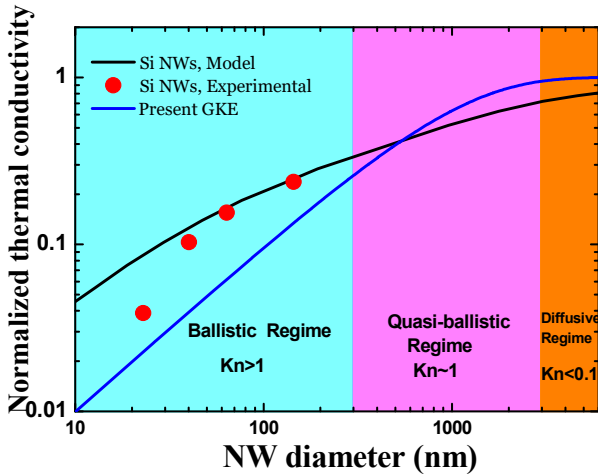


Fig. 2. Comparison of normalized thermal conductivity for silicon nanowire at room temperature.

### C. Effective thermal Conductivity: Model Validation

In nanodevices, where the characteristic lengths are comparable to the MFP, ballistic phonon transport leads to a critical dependence of size effects on the effective thermal conductivity [14]. For the heat flow through a nanowire with radius  $r$ , Eq. (3) can be rewritten as

$$q_x(r) = -\kappa \frac{dT}{dx} + \ell^2 \frac{d^2 q_x(r)}{dx^2} + \ell^2 \frac{1}{r} \frac{dq_x(r)}{dr} \quad (6)$$

The effective thermal conductivity (ETC),  $\kappa_{eff}$ , is defined as [21]

$$\kappa_{eff} = \frac{\int q_x(r) d\Gamma}{S \Delta T / L} \quad (7)$$

Here  $\Gamma$  is the cross section,  $S$  is the surface area and  $L$  is the distance between the two ends of the system. The classical Fourier's law of heat conduction can only predict thermal conductivity in bulk materials when the characteristic dimensions are larger than the phonon MFP. Here, we consider a Knudsen number defined as  $Kn = \frac{\ell}{D}$ , where  $D$  is the diameter of the nanowire, to classify the nanoscale thermal transport within the nanowire [12]. For  $Kn > 1$ , ballistic transport dominates and the thermal conductivity is significantly influenced by the confinement effects. For  $Kn \approx 1$ , the thermal conductivity increases due to enhanced boundary scattering (i.e. weak confinement effect). In diffusive regime ( $Kn \ll 1$ ), Eq. (6) reduces to the Fourier's law,  $q_x(r) = -\kappa \frac{dT}{dx}$ . Fig. 2 shows the diameter dependence of normalized thermal conductivity in Si NWs with a phonon MFP,  $\ell = 300 \text{ nm}$ , at  $T = 300 \text{ K}$ . According to Kwon et al., [14], we assume fully diffusive boundary scattering, i.e.,  $C_w = 1$ , to achieve an accurate comparison with the theoretical and experimental results [14] (Fig. 2). Our proposed model displays a good prediction of experimental data for Si NWs down to 30 nm. From Fig. 2, we can distinguish between three distinct thermal transport regimes: (1) a ballistic regime where the phonon boundary/interface scattering leads to a significant reduction of the thermal conductivity; (2) a quasi-ballistic regime where we expect a Lévy flight due to trapped phonons in the Si NW; (3) a diffusive regime where the effective thermal conductivity reaches the bulk value (the Knudsen number is small enough with  $Kn = 0.05$ ). The GKE gives a consistent result with the theoretical predictions and experimental data. For further validation, the GKE is compared to experimental results [26]

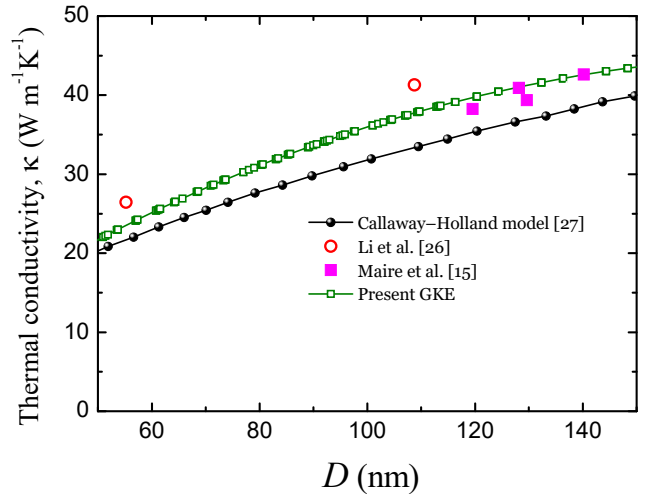


Fig. 3. Thermal conductivity as a function of NW diameter.

and the Callaway-Holland model derived from the first law of thermodynamics based on BTE for phonon distribution [27]. This is particularly useful for investigating the impact of the boundary scattering and size effects (i.e., diameter of the nanowire) on the thermal conductivity. GKE being an analytical solution of the BTE, we compared it with the Callaway-Holland model to justify the accuracy of our proposed framework in Fig. 3, which illustrates the thermal conductivity of Si NWs as a function of the NW diameter. It can be clearly observed that the present model agrees well with the theoretical Callaway-Holland model [27] and experimental data reported by Maire et al. [15]. The thermal conductivity decreases in small diameters due to phonon confinement. As system dimensions reach the quantum regime, the effect of phonon/interface scattering leads to reduced ETC. In the next section, this computational model is applied for analyzing JLNTs devices.

## III. RESULTS AND DISCUSSION

### A. Non-Fourier heat transport

The 3D schematic view of the state-of-the-art JLNT technology under test is illustrated in Fig. 4 (a). The key feature of the fabricated JLNT is its gate-all-around structure that ensures enhanced electrostatic control of the current between

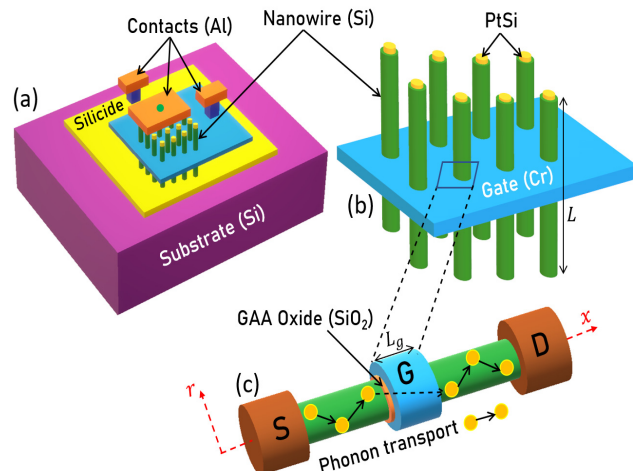


Fig. 4. Schematic representation of (a) vertical GAA JLNT. (b) Nanowires in parallel. (c) Phonon transport in single nanowire. The green dot on the top contact is the location used for thermal extraction.

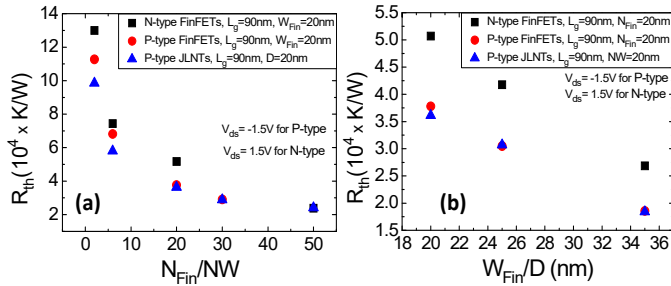


Fig. 5. The extracted thermal resistance in SOI FinFETs [31] and JLNTs as function of (a)  $N_{Fin}/NW$  and (b)  $W_{Fin}/D$ .

source and drain contacts. For the device under test, the gate is fabricated using chromium (Cr) that ensures better control of interfacial thermal transport within the nanowire and offers high thermal conductivity even at room temperature [21]. Moreover, the aluminum (Al) top, bottom and gate contacts are highly beneficial for ensuring weak thermal degradation at higher temperatures. In this work, the thermal properties of Al are obtained based on density functional theory (DFT) calculations with respect to BTE [28]. Furthermore, a 5nm-SiO<sub>2</sub> gate dielectric is formed between the chromium gate and the Si nanowire channel as shown in Fig. 4 (b). Fig. 4 (c) shows the geometry of a highly p-doped single nanowire with a gate length of 18 nm leading to junctionless transition between S/D regions and the channel. More details of the technology can be found in [29-30]. To solve the thermal transport equations for this device configuration, the heat transport is coupled with the electrical characteristics. In this context, Eq. (2) is rewritten as

$$C \frac{\partial T}{\partial t} + \nabla q = P \quad (8)$$

where  $P$  is the dissipated power defined as  $P = V_{ds} I_{ds}$  [31]. To extract the thermal resistance of the device, the heat flux can be obtained as

$$q = \kappa_{eff} \frac{\Delta T}{L} \quad (9)$$

The heat flux distribution is then given by

$$q = \frac{\Delta T}{R_{th}} \quad (10)$$

where  $R_{th}$  is the thermal resistance in unit of (K/W). To obtain an accurate description of nanoscale thermal transport within the JLNT, the thermal properties of the materials chosen for our simulation are listed in Table I. The heat capacity values of silicide and Al are obtained from the material library in COMSOL.

TABLE I: THERMAL PARAMETERS OF DIFFERENT MATERIALS

Symbol	K (Wm <sup>-1</sup> K <sup>-1</sup> )	C (J m <sup>-3</sup> K <sup>-1</sup> )	$\ell$ (nm)
Si [21]	150	1.692×10 <sup>6</sup>	185
SiO <sub>2</sub> [23]	1.4	1.75×10 <sup>6</sup>	0.4
PtSi [25, 33]	18.5	2.1×10 <sup>6</sup>	-
Cr [21]	111	2.47×10 <sup>6</sup>	-
Al [25, 27]	252	2.43×10 <sup>6</sup>	10

## B. Measurements

Due to the high doping in the NW channel, on-wafer DC measurements of the JLNTs under test exhibited an increase of drain current with temperature, in contrast with conventional CMOS technologies. This can be explained by the threshold voltage reduction with temperature combined with a change in

the S/D access resistances due to thermionic emission through the Schottky contacts, along with negligible carrier mobility degradation that result in a monotonic increase in the drain current [32]. As conventional methods were not directly applicable in our case, to extract thermal resistance of the JLNTs using experimental methods, we developed several novel experimental methods using DC measurements under different temperatures along with low-frequency S-parameter measurements [22]. With these DC methods, the thermal resistance is extracted using  $R_{TH} = \Delta T/P_{diss}$  for the available transistor geometries. The extracted values thermal resistances are then compared with the simulations in subsection D for the validation of the proposed modeling framework.

## C. Comparison of thermal resistances in JLNTs and FinFETs

In this section, we compare the thermal resistance of JLNTs and SOI FinFETs as a first assessment of our simulation results. In order to ensure a reasonable comparison between both technologies, we consider a gate length of 90 nm and a  $V_{ds} = -1.5$  V. It is important to note that the model proposed in our method is solved under non-isothermal conditions. The interfacial thermal transport is governed by non-slip boundary condition given by Eq. (3). Here, the thermal resistance is extracted from the drain region where the temperature hot-spot is observed. Fig. 5 (a) compares the extracted thermal resistance as a function of the number of fins (for FinFETs) and nanowires (for JLNTs). The thermal resistance reduces with increasing number of fins and nanowires with the maximum thermal resistance  $R_{th,max}$ , observed in the drain region of the device, corresponding to fewer parallel nanowires and fins. When the number of nanowires increases, the phonon-boundary scattering becomes weak leading to enhanced reduced thermal resistance. In addition, the thermal degradation increases as the diameter reduces due to ballistic phonon transport dominating in sub 20 nm dimensions as observed from Fig. 5 (b). Interestingly, the thermal resistance observed in both p-type SOI FinFETs and JLNTs is smaller than the  $R_{th}$  extracted for n-type SOI FinFETs. This is because of the fact that p-type devices have a higher thermal conductivity compared to n-type devices [31]. In solids, electron-phonon interaction is important to understand energy flow in electronic devices. The thermal transport is affected by two types of carrier scatterings: phonon-

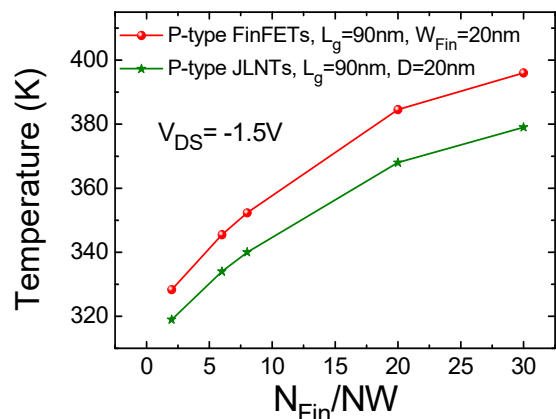


Fig. 6. Extracted device temperature in SOI FinFETs [31] and JLNTs as function of  $N_{Fin}/NW$  for  $V_{ds} = -1.5$  V.

electron and phonon-hole scattering [33]. The reduction of thermal conductivity mostly originates from phonon-electron scattering. In N-type devices, the phonon-electron interaction strongly modifies the lattice vibration which in turn influences the thermal transport and thermodynamic properties. Therefore, the thermal resistance of N-type devices is higher than that of P-type devices due to a higher phonon-electron coupling.

TABLE II - FABRICATION PROCESS PARAMETERS FOR JLNTS

Fig. 6 plots the average temperature within FinFETs and

Process Parameter	Value
Gate length	18 nm
$L$ (nanowire)	150 nm
NW in parallel	25, 36, 81
NW diameter	17, 22, 34 nm

JLNTs with respect to fins and nanowire numbers. The temperature increases with increasing  $N_{Fin}$  and  $NWs$  as the dissipated power  $P$  also increases. For  $N_{Fin}/Nws = 2$  and 6, one can observe a temperature difference,  $\Delta T$ , of around 8 K. However,  $\Delta T$  reaches 17 K for large number of fins and nanowires ( $N_{Fin}/Nws = 20$  and 30). It is to be noted that SOI FinFETs have a higher temperature increase than those extracted for JLNTs, due to a more confined flow of the phonons, indicating better thermal stability for the latter case. The extracted thermal conductivity in SOI FinFETs is found to be 8 W/m/K, whereas it reaches 10 W/m/K for the JLNTs [34]. In the other words, the thermal transport mechanism is more resistive in the FinFETs.

#### D. Nanoscale Thermal Transport in GAA JLNTs

The GAA structure offers the advantage of better thermal stability of nanoscale devices [18], [35]. In order to further understand the heat dissipation in JLNTs, we carried out multiscale GKE model simulation for JLNT geometries diameter 17, 22 and 34 nm with different number of nanowires in parallel, for the operating condition  $V_{ds}=V_{gs}=-2 V$ . Table II lists the JLNTs geometries used for simulation in this work. Fig. 7 shows the extracted thermal resistance in the JLNTs for different diameters and nanowires, comparing device simulation and measurement results from section B. The thermal simulations were performed using an extremely fine mesh with 65000 spatial grids around the transistor active area

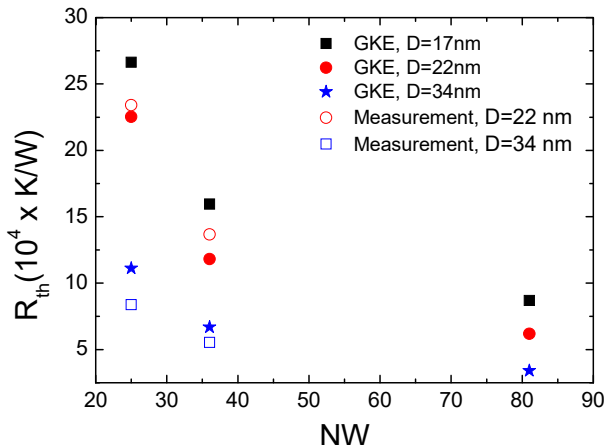


Fig. 7. The extracted thermal resistance in JLNTs as a function of number of nanowires comparing simulation and measurements.

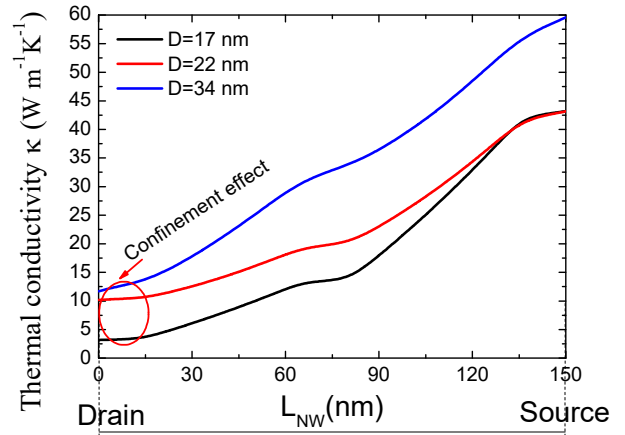


Fig. 8. Effective thermal conductivity along the nanowire for different diameters.

to facilitate solving the GKE model. The maximum lattice temperature is obtained from the dissipated power calculated from  $I_{ds}-V_{ds}$  characteristics. As expected, the thermal resistance decreases with increasing nanowires in parallel, whereas, it increases when diameters are scaled down. In particular, for small diameters, the thermal resistance increases due to phonon confinement effects occurring as a result of the surface roughness which, in turn, results in a loss of momentum and eventually a strong resistive transport at room temperature. For  $D = 17 nm$ , the thermal resistance decreases from  $2.66 \times 10^5 K/W$  to  $7.4 \times 10^4 K/W$  with increasing number of parallel NWs ( $NW = 25$  to 81). Similarly, for  $D = 34 nm$ , the  $R_{th}$  decreases from  $1.12 \times 10^5 K/W$  to  $3.3 \times 10^4$  for  $NW = 25$  and 81, respectively. As depicted in Fig. 7, our simulation results agree quite well with measurements for  $D = 22 nm$  and  $D = 34 nm$ . As observed from the trend in Fig. 7, thermal resistance is significantly influenced by the NW diameter, however, for a higher number of NWs in parallel, the spreading of the thermal resistance values with diameter reduces. Fig. 8 shows the thermal conductivity of the JLNTs along the channel direction with 25 nanowires in parallel extracted from the device

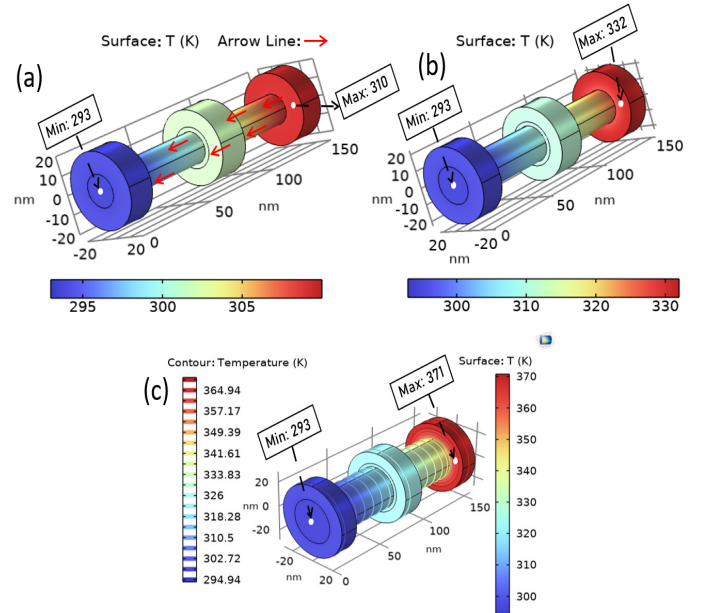


Fig. 9. The temperature distribution within a single nanowire of (a)  $D= 17 nm$ . (b)  $D= 22 nm$  and (C)  $D= 34 nm$ . The arrow indicates the direction of the heat propagation.

simulation. As expected, the lower ETC of the nanowire is directly associated to higher thermal resistance in small dimeters, which, in turn, may lead to pronounced SHEs. It is to be noted that, the ETC reaches 3.26 W/m/K and 11.6 W/m/K for  $D = 17 \text{ nm}$  and  $D = 34 \text{ nm}$ , respectively. The reduction of the thermal conductivity is mostly caused by phonon confinement effects in the drain area (the hot-spot region). Close to the drain area, phonon transport takes place in the ballistic regime and boundary scattering takes place which influences the thermal conductivity. The phonon-boundary scattering rate is significantly high in low dimensional materials which can be held responsible for the weak value of the ETC for  $D = 17 \text{ nm}$ . In addition, for nanowires of diameter smaller than 50 nm, the Young's modulus is likely another factor governing the thermal transport. Incoherent phonon scattering can also impact the heat propagation, which further reduces the thermal conductivity [36]. In general, in sub-10 nm nanowires, incoherent phonon scattering leads to a backscattering mechanism (i.e. resistive effects) which degrades the phonon momentum and thermal conductivity. The temperature hot-spots appear due to the dominance of resistive heat transport. When the thermal conductivity reduces, heat carriers (phonon) are confined in a small space which leads to an accumulation of the heat. The physical phenomena behind the confinement mechanism can be explained by the Lévy walk [37], in which the phonons are trapped in the nanowire through short flights between the boundary and the nanowire. Phonon Lévy flight has been experimentally observed in silicon nanowires which result in the reduction of thermal conductivity in the quasi-ballistic regime. Therefore, the increase of device temperature and the reduction of the thermal conductivity can mainly be explained by the confinement effect. Our simulations results demonstrate that the confinement effect is very weak at the source side. It is expected that the effective thermal conductivities of the devices with  $D=17 \text{ nm}$  and  $D=22 \text{ nm}$  are quite close. Near the source region, the heat transport is less resistive and phonons experience less boundary scattering, therefore leading to a higher thermal conductivity.

For subsequent analyses on heat propagation, we focused on a single nanowire. Fig. 9 plots the simulated distribution of internal device temperature in JLNTs for different diameters. The maximum temperature is detected near the drain region which then gradually diminishes towards the channel layer. Interestingly, the effective temperature rise with increasing diameter is the combined effect of increasing dissipated power  $P$  and reducing thermal resistance in larger diameters. For smaller diameters, in Fig. 9 (a) and Fig. 9 (b), the heat flow is localized in the drain side which then propagates along the nanowire. However, in Fig. 9 (c) for largest diameter (34 nm), the heat accumulation spreads over the drain side only. Furthermore, temperature distributions for smaller diameters are indicative of the thermal confinement near the drain region that leads to elevated temperature higher thermal energy. Further reduction in internal device temperature can be achieved by increasing the diameter and nanowires in parallel.

#### IV. CONCLUSION

In this paper, we investigated nanoscale thermal transport beyond Fourier's law in GAA-JLNTs for the first time using Guyer-Krumhansl equation developed for thermal parameter

extraction. In particular, we demonstrated that non-Fourier heat modeling is an efficient method for understanding heat flow in more-Moore nanoelectronic devices. Our developed simulation framework was used to investigate thermal transport in both FinFETs and JLNTs indicating better thermal stability of the latter technology. Comparison of thermal resistance of the JLNTs from measurements [22] and our proposed model demonstrated excellent agreement validating the accuracy of the proposed modeling framework. Further analysis suggested that a high thermal conductivity is recommended for better control of heat dissipation and reduction of temperature hot-spots in JLNTs. Moreover, JLNTs with larger diameters and higher number of nanowires in parallel clearly demonstrate a higher efficiency for heat dissipation through the 3D vertical nanowire architecture. Further investigation of electro-thermal behavior of the JLNT technology under study will focus on electron-phonon coupling and its impact on thermal transport.

#### REFERENCES

- [1] A. K. Gundu, and V. Kursun, "5-nm Gate-All-Around transistor technology with 3-D stacked nanosheets," *IEEE Trans. Electron Device*, vol. 69, no. 3, pp. 922–929, Mar. 2022. [10.1109/TED.2022.3143774](https://doi.org/10.1109/TED.2022.3143774)
- [2] S. Kim *et al.*, "Investigation of device performance of fin angle optimization in FinFET and Gate-All-Around FETs for 3 nm-node and beyond," *IEEE Trans. Electron Device*, vol. 69, no. 4, pp. 2088–2093, Apr. 2022. [10.1109/TED.2022.3154683](https://doi.org/10.1109/TED.2022.3154683)
- [3] A. Sudarsanan, S. Venkateswarlu, and K. Nayak, "Impact of fin line edge roughness and metal gate granularity on variability of 10-nm node SOI n-FinFET," *IEEE Trans. Electron Device*, vol. 66, no. 11, pp. 4646–4652, Nov. 2019. [10.1109/TED.2019.2941896](https://doi.org/10.1109/TED.2019.2941896)
- [4] A. M. Ionescu, "Nanowire transistors made easy," *Nat. Nanotechnol.* vol. 5, no. 5, pp. 178–179, Mar. 2010. [10.1038/nnano.2010.38](https://doi.org/10.1038/nnano.2010.38)
- [5] G. Larrieu, and X.-L. Han, "Vertical nanowire array-based field effect transistor for ultimate scaling," *Nanoscale*, vol. 5, pp. 2437–41, Jan. 2013. [10.1039/c3nr33738c](https://doi.org/10.1039/c3nr33738c)
- [6] J. P. Colinge C.-W. Lee, A. Afzal, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, pp. 225–229, Feb. 2010. [10.1038/nnano.2010.15](https://doi.org/10.1038/nnano.2010.15)
- [7] C. Mukherjee, A. Poittevin, I. O'Connor, G. Larrieu, and C. Maneux, "Compact modeling of 3D vertical junctionless gate-all-around silicon nanowire transistors towards 3D logical design," *Solid-State Electron.* vol. 183, p. 108125, Sep. 2021. [10.1016/j.sse.2021.108125](https://doi.org/10.1016/j.sse.2021.108125)
- [8] A. L. Moore, and L. Shi, "Emerging challenges and materials for thermal management of electronics," *Mater. Today*, vol. 14, no. 4, pp. 163–174, May 2014. [10.1016/j.mattod.2014.003](https://doi.org/10.1016/j.mattod.2014.003)
- [9] A. Shakouri, "Nanoscale thermal transport and microrefrigerators on a chip," *Proc. IEEE*, vol. 94, no. 8, pp. 1613–1638, Aug. 2006. [10.1109/JPROC.2006.879787](https://doi.org/10.1109/JPROC.2006.879787)
- [10] U. K. Das, and T. K. Bhattacharyya, "Opportunities in device scaling for 3-nm node and beyond: FinFET versus GAA-FET versus UFET," *IEEE Trans. Electron Dev.* vol. 67, no. 6, pp. 2638–2638, Apr. 2020. [10.1109/TED.2020.2987139](https://doi.org/10.1109/TED.2020.2987139)
- [11] J. Fourier, *Théorie analytique de la chaleur* (chez Firmin Didot, père et fils). 1822.
- [12] Y. Guo and M. Wang, "Phonon hydrodynamics for nanoscale heat transport at ordinary temperatures," *Phys. Rev. B*, vol. 97, pp. 035421–27, Jan. 2018. [10.1103/PhysRevB.97.035421](https://doi.org/10.1103/PhysRevB.97.035421)
- [13] J. Lee, J. Lim, and P. Yang, "Ballistic phonon transport in holey silicon," *Nano Lett.* vol. 15, pp. 3273–3279, 2015. [10.1021/acs.nanolett.5b00495](https://doi.org/10.1021/acs.nanolett.5b00495)
- [14] S. Know, M. C. Wingert, J. Zheng, J. Xiang, and R. Chen, "Thermal transport in Si and Ge nanostructure in the 'confinement' regime," *Nanoscale*, vol. 8, no. 27, pp. 13155–13167, Jun. 2016. [10.1039/C6NR03634A](https://doi.org/10.1039/C6NR03634A)
- [15] J. Maire, R. Anufriev, and M. Nomura, "Ballistic thermal transport in silicon nanowires," *Sci. Rep.*, vol. 7, p. 41794; Feb. 2017. [10.1038/srep41794](https://doi.org/10.1038/srep41794)
- [16] D. Jou, J. Casas-Vazquez, and G. Lebon, *Extended Irreversible Thermodynamics*, (Springer, Heidelberg, 2010). [10.1007/978-90-481-3074-0](https://doi.org/10.1007/978-90-481-3074-0)

- 
- [17] R. Anufriev, S. Gluchko, S. Volz, and M. Nomura, "Quasi-ballistic heat conduction due to Lévy phonon flights in silicon nanowires," *ACS Nano*, vol. 12, no. 12, pp. 11928–11935, Nov. 2018. [10.1021/acsnano.8b07597](https://doi.org/10.1021/acsnano.8b07597)
- [18] J. Lai, Y. Su, J. Bu, B. Li, B. Li, and G. Zhang, "Study on degradation mechanisms of thermal conductivity for confined nanochannel in Gate-All-Around silicon nanowire field-effect transistors," *IEEE Trans. Electron Dev.*, vol. 99, pp. 1–7, Aug. 2020. [10.1109/TED.2020.3014557](https://doi.org/10.1109/TED.2020.3014557)
- [19] A. Beardo, M. Calvo-Schwarzwälder, J. Camacho, T.G. Myers, P. Torres, L. Sendra, F.X. Alvarez, and J. Bafaluy, "Hydrodynamic heat transport in compact and holey silicon thin films," *Phys. Rev. App.*, vol. 11, no. 3, pp. 034003–8, Mar. 2019. [10.1103/PhysRevApplied.11.034003](https://doi.org/10.1103/PhysRevApplied.11.034003)
- [20] R.A. Guyer, and J.A. Krumhansl, "Thermal conductivity, second sound, and phonon hydrodynamic phenomena in nonmetallic crystals," *Phys. Rev.*, vol. 148, Aug. 1966. [10.1103/PhysRev.148.778](https://doi.org/10.1103/PhysRev.148.778)
- [21] A. Beardo, M. G. Hennessy, L. Sendra, J. Camacho, T.G. Myers, J. Bafaluy, and F.X. Alvarez, "Phonon hydrodynamics in frequency-domain thermoreflectance experiments," *Phys. Rev. B.*, vol. 101, no. 7, pp. 075303–12, Feb. 2020. [10.1103/PhysRevB.101.075303](https://doi.org/10.1103/PhysRevB.101.075303)
- [22] C. Mukherjee, H. Rezgüi, Y. Wang, M. Deng, A. Kumar, J. Muller, G. Larrieu, C. Maneux, "Nanoscale Thermal Transport in Vertical Gate-all-around Junction-less Nanowire Transistors- Part I: Experimental Methods", *IEEE Trans. Electron Dev.* 2023. (submitted)
- [23] A. Beardo, M. López-Suárez, L. A. Pérez, L. Sendra, M. I. Alonso, C. Melis, J. Bafaluy, J. Camacho, L. Colombo, R. Rurali, F. X. Alvarez, and J. S. Reparaz, "Observation of second sound in a rapidly varying temperature field in Ge," *Sci. Adv.*, vol. 7, no. 27, pp. 1–6, Jun 2021. [10.1126/sciadv.abg4677](https://doi.org/10.1126/sciadv.abg4677)
- [24] H. Rezgüi, F. Nasri, M. F. Ben Aissa, and A.A. Guizani, "Investigation of nanoscale heat transport in sub-10 nm carbon nanotube field-effect transistors based on finite element method," *Therm. Sci. Eng. Prog.*, vol. 25, pp. 100938, Oct. 2021, [10.1016/j.tsep.2021.100938](https://doi.org/10.1016/j.tsep.2021.100938)
- [25] COMSOL, Inc., COMSOL Multiphysics.
- [26] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar, "Thermal conductivity of individual silicon nanowires," *App. Phys. Lett.*, vol. 83, no. 14, pp. 2934–2936, Oct. 2003. [10.1063/1.1616981](https://doi.org/10.1063/1.1616981)
- [27] A. M. Marconnet, T. Kodama, M. Asheghi, and K. E. Goodson, "Phonon conduction in periodically porous silicon nanobridges," *Nano. Micro. Thermophys. Eng.*, vol. 16, pp. 199–219, Dec. 2012. [10.1080/15567265.2012.73219](https://doi.org/10.1080/15567265.2012.73219)
- [28] A. Jain, and A. J. H. McGaughey, "Thermal transport by phonons and electrons in aluminum, silver, and gold from first principles," *Phys. Rev. B*, vol. 93, pp. 081206, Feb. 2016. [10.1103/PhysRevB.93.081206](https://doi.org/10.1103/PhysRevB.93.081206)
- [29] G. Larrieu Y. Guerfi, X. L. Han, N. Clément, "Sub-15 nm gate-all-around field effect transistors on vertical silicon nanowires" *Solid-State Electron.*, 130, 9-14, 2017. [10.1016/j.sse.2016.12.008](https://doi.org/10.1016/j.sse.2016.12.008)
- [30] Y. Guerfi, G. Larrieu "Vertical silicon nanowire field effect transistors with nanoscale gate-all-around" *Nanoscale Res. Lett.* Vol. 11, pp. 210, 2016. [10.1186/s11671-016-1396-7](https://doi.org/10.1186/s11671-016-1396-7)
- [31] H. Jiang, N. Xu, B. Chen, L. Zeng, Y. He, G. Du, X. Liu and X. Zhang, "Experimental investigation of self heating effect (SHE) in multiple-fin SOI FinFETs," *Semicond. Sci. Technol.*, vol. 29, no. 11, pp. 115021–7, 2014. [10.1088/0268-1242/29/11/115021](https://doi.org/10.1088/0268-1242/29/11/115021)
- [32] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "High-Temperature Performance of Silicon Junctionless MOSFETs," *IEEE Trans. Electron Dev.*, vol. 57, no. 3, pp. 620–625, March 2010. [10.1109/TED.2009.2039093](https://doi.org/10.1109/TED.2009.2039093)
- [33] J. Zhou, H.D Shin, K. Chen, B. Song, R.A. Duncan, Q. Xu, A.A. Maznev, K.A. Nelson, and G. Chen, "Direct observation of large electron-phonon interaction effect on phonon heat transport," *Nat. Comm.* vol. 11, no. 6040, Nov. 2020. [10.1038/s41467-020-19938-9](https://doi.org/10.1038/s41467-020-19938-9)
- [34] G. Larrieu, H. Rezgüi, A. Kumar, J. Müller, S. Pelloquin, Y. Wang, M. Deng, A. Lecestre, C. Maneux, and C. Mukherjee, "Thermal consideration in nanoscale gate-all-around vertical transistors, 2023 Silicon Nanoelectronics Workshop (SNW). [10.23919/SNW57900.2023.10183951](https://doi.org/10.23919/SNW57900.2023.10183951)
- [35] I. Jain, A. Gupta, T.B. Hook, and A. Dixit, "Modeling of effective thermal resistance in sub-14 nm stacked nanowire and FinFETs," *IEEE Trans. Electron Dev.* vol. 65, no. 10, pp. 4238–4244, Oct. 2018. [10.1109/TED.2018.2863730](https://doi.org/10.1109/TED.2018.2863730)
- [36] J. Ravichandran, A. K Yadav, R. Cheaito, P. B. Rossen, A. Soukiassian, S. J. Suresha *et al.*, "Crossover from incoherent to coherent phonon scattering in epitaxial oxide superlattices," *Nat Mater*, vol. 13, pp: 168–72, 2014, doi: [10.1038/nmat3826](https://doi.org/10.1038/nmat3826).
- [37] R. Anufriev, S. Gluchko, S. Volz, M. Nomura, "Quasi-ballistic heat conduction due to Lévy phonon flights in silicon nanowires," *ACS Nano*, vol. 12, no. 12, pp. 11928–11935, Nov. 2018. [10.1021/acsnano.8b07597](https://doi.org/10.1021/acsnano.8b07597)