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► **To cite this version:**

Mukherjee Chhandak, H. Rezgui, Y. Wang, M. Deng, A. Kumar, et al.. Nanoscale Thermal Transport in Vertical Gate-All-Around Junctionless Nanowire Transistors-Part I: Experimental Methods. IEEE Transactions on Electron Devices, 2023, pp.1-7. 10.1109/TED.2023.3321277 . hal-04296517

**HAL Id: hal-04296517**

**<https://hal.science/hal-04296517v1>**

Submitted on 20 Nov 2023

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# Nanoscale Thermal Transport in Vertical Gate-all-around Junction-less Nanowire Transistors - Part I: Experimental Methods

C. Mukherjee, *Member, IEEE*, H. Rezgui, *Member, IEEE*, Y. Wang, *Member, IEEE*, M. Deng, *Member, IEEE*, A. Kumar, J. Müller, G. Larrieu, *Member, IEEE*, C. Maneux, *Member, IEEE*

**Abstract**—In this paper, we present the first detailed experimental study of electro-thermal effects in 3D vertical gate-all-around junctionless nanowire transistors (JLNT). In contrast with conventional CMOS technologies, JLNTs exhibit steady increase of current with temperature owing to weak mobility degradation in the highly doped nanowires. Consequently, in this work, we proposed novel experimental methods for extracting thermal resistance using DC and low-frequency S-parameter measurements. Experimental results obtained from different methods are validated against theoretical as well as simulated values obtained from multiphysics simulation of JLNTs.

**Index Terms**—Junctionless nanowire transistors, electro-thermal effects, thermal resistance, thermal capacitance, low-frequency S-parameter, multiphysics simulation.

## I. Introduction

JUNCTIONLESS transistors are being considered off late as a promising beyond-CMOS technological alternative to sustain miniaturization in sub-20 nm technological nodes [1]. Recent years have seen a major paradigm shift in computing hardware to cater to a multitude of neuromorphic applications based on artificial neural networks. To meet the low-power, low-latency criteria [2] for in-memory computing and to overcome the bottlenecks of conventional von-Neumann architectures, the search for potential breakthrough technologies has imposed additional technological constraints on semiconductor manufactures [3]. In this context, vertical junctionless nanowire transistors (JLNT) have shown promise to unlock the full potential of 3D circuit density [4] and performance [5]. JLNTs [6] are not only being seen as a future mainstream technological solution for in-memory computing capable of relaxing the fabrication process challenges due to downscaling, such as short channel effects, leakage currents and gate electrostatic control [7] owing to their gate-all-around (GAA) structures [2] particularly suitable for integrated ferroelectric gate as memory [3, 8], but they can also be fabricated through a simpler process without forming ultra-sharp source-drain junctions in nanoscale devices owing to their constant doping profile across the source-drain region [7].

This work was supported by the project FVLLMONTI funded by European Union's Horizon 2020 research and innovation program under grant agreement N°101016776 and by the LAAS-CNRS micro and nanotechnologies platform, a member of the Renatech French national network.

Vertical arrays of junctionless nanowire transistors are particularly interesting for innovative 3D logic circuits all the while maintaining scaling-friendly [9], low-energy and area-efficient, compact designs [10] through multiple gate-level stacking [3]. However, with denser design and optimized interconnect routing, impact of underlying electrothermal phenomena on performance metrics such as power and latency can become more significant due to thermal confinement in the nano-scale vertical JLNTs [11]. Thermal management thus remains a constraint for design-technology-co-optimization for neuronal circuit design [2]. The operation of junctionless transistors under low and high temperatures has been investigated and analyzed experimentally [12-15], and through electrothermal simulations [16-19] previously. However, existing studies lack in-depth understanding of nanoscale electro-thermal phenomena and thermal parameter extraction methodology compatible with compact modelling [20].

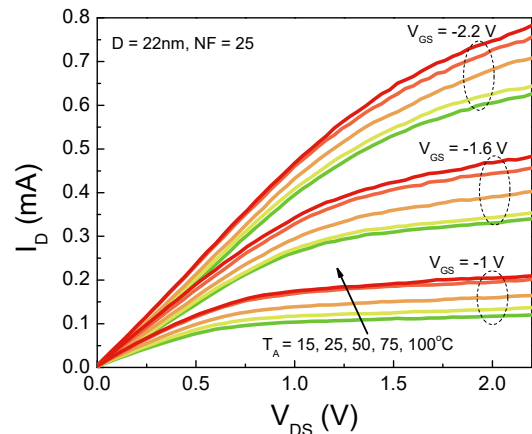


Fig. 1. Drain current as a function of drain-source voltage at fixed gate biases and under a wide range of measurement temperatures for a p-type JLNT [13-15] with NW diameters (D) of 22 nm with 25 NWs in parallel (NF).

It is generally observed that temperature-dependence of JLNT drain current differ from that of conventional MOS devices owing to the absence of zero temperature coefficients (ZTC) in JLNTs. In particular, ZTC points, at which drain current remains constant despite the change in temperature at fixed bias, are of particular interest for certain analog circuits such as

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operational transconductance amplifier [21]. In conventional CMOS technologies, with increasing temperature, the drain current reduces as a net result of the reduction of threshold voltage and a reduction of the mobility due to increased phonon scattering at higher temperatures [22]. In contrast, in junctionless transistors, a linear increase of drain current with temperature is reported [12], similar to what has also been observed from our measurements (Fig. 1). This behavior is attributed to a strong temperature dependence of the threshold voltage and an almost negligible variation in mobility with temperature [12, 13], leading to the absence of ZTCs in JLNTs [14]. In particular, the weak temperature dependence of the mobility has been attributed to the two competing mechanisms, phonon and impurity scattering, which show  $T^{-3/2}$  and  $T^{3/2}$  dependences, respectively, thereby strongly compensating each other [23]. This behavior of the drain current in sub-20 nm junctionless nanowire transistors particularly calls for novel thermal extraction methods in addition to the need for improved understanding of electro-thermal effects and optimize heat transport as well as enhance thermal management and stability.

In this paper, we present for the first time, experimental methods for thermal parameter extraction in 18 nm vertical JLNTs, aided by the understanding of nanoscale thermal transport through Multiphysics simulations, towards SPICE compact model development [20] for circuit level design explorations. These scaled devices, composed of a homogenous highly doped nanowire channel, patterned into boron doped ( $2 \times 10^{19} \text{cm}^{-3}$ ) Si-substrate with nanoscale metallic GAA including symmetrical silicided source and drain contacts, show very good immunity against short channel effect with NW diameter up to 40 nm and  $I_{\text{on}}/I_{\text{off}}$  ratio up to 5 decades [24, 25]. The JLNTs under test, including a wide range of nanowire diameters, ranging between 17 and 34 nm, with 16, 25, 36 and 49 nanowires in parallel, were characterized using several novel experimental methods, to extract thermal impedance of these devices. In particular, we employed both DC measurements under a wide range of temperature as well as low-frequency S-parameter measurements in order to extract thermal resistance and capacitances of this technology and compared the results to theoretical predictions as well as multiphysics simulations carried out using COMSOL software [26], detailed in part II of this work [27]. The rest of this paper is organized as follows: In the section II, we present the principles of our experimental methods. Section III discusses the results comparing extracted thermal resistances obtained from the different experimental methods with theoretical and multiphysics simulation results thereby commenting on the accuracy of each technique. We also present an accurate equivalent electro-thermal network representation of the JLNTs. Finally, section IV presents conclusions and perspectives.

## II. EXPERIMENTAL METHODS

### A. DC extraction methods

From all of our DC measurements, we observed a linear dependence of the drain current with measurement temperature (Fig. 2). As a first estimate of the thermal resistance of the JLNTs, we calculated the ratio of the change in temperature to that of the dissipated power. For this, we first considered an

operating point with as high  $V_{\text{GS}}$  and  $V_{\text{DS}}$  (-2.2 V both) as permissible, where thermal effects are expected to dominate. Next, at the fixed value of  $V_{\text{GS}}$  and  $V_{\text{DS}}$ , we monitored the drain current increase with the temperature from  $I_{\text{D}}-V_{\text{D}}$  and  $I_{\text{D}}-V_{\text{G}}$  measurements. Then thermal resistance was estimated using,

$$R_{\text{TH}} = \frac{\Delta T}{\Delta P_{\text{diss}}} = \frac{1}{V_{\text{DS}}} \frac{\Delta T}{\Delta I_{\text{D}}} \quad (1)$$

Where,  $P_{\text{diss}}$  is the power dissipation which is calculated from the product  $V_{\text{DS}} \times I_{\text{D}}$ . The second term in (1) was then extracted from the slope of  $I_{\text{D}}$  vs.  $T_{\text{A}}$  plots at fixed  $V_{\text{GS}}$  and  $V_{\text{DS}}$  (Fig. 2).

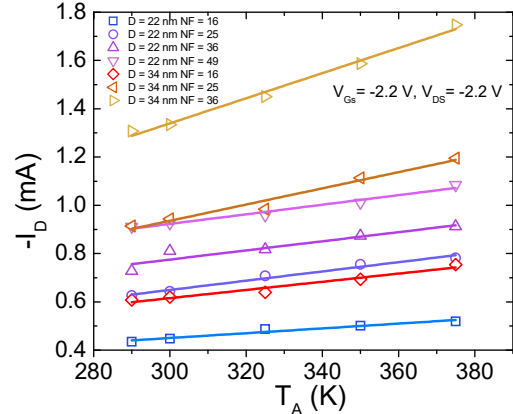


Fig. 2. Drain current as a function of different measurement temperatures,  $T_{\text{A}}$ , for the p-type JLNT geometries under study at  $V_{\text{GS}} = -2.2$  V and  $V_{\text{DS}} = -2.2$  V showing the linear fits associated with each device.

Even though this method (M1) provides a first estimation of thermal resistance in the JLNTs under test, we explored other more accurate extraction methods. For the second method (M2), we use  $I_{\text{D}}-V_{\text{GS}}$  characteristics at different measurement temperatures ( $T_{\text{A}}$ ) to estimate the  $R_{\text{TH}}$  from the intersecting points between these curves (Fig. 3) using the relation of junction temperature ( $T_{\text{j}}$ ), i.e. the internal device temperature,

$$T_{\text{j}} = T_{\text{A}} + P_{\text{diss}} R_{\text{TH}}, \quad (2)$$

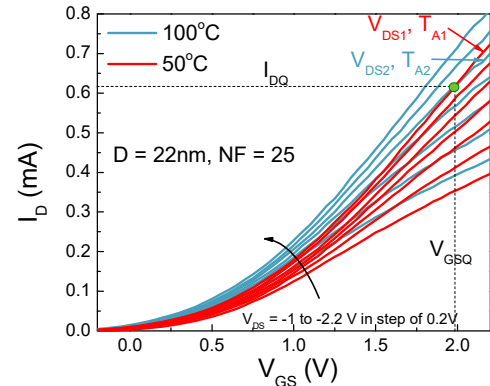


Fig. 3.  $I_{\text{D}}-V_{\text{GS}}$  characteristics of a JLNT at two different  $T_{\text{A}}$  showing the intersecting points ( $I_{\text{DQ}}$ ,  $V_{\text{GSQ}}$ ) of two curves with different  $V_{\text{DS}}$ .

The principle of this method is based on the fact that at the intersecting points, the drain current and gate voltages ( $I_{\text{DQ}}$ ,  $V_{\text{GSQ}}$ ) are the same for two different sets of drain voltages ( $V_{\text{DS1}}$  and  $V_{\text{DS2}}$ ) and measurement temperatures ( $T_{\text{A1}}$  and  $T_{\text{A2}}$ ). As a first step, we theorize that the two junction temperatures ( $T_{\text{j1}}$  and  $T_{\text{j2}}$ ) at the intersecting point are equal, for which the increase in  $T_{\text{A}}$  is compensated by the reduction in  $V_{\text{DS}}$  for the two intersecting curves. For this compensation, we also consider that the  $R_{\text{TH}}$  should be extracted at a bias point with  $V_{\text{GS}}$  and  $V_{\text{DS}}$  as high as possible and that intersecting points at

lower bias would give overestimated values. The  $R_{TH}$  can thus be extracted by equating the two junction temperatures at the intersecting point:  $R_{TH} = (T_{A2} - T_{A1}) / I_{DQ}(V_{DS1} - V_{DS2})$ .

To minimize the relative error associated with these DC methods, in the third DC method (M3), we consider the ratio of relative variations with two input quantities for an intermediate physical device parameter, such as the threshold voltage which strongly depends on both drain bias and temperature [12, 13]. Since the temperature dependence of drain current is principally governed by threshold voltage variation ( $\Delta V_T$ ) in the JLNTs, for method (M3), we extracted the threshold voltage at different temperatures using the transconductance method [28], which relies on estimating the threshold voltage from the gate voltage where the value of the ratio transconductance  $g_m (= \partial I_D / \partial V_{GS})$  to the current  $I_D$  ( $g_m / I_D$ ) has reduced to half its peak value. This method is particularly suited to junctionless devices and is often preferred to other methods that produce more noisy data [28], which introduce additional uncertainty in threshold voltage extraction. Nonetheless, the  $g_m / I_D - V_{GS}$  plots also exhibited oscillation, especially for smaller devices and a hyperbolic smoothing function was used to extract an average  $V_T$  [28]. The extracted  $V_T$  values show a linear dependence with temperature depicting a positive slope, similar to what has been reported for p-type JNTs in [14]. From the slope of these curves (Fig. 4), the values of the thermal resistance can be estimated as,

$$R_{TH} = \frac{\Delta T}{\Delta P_{diss}} = \frac{1}{I_D} \frac{\Delta V_T}{\Delta V_{DS}} \frac{\Delta V_T}{\Delta T} \quad (3)$$

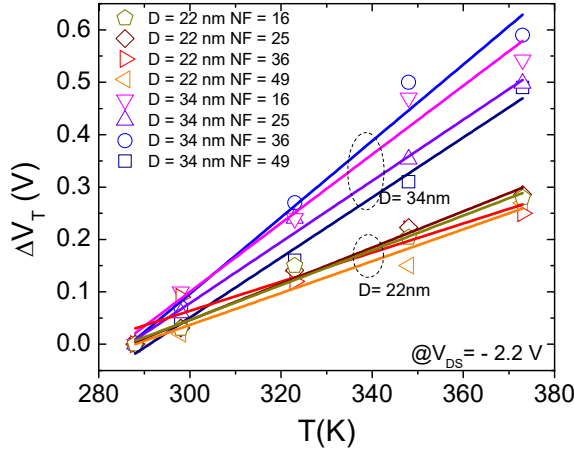


Fig. 4. Threshold voltage shift of the JLNTs under test (with different diameters and nanowires in parallel) as a function of measurement temperature.

The fourth method (M4) also relies on the slopes of the  $I_D$  vs.  $T_A$  plots at high  $V_{GS}$  and  $V_{DS}$ . From the linear dependence of  $I_D$  with the temperature,  $T_A$ , observed for all devices (Fig. 2), we can write the following linear function,

$$I_D = I_{D0}(1 + m_A(T_A - T_{A0})) \quad (4)$$

Where,  $I_{D0}$  is the drain current at nominal temperature,  $T_{A0}$ , (in our case, at 15°C), and  $m_A$  is the slope of the  $I_D$ - $T_A$  curve that can be calculated as  $m_A = (dI_D/dT_A) / I_{D0}$ . In the same temperature range, the junction temperature is governed by (2) in which  $P_{diss} (V_{DS} \times I_D)$  is also a linear function of  $T_A$  at a fixed  $V_{DS}$  and one can assume that  $I_D$  is a linear function of  $T_j$  as well. So a linear relation between these two exists as,

$$I_D = I_{D0}(1 + m_j(T_j - T_{j0})) \quad (5)$$

Where  $m_j$  is the slope of the  $I_D$ - $T_j$  curve. Now, using (2), the change in the junction temperature can be written as,

$$T_j - T_{j0} = T_A - T_{A0} + V_{DS}R_{TH}(I_D - I_{D0}), \quad (6)$$

Substituting (6) in (5) gives,

$$I_D = I_{D0}(1 + m_j(T_A + T_{A0} + V_{DS}R_{TH}(I_D - I_{D0}))), \quad (7)$$

Differentiating with respect to  $T_A$ , we obtain,

$$\frac{dI_D}{dT_A} = I_{D0}m_j(1 + V_{DS}R_{TH}\frac{dI_D}{dT_A}) \equiv \frac{dI_D}{dT_A} = \frac{I_{D0}m_j}{1 - I_{D0}m_jV_{DS}R_{TH}} \quad (8)$$

Replacing  $(dI_D/dT_A) / I_{D0}$  by  $m_A$ , one can write,

$$\frac{1}{m_A} = \frac{1}{m_j} - I_{D0}V_{DS}R_{TH}. \quad (9)$$

In (9),  $m_A$  can be extracted from the measured  $I_D$ - $T_A$  plots at different  $V_{DS}$  and from the slope of  $1/m_A$  vs.  $I_{D0}V_{DS}$ , one can extract the  $R_{TH}$ .

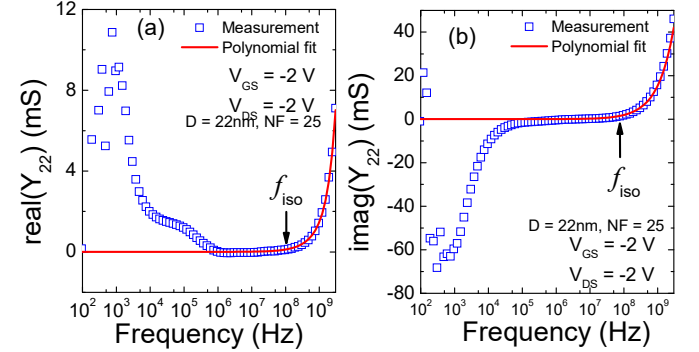


Fig. 5. Extraction of isothermal electrical contributions from (a) real and (b) imaginary parts of the  $Y_{22}$  parameter using polynomial fit.

## B. Low-frequency S-parameter measurements

Low-frequency (LF) S-parameter measurements are an effective way of studying dynamic self-heating in modern transistors [29]. LF S-parameter measurement method has been proven to be quite effective for isolating pure electrical and non-linear electrothermal effects and estimate the values of the elements of the electrothermal networks in bipolar [30] and MOS transistors [29]. Thermal impedance is a particularly crucial parameter for device compact models when evaluating circuit performances under dynamic conditions especially in scaled devices. In a two-terminal device, at higher frequencies, where thermal response is too slow compared to the operating frequency, the frequency response is dominated by the device's electrical capacitances. Hence, S-parameters measured at lower frequencies are used to study the dynamic self-heating. Based on this principle, we performed on-wafer LF S-parameter measurements on different JLNT geometries. The measurement setup consists of a semiconductor parameter analyzer, HP 4152, for DC biasing and a vector network analyzer, Agilent E5061B (5Hz-3GHz). In order to couple RF and DC bias, bias tees (bandwidth of 30 kHz to 3 GHz) were used. A standard SOLT calibration [31] was used with an RF input power of -28 dBm, followed by open-short de-embedding. The thermal impedance was then extracted in the 30 kHz-300 MHz range beyond which pure electrical effects dominate the measured S-parameters. DC bias points were chosen with high  $V_{GS}$  and  $V_{DS}$  where self-heating effects are most likely observable. The measured S-parameters were then converted to Y-parameters that are used for extracting thermal impedance. Pure electrical characteristics of the device dominate at higher frequencies in the Y-parameter vs. frequency plot. So the frequency that separates these two mechanisms, i.e. an isothermal frequency ( $f_{iso}$ ), can be identified from the  $Y_{22}(f)$ , i.e. drain conductance, as illustrated in Fig. 5. Essentially, in the low frequency range before  $f_{iso}$ , one can

extract parameters of dynamic thermal response, while above  $f_{iso}$ , pure electrical, i.e. isothermal, characteristics of the device dominates. Based on the theoretical analysis in [32], the thermal impedance can be represented in terms of its Y parameters as,

$$Z_{TH}(f) = \frac{[Y_{22}(f) - Y_{22}^{iso}(f)]}{\frac{dI_D}{dT_A} [I_{DS} + V_{DS} Y_{22}(f) + V_{GS} Y_{12}(f)]} \quad (10)$$

The  $Y_{22}^{iso}(f)$  is the isothermal electrical contribution that can be estimated by fitting polynomials to the real and imaginary parts of  $Y_{22}$  (Fig. 5) and then reconstructing  $Y_{22}^{iso}(f)$  [29]. The  $dI_D/dT_A$  term has been extracted from the DC measurements earlier in Fig. 4. Finally, from (10), the thermal impedance of the JLNTs can be calculated from measured LF S-parameters.

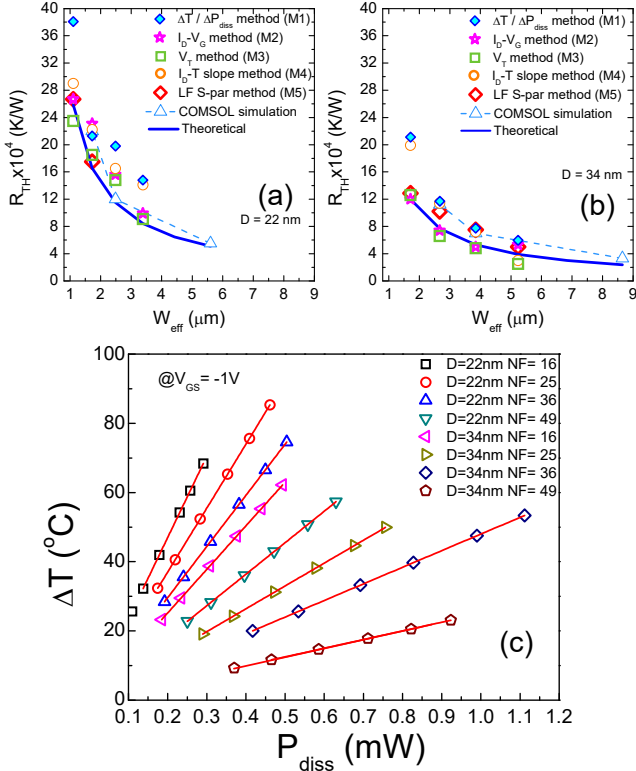


Fig. 6. (a) Extracted thermal resistances as a function of the effective transistor width,  $W_{eff}$  ( $= \pi DNF$ ), as obtained from the four experimental DC methods and the LF S-parameter method in comparison with theoretical predictions and COMSOL simulations [27]; (b) Rise of internal device temperature as a function of dissipated power for the available JLNT geometries

### III. RESULTS AND DISCUSSION

#### A. Thermal resistance extraction

DC measurements performed at different temperatures (15-100  $^{\circ}\text{C}$ ), which revealed a steady increase of the drain current with temperature, were used for all four DC methods described in section II. As a first step, from the drain current data at different temperatures and at high  $V_{GS}$  and  $V_{DS}$ ,  $R_{TH}$  of the JLNTs were estimated through (1) using the method M1. These values were then compared to theoretical  $R_{TH}$  values calculated considering the whole system of nanowires and the dielectric (essentially  $\text{SiO}_2$ ). The thermal resistance of  $\text{SiO}_2$ ,  $R_{\text{SiO}_2}$ , is considered in parallel with the thermal resistance of the nanowires,  $R_{NW}$ . Their equivalent resistance is then considered in series with the contribution of the PtSi layer for the device  $R_{TH}$ , written as

$$R_{TH,theo} = \frac{R_{NW} R_{\text{SiO}_2}}{R_{NW} + R_{\text{SiO}_2}} + R_{PtSi} \quad (11)$$

With,  $R_{NW} = \frac{4L}{\kappa_{NW} \pi D^2 NF^2}$ ,  $R_{PtSi} = \frac{1}{2\kappa_{PtSi} D \cdot NF}$  [33] and  $R_{\text{SiO}_2} = \frac{1}{2\kappa_{\text{SiO}_2} D \cdot NF \sqrt{(D_{ex}/D)^2 - 1}}$  [34]. Here,  $L$  is the total nanowire length and effective nanowire thermal conductivity values,  $\kappa_{NW}$ , were considered between 8 to 15  $\text{Wm}^{-1}\text{K}^{-1}$  for different diameters [27]. The thermal conductivities of PtSi,  $\kappa_{PtSi}$ , and  $\text{SiO}_2$ ,  $\kappa_{\text{SiO}_2}$ , are considered to be 30  $\text{Wm}^{-1}\text{K}^{-1}$  [35] and 1.4  $\text{Wm}^{-1}\text{K}^{-1}$  [36], respectively, and  $D_{ex}$  is the thermal exchange diameter, typically 100 nm. The first part of (11) signifies the nanowire contribution whereas the latter is due to PtSi contact.

A comparison between the extracted values of the  $R_{TH}$  using the M1 DC method with the theoretical calculations (Figs. 6 (a)-(b)), shows an overestimation by the experimental method especially in smaller geometries. This is likely because of the uncertainty in the measured  $I_D$  due to a loss of reproducibility as dimensions get smaller, thus leading to an underestimation of the slope of the  $I_D$ - $T$  plot.

Next, following the M2 DC method, a higher precision was observed when compared with theoretical values for both sets of devices with nanowire diameters of 22 and 34 nm (Figs. 6 (a)-(b)). Again, a higher uncertainty was observed for smaller geometries but the results are closer to theoretical predictions compared to the first method. The third DC method (M3) provided more reliable results and similar overall accuracy as M2 while showing higher precision for smaller geometries. This is probably because of the relative errors of the terms  $\Delta V_T/\Delta V_D$  and  $\Delta V_T/\Delta T$  compensating each other.

The fourth DC method (M4), described by eqs. (4) - (9), provided results of better accuracy compared to the first method but slightly higher values than the theoretical or M3 for smaller geometries (Figs. 6(a)-(b)), since it also involves estimating the slope of the  $I_D$ - $T$  curve which incorporates uncertainty in the measurements of  $I_{D0}$  that are crucial for accurate extraction.

Lastly, the internal device temperature rise, calculated using (2), is shown in Fig. 6(c) for all geometries as a function of dissipated power, indicating a significant temperature increase at high bias conditions (confirmed through multiphysics simulations in [27]) leading to possible device self-heating.

#### B. Thermal impedance extraction

The LF S-parameter measurements described in section II were leveraged to extract the thermal impedance of the JLNTs using (10). Keeping in mind that the accuracy of this method also depends on the accurate estimation of the slope  $dI_D/dT_A$  extracted from DC measurements as well as removing the pure electrical contribution of the output conductance ( $Y_{22}^{iso}$ ) from the S-parameter measurements, magnitude and phase of the thermal impedance were extracted as shown in Figs. 7 (a) and (b). The  $R_{TH}$  can be extracted from the magnitude of the  $Z_{TH}$  at low frequencies (0.1-10 kHz range) where dynamic self-heating is less predominant and static thermal response dominates. Hence, from the constant value of the magnitude of  $Z_{TH}$  in the 100-1000 Hz range (Fig. 7(a)), one can estimate the  $R_{TH}$  for each NW dimension. The extracted values are compared with the other extracted  $R_{TH}$  values from the previously described DC methods in Figs. 6(a)-(b) and Table I, highlighting that the values estimated using LF S-parameter method are in the same range as the DC methods.

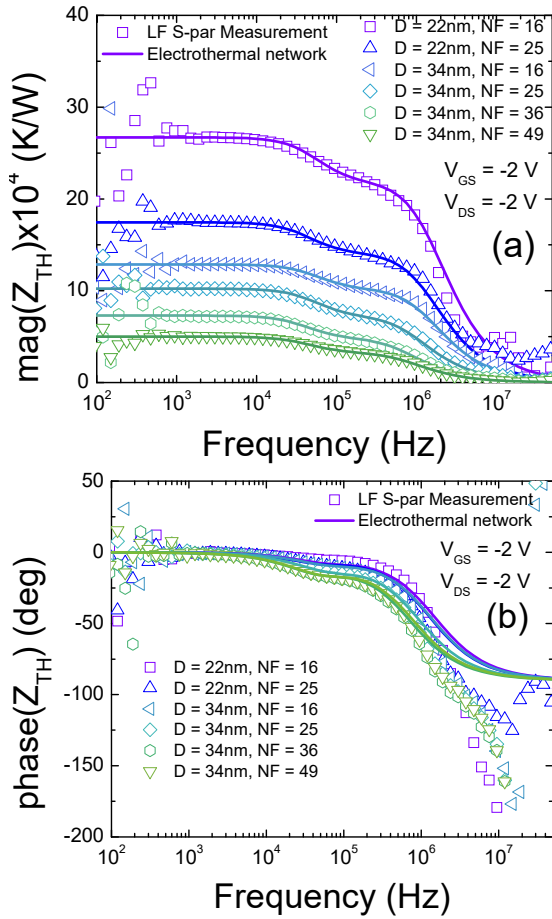


Fig. 7. (a) Magnitude and (b) Phase of the extracted thermal impedance ( $Z_{TH}$ ) of the JLNTs at  $V_{GS} = -2V$  and  $V_{DS} = -2V$  comparing measurement results and electrothermal network simulations.

TABLE I  
THERMAL RESISTANCE EXTRACTED USING DIFFERENT METHODS

Geometry		DC methods ( $K/W \times 10^4$ )				Theo. ( $K/W \times 10^4$ )	AC (LFS) method ( $K/W \times 10^4$ )	COMSOL ( $K/W \times 10^4$ )
D (nm)	NF	M1	M2	M3	M4			
22	16	21.3	23.1	22.2	18.5	25.9	17.5	22
22	25	19.8	15.6	16.5	14.8	16.5	-	12
34	16	11.7	7.4	11.4	6.6	11.96	10.2	11.2
34	25	7.75	5.1	7.2	4.8	7.7	7.5	7

### C. Equivalent electro-thermal network

What is further interesting is that from the extracted thermal impedance one can also estimate the elements of the entire thermal network of the vertical JLNTs that constitutes its heat-flow dynamics. To do so, one can represent the  $Z_{TH}$  of the device by an equivalent electro-thermal network consisting of resistive ( $R_{TH}$ ) and capacitive ( $C_{TH}$ ) elements using a modified Foster-like equivalent electro-thermal network [37], which is a representation of the device self-heating and is commonly used to recalculate the internal device temperature ( $T_J$ ). In a compact model implementation, this network is represented by a fictitious node and thermal effects are emulated through electrical parameters of the equivalent circuit. Drawing analogy with voltage and currents, in the thermal network, the dissipated power is represented as the equivalent of the node current whereas the node voltage gives the device internal temperature calculated using  $R_{TH}$  and  $C_{TH}$ . However, this implementation only considers a single pole for the frequency response of the

thermal network, which is often not sufficient in modern transistors due to distributed nature of the thermal elements. For example, in our measured LF S-parameters, we observed that the frequency-dependent behavior of the  $Z_{TH}$  can only be captured accurately by considering an equivalent two-pole electro-thermal network consisting of two resistive and two capacitive elements (Fig. 8).

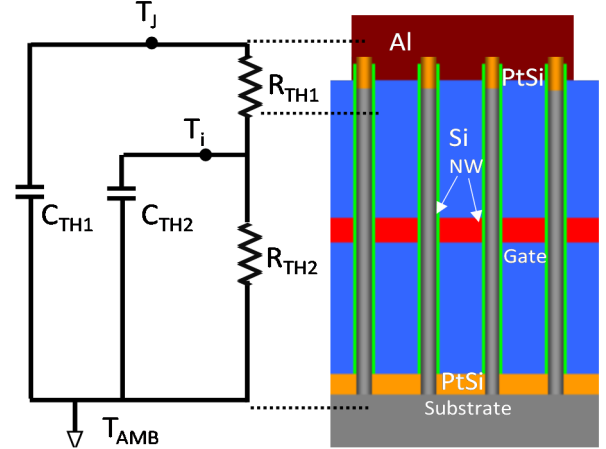


Fig. 8. Equivalent electrothermal R-C network of the vertical JLNT depicting contributions from the nanowires and PtSi contact regions.

Using the two-pole thermal network shown in Fig. 8, we can calculate the total device thermal impedance  $Z_{TH}$  as

$$Z_{TH} = (Z_{TH2} + R_{TH1}) / (1 + j\omega C_{TH1}(Z_{TH1} + R_{TH1})) \quad (12)$$

$$\text{With, } Z_{TH2} = R_{TH2} / (1 + j\omega C_{TH2}R_{TH2}).$$

Next, we simulated the magnitude and phase of the  $Z_{TH}$  using (12) and compared the results with the measurements shown in Fig. 7. Through model fitting we could then extract the parameters,  $R_{TH1}$ ,  $R_{TH2}$ ,  $C_{TH1}$  and  $C_{TH2}$ , of the equivalent thermal network which are shown in Table II and Fig. 9, with the total thermal resistance of the device given by  $R_{TH1} + R_{TH2}$ . The results indicate that larger geometries have lower thermal resistances, which is however compensated by the higher device current and dissipated power ( $P_{diss}$ ) under fixed bias conditions, possibly leading to a higher device temperature in larger devices [27]. Nonetheless, thermal conductivity of the nanowires improve in larger geometries that potentially contribute to a more efficient heat evacuation.

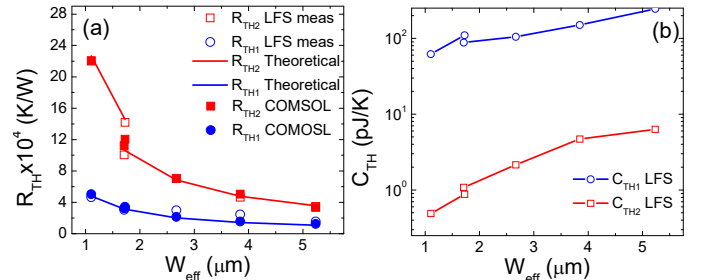


Fig. 9. Thermal (a) resistances and (b) capacitances of the electrothermal network as a function of the effective device width showing the two sets of contributions from the nanowire and PtSi regions, as extracted from LF S-parameters and COMSOL simulations in comparison with theoretical values.

To interpret the physical origin of the two sets of thermal resistances, we refer to the theoretical expression of (11) in which the first term refers to the thermal resistance of the nanowire ( $R_{TH2}$ ) whereas the second term is due to the contribution of the PtSi contact region ( $R_{TH1}$ ). Comparing these two theoretical contributions separately (table II and Fig. 9 (a))

with the extracted values of  $R_{TH1}$  and  $R_{TH2}$ , we could clearly see a strong correlation for all geometries, validating the proposed two-pole electrothermal network that originates from the contributions of the two regions of the JLNT. This is illustrated schematically in Fig. 8 with the Foster-like equivalent thermal network superimposed against different regions of the vertical device structure. To the best of our knowledge, this is the first report on the extraction of electro-thermal equivalent network in junctionless transistors. In the next section, numerical Multiphysics simulation results further corroborate the consistency of these results.

TABLE II  
EXTRACTED ELEMENTS OF THE ELECTRO-THERMAL NETWORK

Geometry		LFS method (K/W $\times 10^4$ )		Theoretical (K/W $\times 10^4$ )		COMSOL (K/W $\times 10^4$ )		LFS method (pJ/K)	
D (nm)	NF	$R_{TH1}$	$R_{TH2}$	$R_{TH1}$	$R_{TH2}$	$R_{TH1}$	$R_{TH2}$	$C_{TH1}$	$C_{TH2}$
22	16	4.65	22.1	4.73	22.6	5	22	62	0.49
22	25	3.25	14.2	3.03	14.5	3.4	12	110	0.88
34	16	3.05	10.1	3.06	10.6	3.2	11.2	88	1.08
34	25	2.99	7.02	1.96	6.8	2.1	7	105	2.15
34	36	2.45	4.65	1.36	4.7	1.4	4.5	150	4.7
34	49	1.55	3.48	1.02	3.5	1.1	3.3	245	6.3

#### D. Numerical Simulations

As a final validation of the thermal resistance extraction methods proposed in this work, numerical multiphysics simulation was performed using COMSOL software [26] by coupling the heat flow equation with drift diffusion transport based on a non-Fourier GKE formulation [27]. The complete vertical junctionless nanowire transistor structure was reconstructed virtually using COMSOL taking into account the material properties and device geometries as the fabricated transistors [24]. Additional details on the simulation methodology can be found in part-II of this work [27]. For thermal extraction, the JLNTs were biased at the same operating conditions as the measurements and the thermal resistances were then extracted from the calculated heat flux through the devices. The thermal resistances extracted using COMSOL simulations are then compared with the theoretical predictions and experimentally extracted values shown in Figs. 6 (a)-(b), depicting very good agreement, thus validating the experimental thermal resistance extraction methods proposed in this work. Moreover, from COMSOL simulations we have also extracted the thermal resistances  $R_{TH1}$  and  $R_{TH2}$  by separating the contributions using a cut-point at the interface between the nanowire and PtSi contact regions of the simulated structure. These values are also shown in table II and Fig. 9 (a) depicting a very good agreement with the experimental results, further affirming the accuracy of the multiphysics simulations.

#### IV. CONCLUSION

In this paper, we investigated novel experimental methods for studying electrothermal effects for the first time in GAA-JLNTs. We explored several different DC methods as well as low-frequency S-parameter measurements to extract thermal resistance and capacitances across several geometries of the JLNTs for the first time. Relative accuracy of each extraction

method is discussed and the extracted thermal parameters are compared with theoretical predictions as well as multiphysics COMSOL simulation, detailed in part II of this work [27], depicting good agreement. The threshold-voltage-based DC method (M3) provided highest accuracy for the extracted thermal resistance compared to theoretical values owing to higher resilience to experimental uncertainties, especially for small device dimensions. Elements of the equivalent thermal network are specifically extracted from LF S-parameter measurements for the understanding of dynamic electro-thermal behavior of the device. The experimental methods proposed in this work are not limited to JLNTs and can be extended for studying thermal transport other novel nanoscale device architectures. Our results indicate that JLNTs with larger diameters and higher number of nanowires in parallel have a higher efficiency for heat dissipation through the 3D vertical nanowires. In the future scope of this work, the elements of the thermal network will be integrated in the compact model for JLNT-based 3D logic circuit level exploration [38] and design-technology co-optimization (DTCO) [3], and will play an important part in redefining the semiconductor value chain spanning across device and system levels involving these emerging 3D vertical technologies.

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