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Nil Davy, Romain Hersent, Virginie Nodjiadjim, Marina Deng, Mukherjee Chhandak, et al.. 455/610-GHz fT/fMAX InP DHBT technology with demonstration of a beyond-110-GHz-bandwidth large-swing PAM-4 2:1 AMUX-driver. Compound Semiconductor Week (CSW), May 2023, Jeju Island (South Korea), South Korea. <hal-04296467>

HAL Id: hal-04296467

<https://hal.science/hal-04296467v1>

Submitted on 20 Nov 2023

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455/610-GHz f_T/f_{MAX} InP DHBT technology with demonstration of a beyond-110-GHz-bandwidth large-swing PAM-4 2:1 AMUX-driver

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Abstract—We report on an Indium Phosphide (InP) double heterojunction bipolar transistor (DHBT) technology for integrated circuit design and fabrication. The $0.4 \times 5 \mu\text{m}^2$ DHBT devices exhibit a 455-GHz f_T and a 610-GHz f_{MAX} , with a 4 V common-emitter breakdown voltage, the BV_{CE0} , and a peak current gain β of 25. This enabled state-of-the-art 2:1 Analog multiplexer (AMUX)-driver results with beyond-110-GHz bandwidth and 2-Vppd PAM-4 swing at 100 GBd.

Keywords—Double heterojunction bipolar transistor; Indium Phosphide; Analog multiplexer (AMUX); large-swing linear electro-optical modulator driver; 4-level pulse amplitude modulation (PAM-4), high-speed integrated circuit (IC)

I. INTRODUCTION

InP DHBTs have shown cut-off frequencies exceeding 1 THz with > 4 V breakdown voltages [1-2]. These devices can enhance the link capacity of high-frequency and large output-power front ends for 6G communications. However, optical communication front-end integrated circuits require several tens to thousands of transistors to be monolithically integrated, imposing very-high reproducibility and yield requirements along with the high-performance criteria. To this end, III-V Lab has developed a circuit-oriented InP-DHBT technology enabling state-of-the-art high-speed integrated circuits (IC) [3-4]. In this paper, we report on a 455-/610-GHz f_T/f_{MAX} 4 V BV_{CE0} InP-DHBT process, with up to several hundreds of DHBTs integrated per IC. Using this technology, we fabricated an AMUX-driver IC with record >2.1 -THz gain-bandwidth product and 2-Vppd PAM-4 output-swing at 100 GBd.

II. TRANSISTOR TECHNOLOGY

The DHBT structure is grown using solid source molecular beam epitaxy (SSMBE). The compositionally graded InGaAs base is 22-nm thick and highly C-doped ($> 8 \times 10^{19} \text{ cm}^{-3}$). The 110-nm thick composite collector includes InGaAs spacer, a thin InGaAsP layer, a highly doped InP doping plane, and a lightly doped InP layer. Transistors, as shown in Fig. 5, are fabricated using a wet-etched self-aligned triple mesa technology [5]. Various emitter lengths (from 3 to 10 μm) and widths (from 0.4 to 0.7 μm) are available; the overall fabrication yield on the 3-inch wafer is $>99\%$. The DC characteristics of a $0.4 \times 5 \mu\text{m}^2$ DHBT are shown in Fig. 1. The peak current gain is 25, the base and collector ideality factors are $\eta_B=1.83$ and $\eta_C=1.12$, respectively. This device exhibits a 4 V BV_{CE0} at a collector current density $J_C=0.01 \text{ mA}/\mu\text{m}^2$. Cut-off frequencies are extracted from on-wafer S-parameter measurements up to 110 GHz. Fig. 2 shows extracted f_T and f_{MAX} of a $0.4 \times 5 \mu\text{m}^2$ DHBT at various V_{CE} . The device exhibits peak f_T and f_{MAX} of 455 GHz and 610 GHz, respectively. In comparison, frequency performances of shorter devices are degraded by emitter resistance, while longer ones are affected by the base-collector capacitance, as illustrated in Fig. 3. Similarly, wider transistors feature lower performances as depicted on Fig. 4.

III. ULTRA-LARGE BANDWIDTH INP-DHBT ANALOG MULTIPLEXER-DRIVER INTEGRATED CIRCUIT

The 0.5 μm DHBTs were leveraged for the design and fabrication of a lumped AMUX-driver IC with state-of-the-art performances, as shown in Fig. 6. The circuit process features three Au-based metallization levels, SiN MIM capacitors and NiCr thin-film resistors. The AMUX-driver contains 76 DHBTs (5 and 7 μm emitter lengths). The 2:1 AMUX-driver operation, electro-magnetic (EM)-simulation and design details are described in [3-4]. As depicted on Fig. 7(a) the AMUX-driver shows a record >2.1 -THz gain-bandwidth product with a 19.6-dB (25.6-dB differential) $|S_{21}|$ at 0.1-GHz and >110 -GHz bandwidth. It also features ~ 11 -dB peaking gain around 100 GHz. A good agreement between measurement and simulation is also obtained. Besides, Fig. 7(b) depicts the AMUX-driver 2-Vppd output-swing 100-GSa/s 100-GBd PAM-4 differential output eye diagram with clear eye-opening.

Acknowledgement: This work was supported by the European Commission through the Photonics Public Private Partnership Initiatives under Grant H2020-ICT-2019-2 (Twilight Project).

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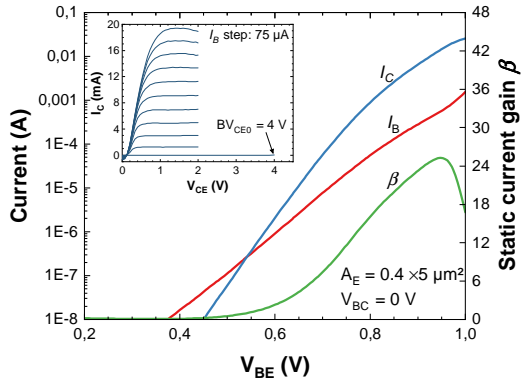


Fig. 1: Gummel plot of a $0.4 \times 5 \mu\text{m}^2$ InP DHBT at $V_{CB} = 0 \text{ V}$ and (inset) corresponding I_C - V_{CE} curves.

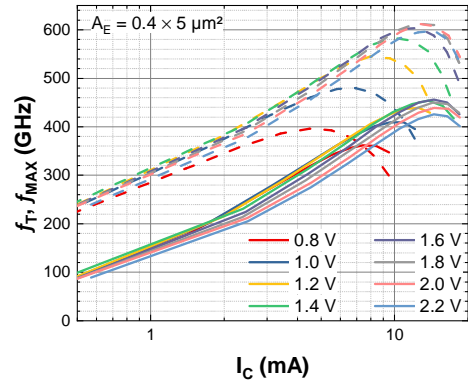


Fig. 2: f_T (solid lines) and f_{MAX} (dashed lines) as function of I_C for different V_{CE} .

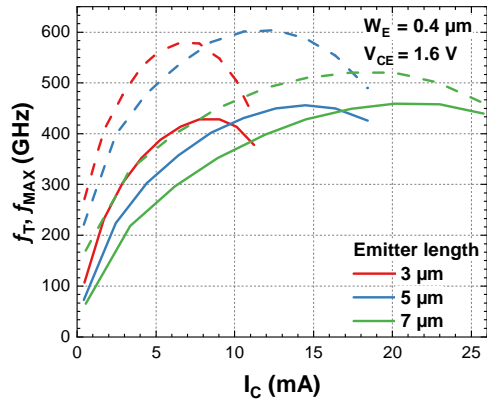


Fig. 3: f_T (solid lines) and f_{MAX} (dashed lines) as function of I_C for various emitter lengths



Fig. 4: f_T (solid lines) and f_{MAX} (dashed lines) as function of I_C for various emitter widths at $V_{CE} = 1.6 \text{ V}$

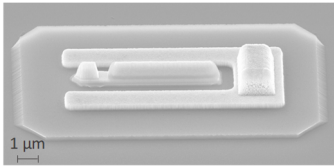
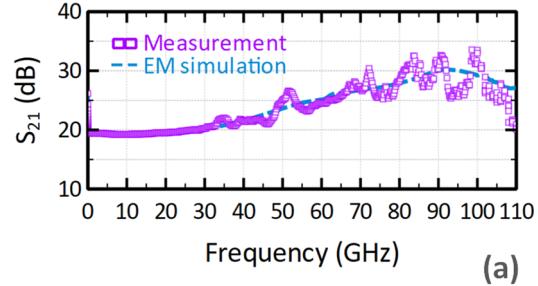


Fig. 5: $0.4 \times 5 \mu\text{m}^2$ InP DHBT microphotograph.



(a)

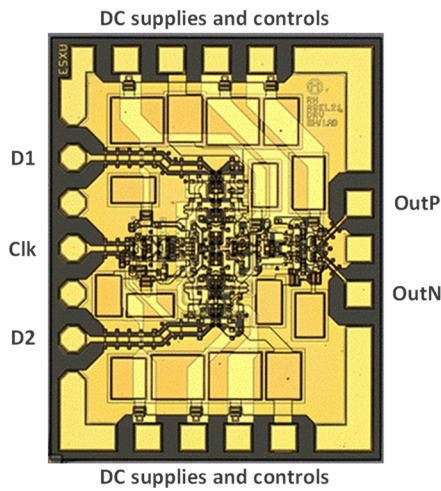


Fig. 6: InP-DHBT AMUX-driver die microphotograph. The chip sizes $1.2 \times 1.5 \text{ mm}^2$. Data/Clock input and output ports are respectively located on the west and east sides of the die. DC supplies and controls are located on the north and south sides.



(b)

Fig. 7: InP-DHBT AMUX-driver (a) measured versus simulated path-through-mode single-ended S_{21} (b) 100-GSa/s 100-GBd (200-Gb/s) PAM-4 differential output eye diagram. Horizontal and vertical scales are 5 ps/div and 600 mV/div, respectively.