



Hybrid Radiation Hardening Approach: a RISC-V System-on-Chip case study

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Facilities:

- Chiplr - ISIS Facility, Rutherford Appleton Laboratory, United Kingdom
- CNA - University of Seville, Junta de Andalucía, CSIC, Spain
- CHARM - European Organization for Nuclear Research (CERN), Switzerland
- PARTREC - University of Groningen, Netherlands

Outline

Background

Proposed Strategy

Hardware and software

Experimental Results

Test campaigns (Chiplr, PARTREC, CNA, CHARM)

Conclusion

Background

Background

Context / Statement

- COTS (Commercial Off-The-Shelf) components are rapidly reaching dependable systems in space applications

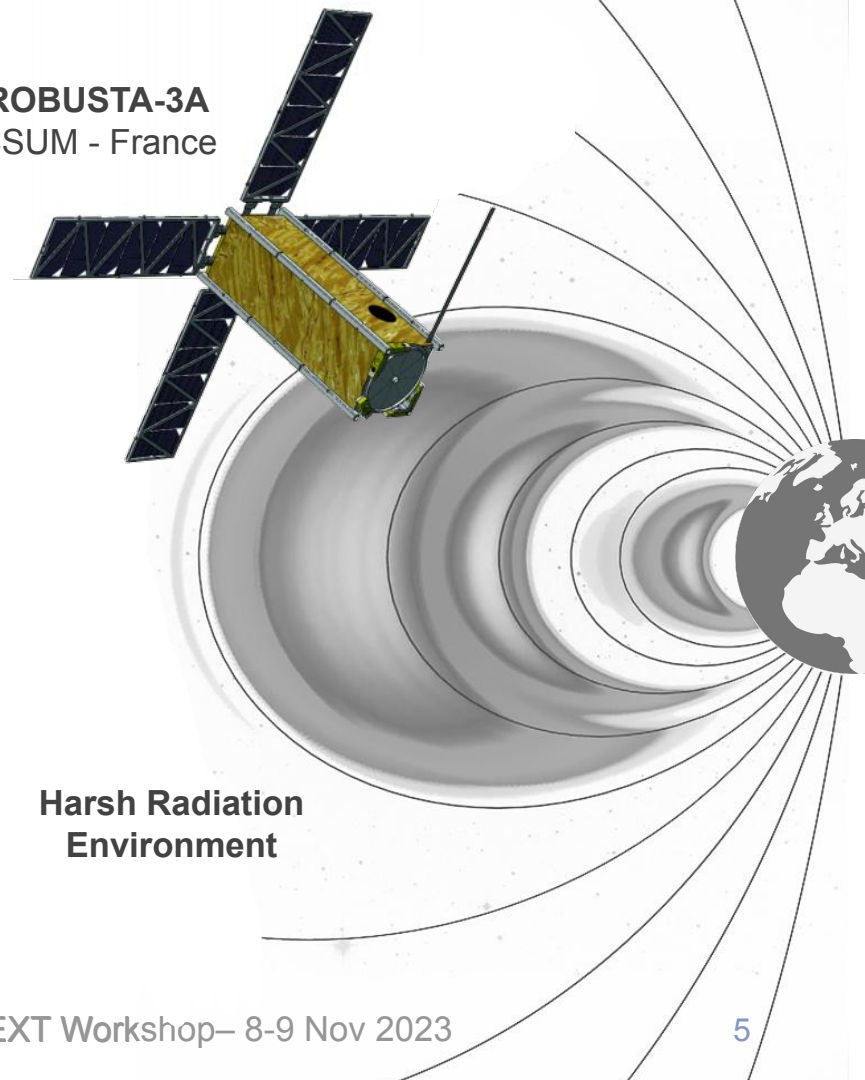
Motivation

- Demand for high-performance, feature-rich, flexible, and cheaper processing units for attending complex application demands

Challenges

- Radiation Effects (**SEE**, TID, and DD)

ROBUSTA-3A
CSUM - France



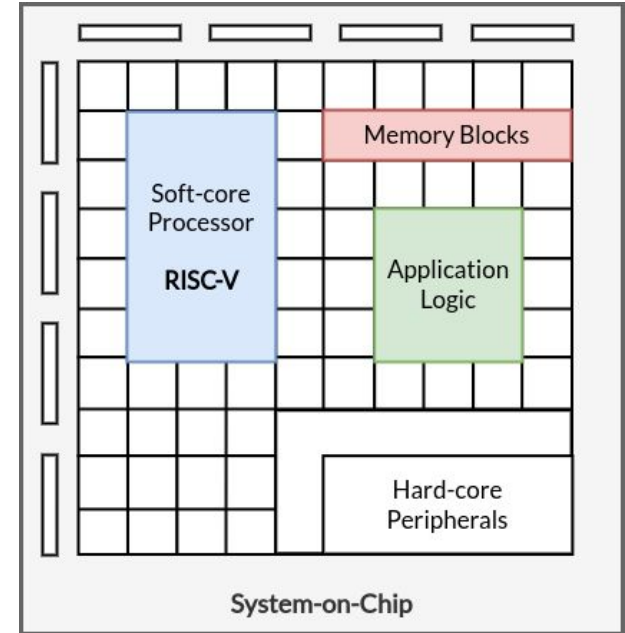
Background

Single-Event Effects on System-on-Chip (SoC)

- System and code memories upsets
- System registers upsets
- Communication bus corruption
- Timeouts, loops, hangs

Solution under investigation

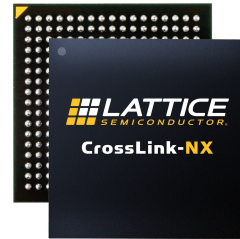
- RISC-V SoC based on a COTS FPGA
 - Hardening techniques (exploiting redundancies)
 - Reconfigurable and modular design
 - Radiation testing



Background

FPGAs are not built the same!

- Configuration Memory (CMEM) can be highly sensitive (dominate error rates)
- COTS drawbacks apply for these devices (lot variability, latch-up, packaging, ...)



	Xilinx's Zynq-7000	Lattice's CrossLink-Nexus	Microchip's PolarFire
Main radiation concerns	SEL, SEU, SEFI *CMEM (built-in mitigation)	SEU, SEFI *CMEM (built-in mitigation)	SEU, SEFI
Technology	SRAM-based	SRAM-based	SONOS-based
Process	TSMC's 28HPL (28 nm)	Samsung's FD-SOI (28 nm)	UMC's (28 nm)

Proposed Strategy

Proposed Strategy

A hybrid hardening approach [1,2]

Hardware: Fault-tolerant RISC-V System-on-Chip

- Soft-core SoC entirely developed by the group (UM)
- Reliable SoC with enhanced fault observability
- Combination of Triple Modular Redundancy (TMR) and Error Correcting Code (ECC) for most critical structures

Software: Application-independent recovery strategy

- **Periodic context saving:** save important registers, memory, and pointers
- **Context Restoration:** triggered by the added observability at hardware covering the full SoC



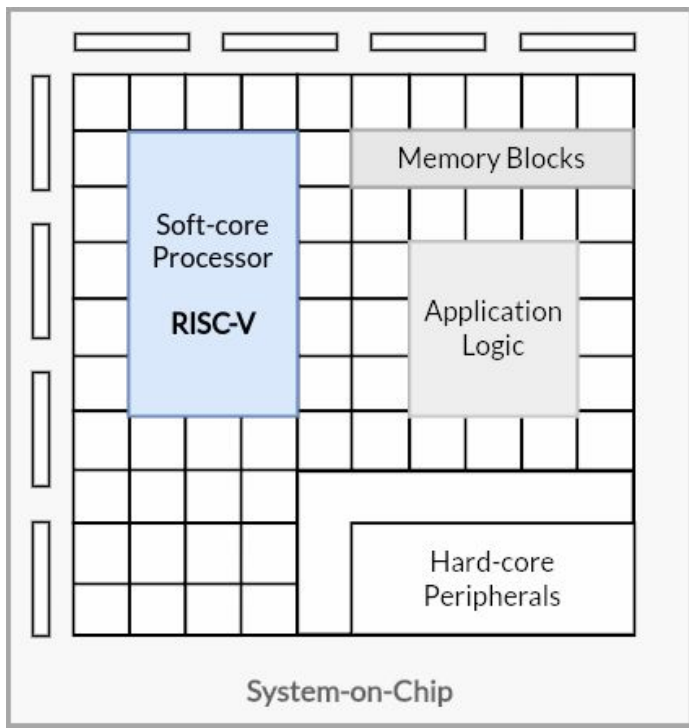
[1] D. A. Santos, et. al., “Enhancing Fault Awareness and Reliability of a Fault-Tolerant RISC-V System-on-Chip”, Electronics 2023, 12, 2557.



[2] P. M. Aviles, et. al., “Radiation Testing of a Multiprocessor Macrosynchronized Lockstep Architecture With FreeRTOS”, TNS, vol. 69, no. 3, pp. 462–469, 2022.

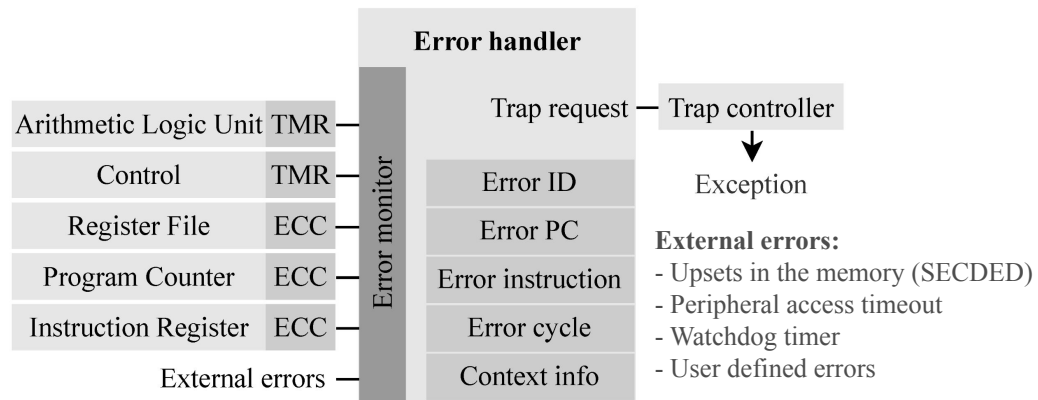


Proposed Strategy: Hardware

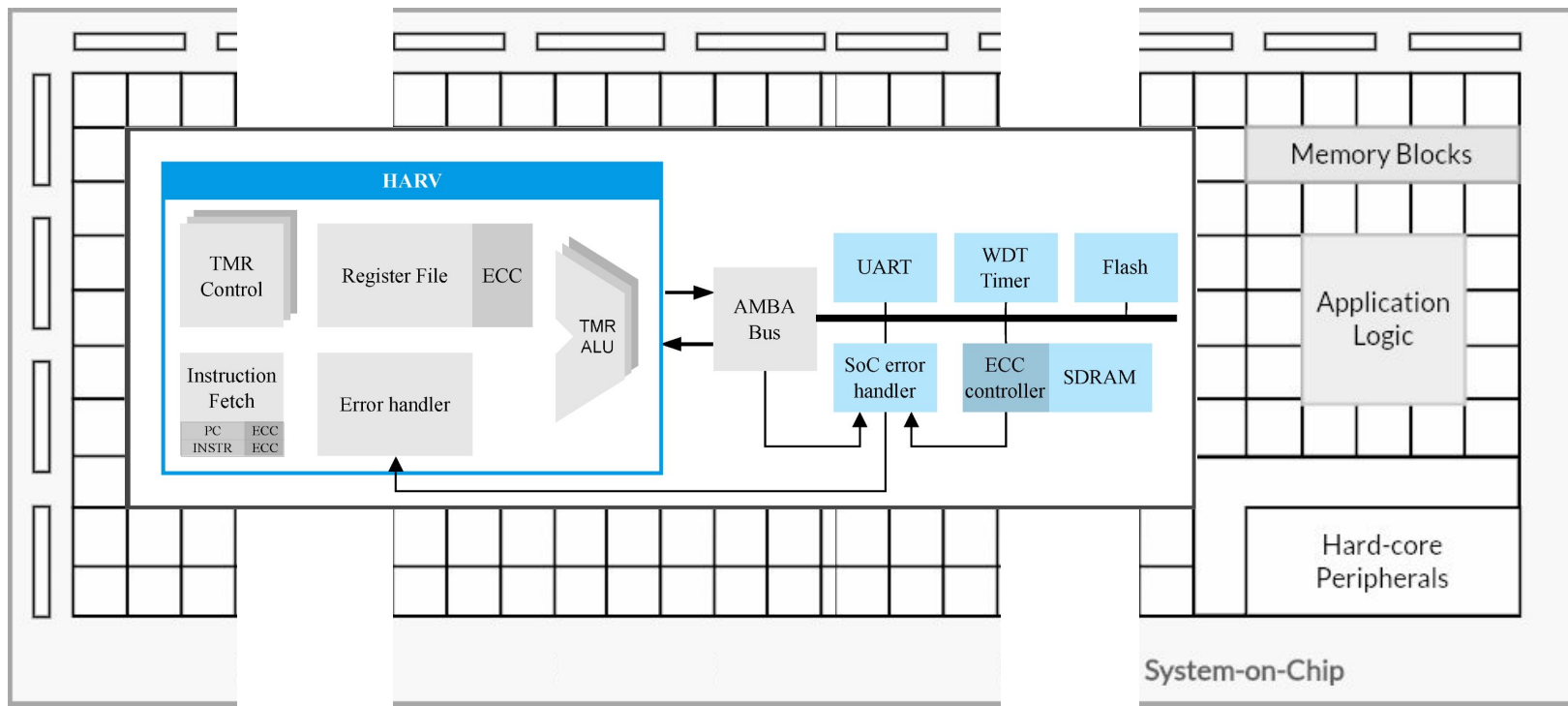


Fault-tolerant RISC-V System-on-Chip

- Enhanced single-core processor with embedded observation of the hardened structures of the full SoC
- Provides detailed information about the processor context and external errors



Proposed Strategy: Hardware



Proposed Strategy: Software

Enable the system or application to recovery to a previous error-free state

Consists of three operations

- Context saving: **Checkpoint** performs the processor context saving in **safe memory**
- Context Restoration: **Rollback** restores the processor context to a **previous state**
- System hard reset (last resource) is triggered due to abnormal behavior or hangs

Reference implementation

- Macrosynchronized Lockstep Architecture (MSLS) [2]
 - Synchronizes **two** ARM processor **cores**
 - Enables error detection with a **loosely-coupled lockstep** architecture

This implementation

- Only a single core required! (fault awareness triggers recovery, not cores mismatch)

Proposed Strategy: Software

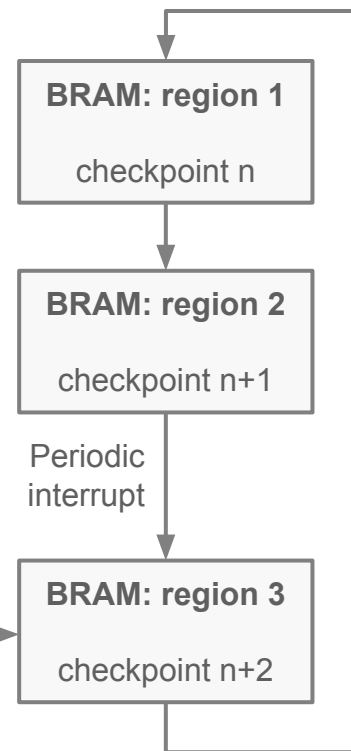
Checkpoint

- Implemented in software through a periodic interrupt
- Context of the application is transferred to a safe memory
 - Includes register file and the local variables of the application
- Saved in BRAM memory blocks with SECDED protection
 - Includes an extra error detection code (CRC32)

Error handling

- Performed using an exception service routine
- Based on the severity of the error for the execution:
 - Report error and continue execution
 - Correct upset at hardware
 - Rollback to a previous checkpoint
 - Reset SoC and reconfigure FPGA

Rollback pointer →
> to the last checkpoint available





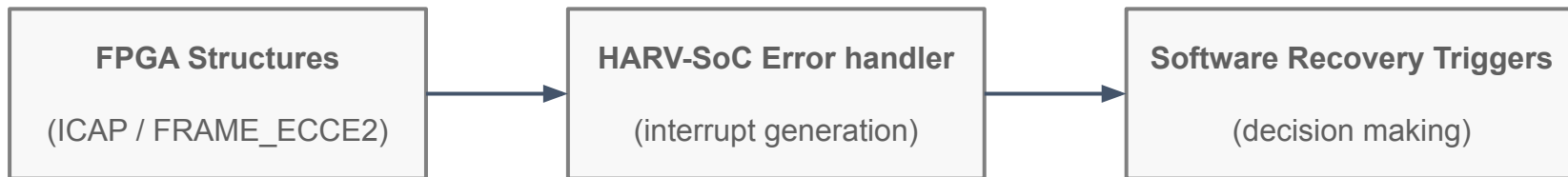
Proposed Strategy: Software

For SRAM-based FPGA designs

- Main concern: Configuration Memory (CMEM) upsets

Proposed solution (valid for Xilinx FPGAs)

- We implemented an interface to the built-in scrubber in the CMEM (Xilinx FRAME_ECCE2 buffer, not SEM IP!)
- This custom solution allows a low-cost and transparent interface for CMEM reporting

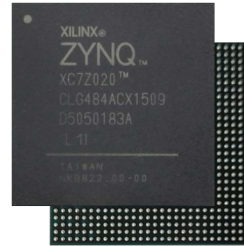


Experimental Results

Experimental Results

On going work!

- Some results from the proposed strategy (most relevant, not a deep dive)



	Xilinx's Zynq-7000 SRAM-based (28 nm)	Microchip's SmartFusion2 Flash-based (65 nm)	
Test campaign #1 (Software strategy)	CNA (protons) [2]	-	UC3M
Test campaign #2 (Hardware)	-	Chiplr (atmospheric neutrons) [1,3]	UM
Test campaign #3 (Hardware)	-	PARTREC (high-energy protons) [4]	UM
Test campaign #4 (Hardware)	-	CHARM (mixed-field environment) [1]	UM
Test campaign #5 (Hardware + Software)	Chiplr (atmospheric neutrons) [5]	-	UM + UC3M

Experimental Results: Test Campaign #1

Objectives

- Evaluate the software recovery strategy (using a two-core loosely-coupled lockstep)
- Comparison between baremetal and Operating System (OS) versions

Outcomes

- Software strategy highly effective to detect errors and significant for correction
- Technique more effective to baremetal applications

Software strategy detection and correction evaluation: baremetal vs OS

Category		Mmult	
		Baremetal	OS
Errors	Undetected errors	2 (0.7%)	5 (2%)
	Detected errors	273 (99.3%)	248 (98%)
	Total errors	275 (100.0%)	253 (100.0%)
Detected errors	Corrected errors	142 (52%)	65 (26.2%)
	WDT	64 (23.4%)	118 (47.6%)
	SW Reset	67 (24.6%)	65 (26.2%)

CNA

[2] P. M. Aviles et. al., “Radiation Testing of a Multiprocessor Macrosynchronized Lockstep Architecture With FreeRTOS”, TNS, vol. 69, no. 3, pp. 462–469, 2022.



Experimental Results: Test Campaign #2

Objectives

- Evaluate the applied fault tolerant techniques
- Evaluate the impact in an application

Outcomes

- Hardware strategies highly effective to improve reliability (detect and correct)
- However:
 - Limited observability
 - Lack of “time to failure” type of analysis

Hardware strategy correction evaluation: impact on the test benchmark

Hardening configuration	Correct	Error	Timeout
None	75.80%	0.64%	23.57%
Processor	73.19%	0.00%	26.81%
Memory	97.59%	0.00%	2.41%
Memory&Processor	97.73%	0.00%	2.27%

Chiplr

[3] D. A. Santos et al., "Neutron Irradiation Testing and Analysis of a Fault-Tolerant RISC-V System-on-Chip," DFT, 2022, pp. 1-6.



Experimental Results: Test Campaign #3

Objectives

- Evaluate the hardware reliability for space applications
- Better understand fault propagation

[4] [accepted, not published yet] D. A. Santos et. al., “Characterization of a Fault-Tolerant RISC-V System-on-Chip for Space Environments”, DFTS, 2023.

Outcomes

- More robust analysis, including: MFTF, TID and benchmarks impact

Hardware strategy correction and fault propagation analysis

Configuration	HFTE Type	#HFTE ¹	#Propagated HFTEs ¹	HFTE Propagation XS ¹ [cm ² /device]
Baseline	Memory single-bit upset	21	0	-
	Register file single-bit upset	6	1	6.99×10^{-13}
	Timeout load access fault	6	4	2.80×10^{-12}
Hardened	Memory single-bit upset	23	0	-
	Register file single-bit upset	11	0	-
	Timeout load access fault	3	1	6.28×10^{-13}
	Memory double-bit upset	2	0	-
	Program counter single-bit upset	1	0	-
	Instruction register double-bit upset	1	0	-
	Program counter double-bit upset	1	0	-
	Load access fault	1	0	-

PARTREC

Experimental Results: Test Campaign #4

Objectives

- Evaluate the hardware reliability and fault awareness

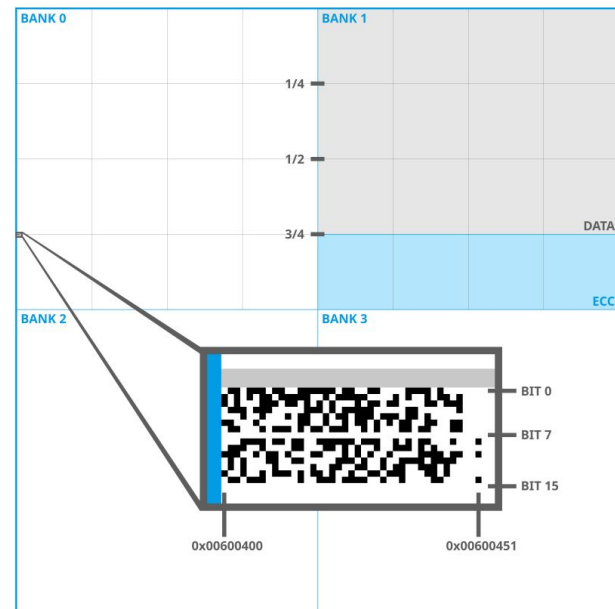
Outcomes

- Enhanced observation in reported errors

CHARM

Hardware observability analysis

Error	#Errors	Percentage	HEH XS [cm ² /device]
Memory single-bit upset	71	52.21%	7.38×10^{-11}
Memory double-bit upset	35	25.74%	3.64×10^{-11}
Register file single-bit upset	21	15.44%	2.18×10^{-11}
Load access fault	6	4.41%	6.24×10^{-12}
Store access fault	2	1.47%	2.08×10^{-12}
Program counter double-bit upset	1	0.74%	1.04×10^{-12}



[1] D. A. Santos, et. al., “Enhancing Fault Awareness and Reliability of a Fault-Tolerant RISC-V System-on-Chip”, Electronics 2023, 12, 2557.



Experimental Results: Test Campaign #5

Objectives

- Evaluate the proposed hardware + software strategy

Outcomes

- Capabilities of the software recovery on top of the added hardware observability
- Missing more evaluation scenarios for reporting the combined reliability improvement

Software recovery effectiveness

Recovery attempts	Occurrence
Effective at 1st rollback	44.51 %
Effective at 2nd rollback	0.58 %
Effective at 3rd rollback	0.00 %
Failed at 1st attempt	23.70 %
Failed at 2nd attempt	9.83 %
Failed at 3rd attempt	12.14 %
Failed before checkpoint	9.25 %
Total effectives	45.09 %
Total failures	54.91 %

Future work!

ChipIrr

[1] [accepted, not published yet] D. A. Santos, et. al., “Hybrid Hardening Approach for a Fault-Tolerant RISC-V System-on-Chip”, RADECS, 2023.

Conclusion

Conclusion

Successful test of a complex system and recovery strategies in different facilities

- Use of COTS FPGA for the deployment and validation of reliable processing units
- Evaluate different devices with distinct sensitivities for a radiation testing
- Comparison of irradiation campaigns results for different facilities/particles

Development and characterization of a robust, flexible, and low-cost SoC for space applications based on readily available technologies (COTS FPGAs) and an open processor architecture (RISC-V)

Proposition of guidelines for SoC testing with enhanced observability



RADNEXT

Thanks for your attention!

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Experimental Results: Other Outcomes

Preliminary device failure comparison between the SoC in different FPGAs

¹ For the SRAM-based FPGA, the custom integration with the built-in scrubber was used

² Failure: assumed when power cycle was required to restore functional state

³ ChipIrr: atmospheric neutrons



	Xilinx's Zynq-7000 ¹ SRAM-based (28 nm)	Microchip's SmartFusion2 Flash-based (65 nm)
Total Fluence ³ [n/cm ²]	1.80×10^{12}	5.83×10^{10}
Mean Fluence to Failure ² [n/cm ²]	2.06×10^{10}	3.60×10^8
Cross Section [cm ²]	4.98×10^{-11}	2.78×10^{-9}

~ 200x difference in robustness!