Three-phase bidirectional active split source inverter for automotive traction application

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Three-Phase Bidirectional Active Split Source Inverter for Automotive Traction Applications

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Abstract

The Split Source Inverter (SSI) is an attractive single-stage boost DC-AC converter topology. It requires fewer components than the Z-source inverter to achieve the boost function and also maintains a continuous input current. However, a significant drawback of this topology is its limited DC-bus voltage utilization. This paper introduces a new inverter topology derived from the SSI, aimed at addressing the DC voltage utilization issue and assessing its viability for traction applications. The new three-phase single-stage boost DC-AC inverter topology is named B-ASSI, and a potential modulation scheme is proposed to accompany it. To verify their functionality, the proposed converter and modulation scheme are simulated using Matlab/Simulink. Furthermore, a Proof of Concept (POC) is executed to experimentally validate the performance of the proposed inverter topology

Keywords: DC - AC converter, Voltage source inverter (VSI), single-stage inverter, Z-source inverter (ZSI), Split Source inverter (SSI)

1. Introduction

In automotive applications, a common approach involves a two-stage configuration comprising a DC-DC Boost converter followed by a DC-AC two-level voltage source inverter (VSI) conversion stage. The purpose of the DC/DC Boost stage is to maintain a constant and higher voltage on the DC-bus. However, the introduction of an extra conversion stage in this configuration leads to a reduction in the overall efficiency of the powertrain. Over the last decade, there have been advancements in single-stage topologies that offer a promising solution. These single-stage topologies can achieve the boosting function of the DC-DC stage without significantly compromising the overall efficiency of the system. The Z-source inverter [1] and the quasi-Z-source inverter [2] are both examples of single-stage boosting topologies. A comprehensive review of impedance source inverter topologies, their modulation techniques, and their application in traction systems can be found in references [3, 4, 5]. The main drawback of these topologies is the need for bulky and voluminous passive components. While space is limited in an embedded environment, some research has explored the integration of these topologies in electrical automotive traction applications and compared them with the traditional DC-DC Boost + VSI configuration [6]. However, the high cost and control complexity associated with these

impedance source inverters are still preventing their widespread adoption in automotive applications. The Split source inverter (SSI) was initially introduced as a single-phase topology for grid-connected photovoltaic application in [7]. Later, a three-phase version of this topology was proposed in [8] and illustrated in Fig. 1, making it a promising candidate for renewable energy applications [9]. The SSI has emerged as a competitive alternative, offering distinct advantages over other topologies. Unlike the traditional Z-source inverter, the SSI achieves the elevation of the DC-bus voltage using just one inductor and three input diodes. In contrast, the Z-source inverter (ZSI) requires 2 inductors and 2 capacitors for the same purpose. The main advantages of the SSI, as highlighted in [8], can be summarized as follows :

1. A continuous input current.
2. Lower voltage stresses for higher boosting factors.
3. A lesser component count compared to the ZSI.
4. Same switching states as the Voltage Source Inverter (VSI).

And the main drawbacks are :

1. Dead-times are still required.
2. Higher current stress is imposed on the switches for higher boosting factors.
3. Unequal distribution of current stress among the switches.

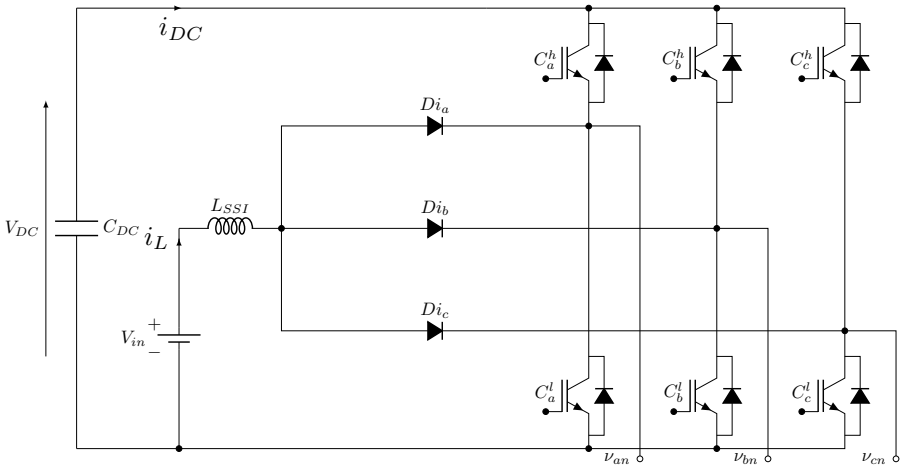


Figure 1: Three-phase Split source inverter. From [8].

Many studies have been conducted to improve the SSI topology. In [10], the authors propose an alternative connection of the source to the positive side of the DC-bus using common-cathode diodes to reduce the converter's size. Another approach is presented in [11], where the diodes are replaced with switches operating in synchronous rectification mode. This modification enables bidirectional power flow in the topology. In [12] and [13], an alternative configuration for the SSI is proposed. The idea is to add a switch to an inverter leg to achieve the same effect and effectively reduce the component count of the SSI. However, this modification results in an unequal current distribution among the switches and introduces limiting factors when extending this topology to a three-phase version. Furthermore, other variations of the Split Source Inverter

have been proposed for three-level topologies [14, 15] by using the diode-clamped or flying capacitor configuration. Another multilevel operation of the SSI has also been proposed in [16] or in [17] with a cascaded operation of SSI. However, the adoption of multilevel topologies for automotive applications is still limited due to the higher volume requirements of passive elements. The authors in [18, 19] investigate the common mode voltage generated in the SSI and propose a new modulation scheme to address this issue. One of the key aspect of the SSI is that the obtained boost factor depends on the modulation. In [20], a modulation scheme has then been adopted as a way of decoupling the boost factor of the DC side from the AC side and controlling each independently. All of the proposed topologies suffer from a low DC bus voltage utilization ratio. Researchers have thus proposed alternative configurations of the DC side with additional coupled inductors or other high gain boost cells to increase the boost factor [21, 22, 23, 24, 25]. However, increasing the boost factors exacerbates the DC bus utilization ratio problem and results in higher cost due to higher voltage stresses on the switches. The authors in [26] propose a comprehensive analysis of this inherent limitation and present a topology called the Active Split Source inverter to solve the problem. Nevertheless, this topology has only been proposed for single-phase photovoltaic applications. More recently, alternative configurations have emerged, such as Multi-outputs Split source inverters [27] or multi-inputs [28], which are good candidates for interfacing multiple voltage sources. Very few studies have been conducted on the adoption of the SSI for Electric Vehicles (EV) traction applications. The authors in [29, 30] proposed the adoption of the SSI with a nine-switch inverter for 6 phase induction motors. The multiphase version of the SSI studied in [31] could be interesting due to the numerous advantages that multiphase machines provide for traction applications. However, in both studies, the modulation index is kept constant. In electric automotive traction applications, the modulation index depends on the electrical motor's operating conditions (Torque and Speed). Furthermore, the topologies in the literature often propose to keep the usage of the input diodes of the classical SSI, which renders the architectures unidirectional in power flow. That is not applicable in traction application where regenerative breaking is needed. This paper proposes a novel three-phase inverter based on the Active Split Source inverter (ASSI) presented in Fig. 2 to solve the low DC bus voltage utilization ratio. The proposed converter has bidirectional capabilities and will be called Bidirectional Active Split Source Inverter (B-ASSI). A possible modulation scheme for the proposed converter is also presented, ensuring compatibility with electric automotive applications.

This paper is structured as follows : In Section 2, the limitatiosn of the SSI for automotive applications will be presented. Section 3 introduces the proposed converter and its operation, along with a possible modulation scheme. Finally, Section 4 and 5 present the simulation and experimental results, respectively.

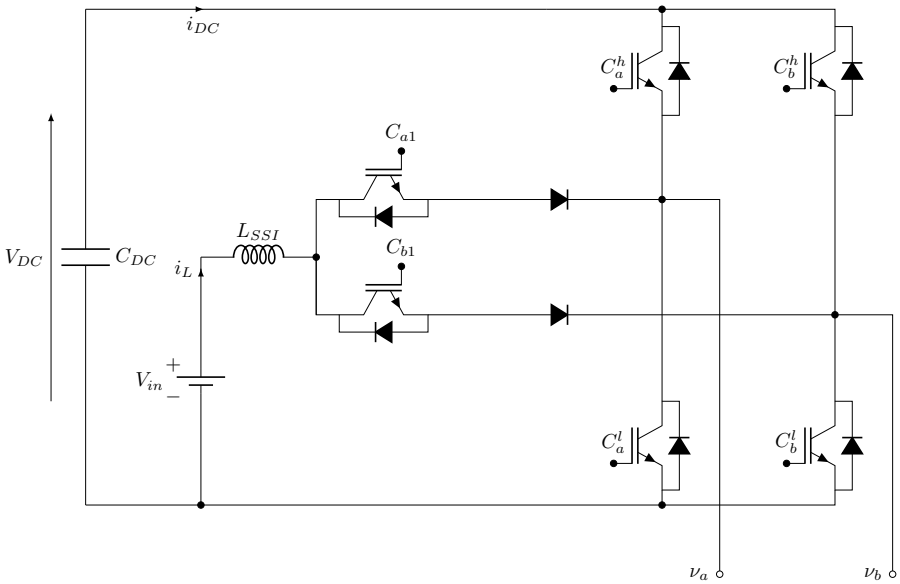


Figure 2: Existing single-phase Active Split source inverter (ASSI) presented in [26].

2. SSI analysis and its limitation

2.1. SSI analysis and modulation

The SSI (Fig. 1) shares the same states as the two-level inverter, namely six active states and two zero-sequence states, as enumerated in Tab. 1. During any of the active states, as well as during the zero-sequence state V_{000}, one of the diodes will be conducting and connects the inductor to the negative pole of the DC bus. Thus, the inductor will be charging. On the other hand, during the zero-sequence state vector V_{111}, the inductor will only discharge (and charge the DC bus capacitor) for the duration T_{111}.

Table 1: States of the Split Source Inverter.

	Switches States			Diodes States			
Vector	S_a^h	S_b^h	S_c^h	D_{ia}	D_{ib}	D_{ic}	Inductor State
V_{000}	OFF	OFF	OFF	ON	ON	ON	Charge
V_{100}	ON	OFF	OFF	OFF	ON	ON	Charge
V_{110}	ON	ON	OFF	OFF	OFF	ON	Charge
V_{010}	OFF	ON	OFF	ON	OFF	ON	Charge
V_{011}	OFF	ON	ON	ON	OFF	OFF	Charge
V_{001}	OFF	OFF	ON	ON	ON	OFF	Charge
V_{111}	ON	ON	ON	ON	ON	ON	Discharge

The Split Source inverter can be described as a boost converter with an equivalent duty cycle that represents the time during which the inductor is in the charging state. This duty cycle M_{DC} is expressed by (1) :

$$M_{DC} = 1 - \frac{T_{111}}{T_{PWM}} \tag{1}$$

Where T_{PWM} is the duration of one PWM cycle, and T_{111} is the duration of the zero-sequence state V_{111}. This duration T_{111} is mirrored by the lower envelope of the three-phase duty cycles of the inverter legs.

The static characteristics of the classical SSI can be obtained from the charge and discharge states of the inductor. With i_L as the input current and V_{DC} as the DC bus voltage being the state-space variables, the SSI can be modeled by equation (2) during T_{111}. This corresponds to the state of inductor discharge where the diodesare conducting and the DC bus is connected to the input voltage.

For $0 \leq t \leq (1 - M_{DC})T_{PWM}$

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in} - V_{DC} - r_L i_L}{L_{SSI}} \\ \dfrac{dV_{DC}}{dt} = \dfrac{i_L}{C} \end{cases} \tag{2}$$

Where V_{DC} is the voltage across the DC bus capacitor, V_{in} is the input voltage from the source. The current i_L représents the current circulating through L_{SSI} as depicted in Fig. 1. The duty cycle M_{DC} is defined by the level of the lower envelope relative to 1 (see Fig. 3). Then, for all other states where at least one diode is conducing, this corresponds to the state of inductor charging. Thus, for $(1 - M_{DC})T_{PWM} \leq t \leq T_{PWM}$, the model can be described by equation (3).

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in} - r_L i_L}{L_{SSI}} \\ \dfrac{dV_{DC}}{dt} = \dfrac{-i_{load}}{C} \end{cases} \tag{3}$$

Where i_{load} is the current absorbed by the motor. It is defined in equation (4), which is the same as the one in a two-level inverter.

$$i_{load} = C_a^h \cdot i_a + C_b^h \cdot i_b + C_c^h \cdot i_c \tag{4}$$

It can be noticed in (3) that during the state V_{111}, the current $i_{load} = 0$ and is removed from the term dV_{DC}/dt. The following equation (5) describes the averaged state-space model of the SSI.

$$\begin{bmatrix} \dfrac{di_L}{dt} \\ \dfrac{dV_{DC}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_{SSI}} & -\frac{1-M_{DC}}{L_{SSI}} \\ \frac{1-M_{DC}}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_{DC} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{SSI}} & 0 \\ 0 & -\frac{M_{DC}}{C} \end{bmatrix} \begin{bmatrix} V_{in} \\ i_{load} \end{bmatrix} \tag{5}$$

Thus, the SSI is mathematically described as a Boost converter. The static gain or elevation ratio can be defined by (6) :

$$\frac{V_{DC}}{V_{in}} = \frac{1}{1 - M_{DC}} \tag{6}$$

M_{DC} is linked with the duration of the zero-sequence state vector V_{111}, corresponding to the lower envelope of the duty cycles of the inverter legs in the case of classic PWM schemes based on the same triangle carrier. By using a Space Vector Pulse Width Modulation (SVPWM), the lower envelope is not constant. This will induce low-frequency ripple on the boost factor as well as on the inductor current and DC bus capacitor voltage, leading to increased requeirements in their

sizing. To maintain stable DC bus voltage, a modulation scheme called a Modified Sinusoidal Pulse Width Modulation (MSPWM) has been proposed for SSI [20]. This modulation scheme modifies the timing of the zero-sequence states and ensures a constant duration T_{111}. If the duration T_{111} is constant, the obtained elevation ratio from (6) is also constant. The resulting duty cycles are presented in Fig. 3. The inductor discharging time can then be controlled by adjusting the duty cycle biases. Thus, the authors in [20] proposed a control scheme to decouple the boost factor M_{DC} from the modulation index M_{ac} defined by (7).

$$M_{ac} = \frac{V_{ac}}{\frac{V_{DC}}{\sqrt{3}}} \tag{7}$$

V_{ac} being the output phase voltage of the inverter.

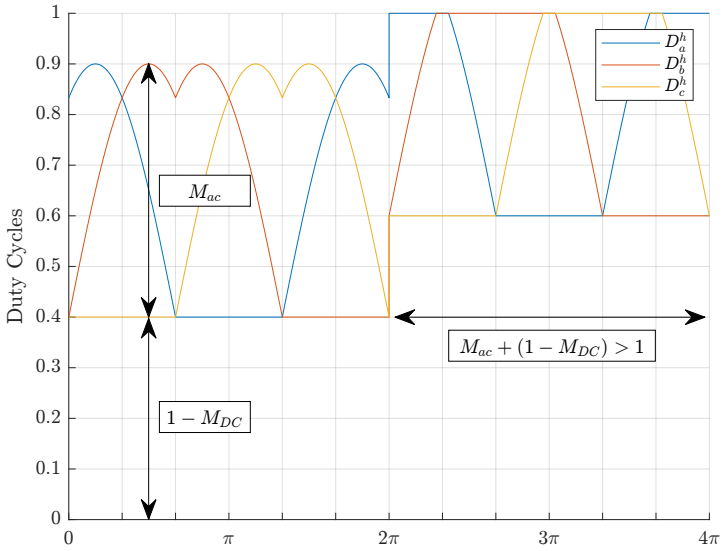


Figure 3: Duty cycles for a MSPWM and limits when $M_{ac} > M_{DC}$.

2.2. *Limitation of the SSI for traction applications*

The SSI and the associated MSPWM present numerous advantages. However, there is an inherent limitation that prevents the use of the SSI in automotive applications. This limitation is indicated by the implicit condition in the MSPWM, as stated in (8) and illustrated in Fig. 3.

$$M_{ac} \leq M_{DC} \tag{8}$$

It can be observed in Fig. 3 that if the modulation index is increased to a level above M_{DC}, the duty cycles will be saturated. In this scenario, the load cannot be controlled anymore. This constraint also affects the maximum AC output that can be obtained in steady-state, which can be expressed from (6),(7) and (8) :

$$V_{ac} \leq V_{DC} - V_{in} \tag{9}$$

As indicated by (9), with the use of a classical SSI, even with the implementation of MSPWM, the maximum output phase voltage V_{ac} remains bounded by the difference between the elevated

V_{DC} and the input voltage V_{in}. In [26], the authors state that to solve the DC link utilization ratio, increasing the boost factor or modifying the modulation alone cannot resolve this limitation. Consequently, a topological modification is required. Indeed, since the states of the passive diodes are imposed by M_{ac}, the system does not present the Degree of Freedom (DoF) to control the elevation ratio. One solution was to add switches to gain a new DoF, which is the case with the single-phase Active Split Source Inverter presented in Fig. 2.

The following sections present an inverter topology and its modulation to overcome this limitation in the three-phase inverter case and to drive the motor for its entire range of load operating conditions without losing control over the regulated DC link voltage.

3. B-ASSI : Analysis and modulation

3.1. Operation and model of the proposed topology

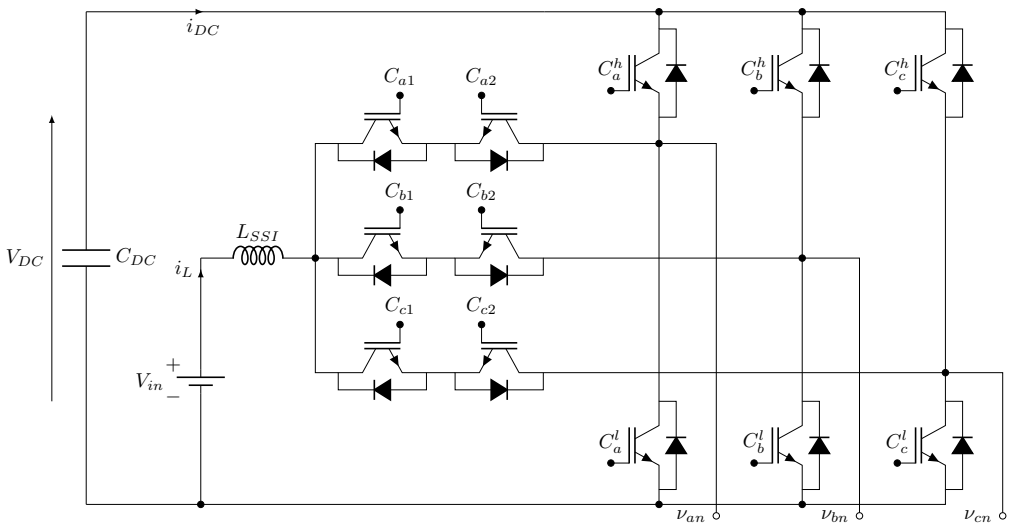


Figure 4: Proposed B-ASSI topology : Three-phase single-stage bidirectional Active Split Source Inverter.

The proposed B-ASSI is described in Fig. 4. This inverter uses two clamping switches connecting the input voltage source to each inverter leg middle point. The command of the first switches S_{a1}, S_{b1} and S_{c1} allows the control of the inductor current charging or discharging state during the actives states without influencing the voltage applied to the load. The second set of switches S_{a2}, S_{b2} and S_{c2} replaces the diodes in the ASSI to allow bidirectional power flow. Thus, there is a new degree of freedom in the control of inductor current charging or discharging time during the active state of the two-level inverter. This way, without impacting the load in any way, complete control over the inductor current as well as the DC bus voltage is achieved. All the states of the inverter topology used with the proposed modulation are depicted in Tab. 2. Where C_a^h, C_b^h, C_c^h are the command signals of the inverter leg switches S_a^h, S_b^h, S_c^h and C_{a1}, C_{b1}, C_{c1} are the command of the first set of clamping switches S_{a1}, S_{b1}, S_{c1}. Fig. 5 illustrates the degree of freedom in the choice of the inductor current state when an active state V_{100} is used on the inverter side. The original inductor charging state forced for classical SSI topologies depicted in

Fig. 5 (top) can be changed to an alternative inductor discharging state in Fig. 5 (bottom) for the proposed topology.

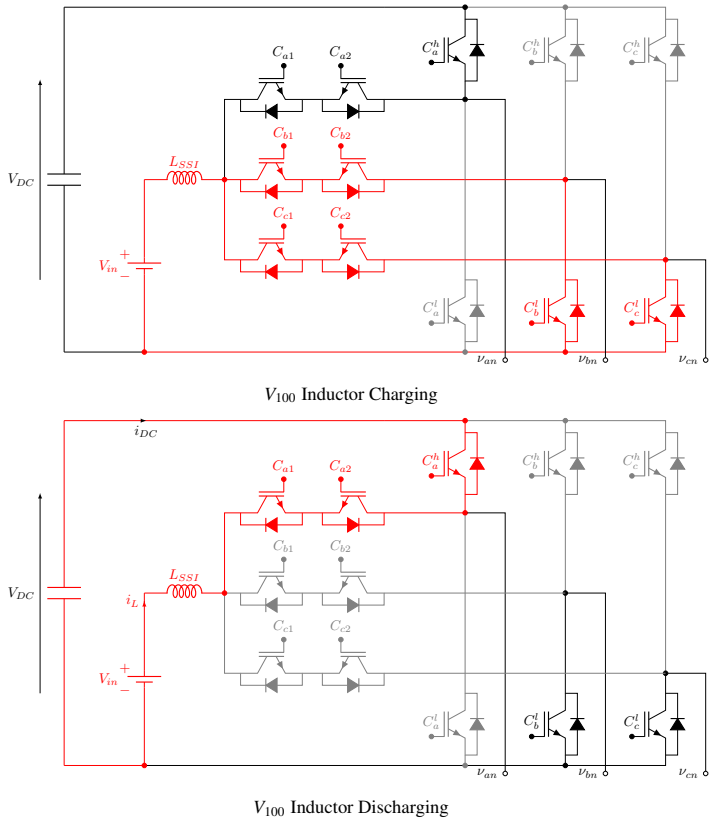


Figure 5: One possible active state for both Inductor Charging and Discharging state (impossible state for a classical SSI).

The converter can operate in two different modes. The first mode is called the non-saturated mode, in which the discharge of the inductor operates only during the zero state V_{111}. This means that, no discharge happens during any active state. The modulation used is the MSPWM described in Fig. 3. Now the second mode is accessible and is called the Saturated conduction mode. The Discharge of the inductor can happen in any active state, and the duration is chosen by the desired DC bus voltage level. Thus, the model of the B-ASSI in the non-saturated mode is the same as the model of the classical SSI and is described by (5).

The model in saturated mode for the discharge and charge of the inductor is described by (10) and (11) respectively.

For $0 \leq t \leq (1 - M_{DC})T_{PWM}$

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in} - V_{DC} - r_L i_L}{L_{SSI}} \\ \dfrac{dV_{DC}}{dt} = \dfrac{i_L - i_{load}}{C} \end{cases} \tag{10}$$

For $(1 - M_{DC})T_{PWM} \leq t \leq T_{PWM}$

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{V_{in} - r_L i_L}{L_{SSI}} \\ \dfrac{dV_{DC}}{dt} = \dfrac{-i_{load}}{C} \end{cases} \tag{11}$$

Finally, the averaged state-space model of the B-ASSI in saturated mode is described in the following equation (12) :

$$\begin{bmatrix} \dfrac{di_L}{dt} \\ \dfrac{dV_{DC}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L_{SSI}} & -\frac{1-M_{DC}}{L_{SSI}} \\ \frac{1-M_{DC}}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_{DC} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{SSI}} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} V_{in} \\ i_{load} \end{bmatrix} \tag{12}$$

For both mode, with Volt-Second balance, it can be found :

$$\frac{V_{in} M_{DC} T}{L_{SSI}} + \frac{(V_{in} - V_{DC})(1 - M_{DC})T}{L_{SSI}} = 0 \tag{13}$$

The static characteristic or boost ratio can then be derived from (13) and is expressed by equation (14) :

$$\frac{V_{DC}}{V_{in}} = \frac{1}{1 - M_{DC}} \tag{14}$$

3.2. Proposed Modulation

With the simple SSI and an MSPWM, it is possible to decouple and control both the AC load and the DC bus voltage. But this is true only if the modulation index satisfies (8). To solve this limitation, the principle of a possible modulation scheme of the proposed converter is presented in Fig. 6. With this modulation, the duration of the state V_{111} is adjusted according to the load operating condition. The command signals C_{a1}, C_{b1}, and C_{c1} of the clamping switches, then adjust discharging time of the inductor current during the active state according to the desired boost factor. This can be seen as the duty cycle for S_{a1} is set to the same $1 - M_{DC}$ independently of the M_{ac}. The DC bus voltage boost factor $1/(1 - M_{DC})$ and the modulation index M_{AC} are truly decoupled for the entire speed range of the drive.

The generated command signals C_{x1} are plotted in Fig. 7. Those command signals are generated from a duty cycle called $D_{x1}(x = a, b, c)$ described in Fig. 6 and defined by the following equation (15) :

$$D_{x1} = \begin{cases} (1 - M_{DC}) & \text{when } (1 - M_{DC}) \geq D_x \\ 0 & \text{otherwise} \end{cases} \tag{15}$$

The resulting duty cycles of the inverter legs $D_x(x = a, b, c)$ and of the clamping switches D_{x1} are then compared to the same triangle carrier wave. Since only one or at most two duty cycles D_x are equal to the lower envelope, at least one duty cycle D_{x1} is set to one. This ensures that at any moment, all three clamping switches are not set OFF at the same time. The command signals of the switches S_{a2}, S_{b2} and S_{c2} are generated from the other command signals for the switches S_x and S_{x1}, and are plotted in Fig. 7. If the inductor is charging, the switches imitate

Table 2: All working states of the proposed modulation for the inverter.

Vector	C_a^h	C_b^h	C_c^h	C_{a1}	C_{b1}	C_{c1}	C_{a2}	C_{b2}	C_{c2}	Inductor State
V_{000}	0	0	0	1	1	1	1	1	1	Charge
V_{100}	1	0	0	0	0	0	-	-	-	-
V_{100}	1	0	0	x	x	x	0	1	1	Charge
V_{100}	1	0	0	1	0	0	1	1	1	Discharge
V_{110}	1	1	0	0	0	0	-	-	-	-
V_{110}	1	1	0	x	x	x	0	0	1	Charge
V_{110}	1	1	0	1	1	0	1	1	1	Discharge
V_{010}	0	1	0	0	0	0	-	-	-	-
V_{010}	0	1	0	x	x	x	1	0	1	Charge
V_{010}	0	1	0	0	1	0	1	1	1	Discharge
V_{011}	0	1	1	0	0	0	-	-	-	-
V_{011}	0	1	1	x	x	x	1	0	0	Charge
V_{011}	0	1	1	0	1	1	1	1	1	Discharge
V_{001}	0	0	1	0	0	0	-	-	-	-
V_{001}	0	0	1	x	x	x	1	1	0	Charge
V_{001}	0	0	1	0	0	1	1	1	1	Discharge
V_{101}	1	0	1	0	0	0	-	-	-	-
V_{101}	1	0	1	x	x	x	0	1	0	Charge
V_{101}	1	0	1	1	0	1	1	1	1	Discharge
V_{111}	1	1	1	1	1	1	1	1	1	Discharge
-	Forbidden State									
x	Any other state									

the diode function. It is set to one if the lower switch of the considered leg is ON or when there is a state V_{111}. If the inductor discharge is requested during an active state, then the switch must be ON when the high side switch of the considered inverter leg is ON. Finally, the lower envelope is dependent on the load operating conditions and can be freely increased or decreased. Two cases can be differentiated and are stated in (16). If $M_{ac} \leq (1 - M_{DC})$, the classical MSPWM Fig. 5 can be used and if $M_{ac} > M_{DC}$, the proposed modulation Fig. 6 is used. The block schematic of the proposed modulation is represented in Fig. 12.

$$\begin{cases} (1 - M_{DC}) & \text{when } M_{ac} \leq (1 - M_{DC}) \\ (1 - M_{ac}) & \text{when } M_{ac} > (1 - M_{DC}) \end{cases} \tag{16}$$

In order to ensure that all the states are well respected, the duty cycles D_{x1} must be saturated by a maximal value expressed by (17) :

$$M_{DC} \geq (1 - \sqrt{3}/2) \cdot M_{ac} \tag{17}$$

The minimal elevation ratio function of the modulation index is stated by equation (18) :

$$\frac{V_{DC}}{V_{in}} \geq \frac{1}{1 - (1 - \frac{\sqrt{3}}{2}) \cdot M_{ac}} = \frac{2}{\sqrt{3} \cdot M_{ac}} \tag{18}$$

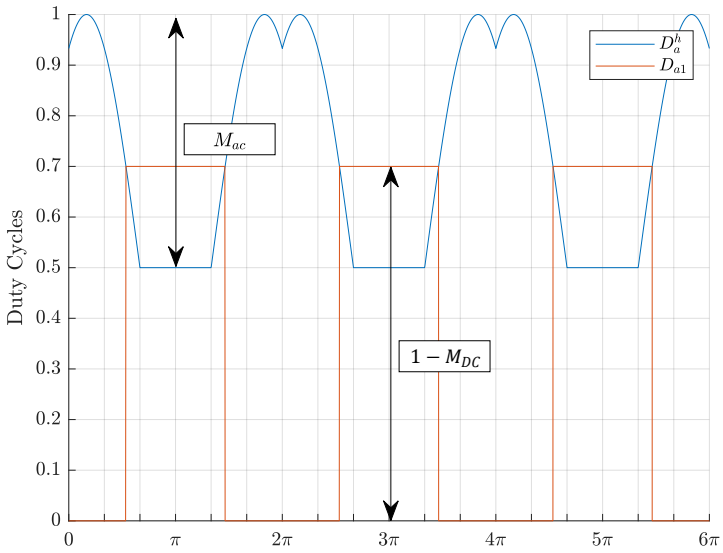


Figure 6: Definition of the proposed Modulation for phase A, in blue the duty cycle D_a for S_a^h, in orange the duty cycle D_{a1} for S_{a1}.

3.3. Generation of the command signals taking Dead-Time into account

As stated in [26], the use of a single switch in reverse conduction mode is not sufficient to overcome the inherent SSI limitation. In the ASSI, the use of diodes in series with the clamping switch was sufficient, as the diode passively open to prevent the DC bus from the shoot-through phenomenon. However, in an automotive application, the use of reverse blocking devices will not enable bidirectional power flow, which is needed for regenerative braking. Therefore, the additional second clamping switches S_{a2}, S_{b2} and S_{c2} are required, and their commands C_{a2}, C_{b2}, and C_{c2} must avoid the same shoot-trough states and allow bidirectional power flow. The generations of the command signals must be controlled precisely to enable adequate performance and avoid creating any undesired state. This subsection focuses on how to generate the appropriate command signals for the additional switches to ensure bidirectionality under any load operating conditions, taking into account the practical constraints of the converters.

There are three conditions to respect when selectring the states :

1. The two switches of the inverter leg should not be turned on simultaneously. Dead-times are still mandatory.
2. The three clamping switches S_{a1}, S_{b1} and S_{c1} should not be turned off simultaneously. The inductor current shall not be discontinuous.
3. The clamping switches S_{a1}, S_{b1} and S_{c1} as well as S_{a2}, S_{b2} and S_{c2} must not create a state where the DC bus would be experiencing a shoot-through phenomenon.

With the proposed modulation, bidirectional power flow is achieved by generating the command signals C_{a2}, C_{b2} and C_{c2} with simple logic from existing PWM signals (C_x and C_{x1}, $x = a, b, c$). This means that no additional PWM driver is needed for the switch S_{x2}. The function is implemented in programmable logic and is given by (19) and (20).

$$C_{x2} = ((\overline{C_a^l} \cdot \overline{C_b^l} \cdot \overline{C_c^l}) + C_x^l) \cdot \overline{Discharge} + Discharge \tag{19}$$

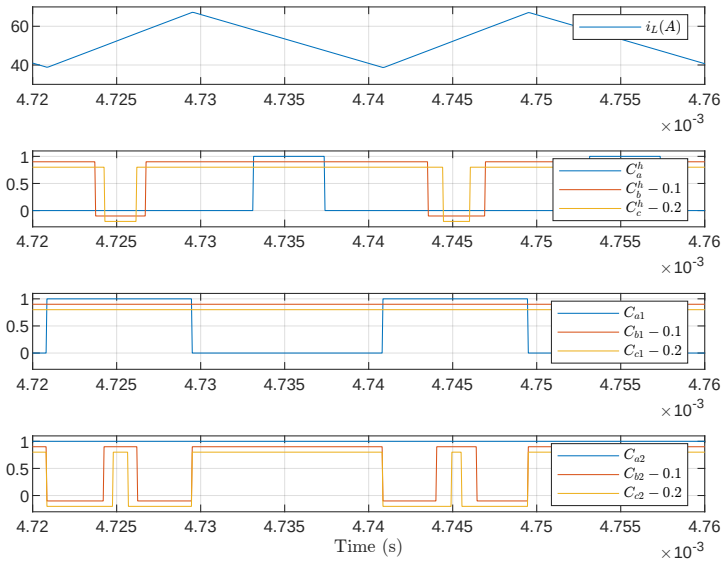


Figure 7: Obtained command signals for each clamping switch S_x, and S_{x2} .

$$Discharge = \overline{C_{a1}} + \overline{C_{b1}} + \overline{C_{c1}} \tag{20}$$

This function is generated by considering all the conduction cases. For demonstration, three cases are presented in Fig. 8, Fig. 9 and Fig. 10. Since the proposed B-ASSI can operate in two modes, it may or may not require an inductive discharge during an active state. When an inductive discharge is not necessary, the switches S_{x1} are always ON, and the diode mimic the conduction states from the SSI described in Tab. 1. In the other mode, the inductive discharge can take place during the first or the second active state of the switching period. The difference lies in whether one or two clamping switches S_{x1} need to be turned OFF. In Fig. 8, the latter case is depicted. On the left-hand side, the chronogram of the modulation for the given switching period is given. The sub-figures from Fig. 8b to Fig. 8e describe the circuit from the initial states until the inductive discharge is achieved. This case represents the most complicated scenario that can be encountered under normal conditions. The discharge function is thus created to detect the exact states where the discharge is needed. The appropriate states of the switches C_{x2} are given to prevent any shoot-trough phenomenon during the entire switching cycle. Furthermore, the inductor current can be negative during the entire operation, thus achieving bidirectional power-flow. Since dead-times are still required for the topology, it is necessary to consider the proper operation of the switches S_{x2} in any state that could occur. Fig. 9 shows the importance of considering dead-times, as well as the significance of referencing the logic function (19) to the signals with applied dead-times (C_x^l). The scenario depicted in Fig. 9 shows the operation of the B-ASSI in non-saturated mode, meaning there is no need to discharge the inductor during an active state. In these figures, the commands signals C_{x2} are not the ones that are implemented, but a version that does not take into account dead-times. In this mode, when $C_{x1} = 1$, the function $Discharge = 0$, and finally, the logic function is set to $C_{x2} = C_a^h \cdot C_b^h \cdot C_c^h + C_x^l$. This case considers

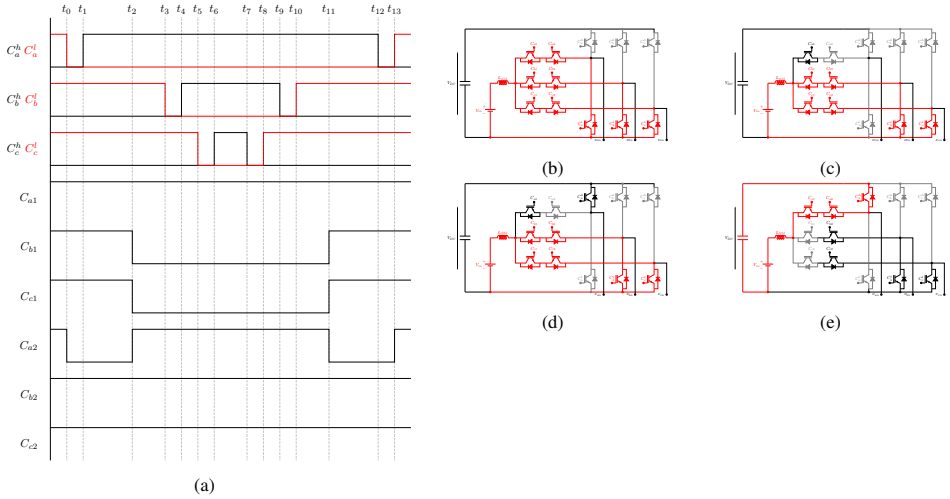


Figure 8: Operation of the B-ASSI with the proposed modulation under normal conditions, (a)-Chronogram, (b)-$t\epsilon[0;t_0]$, (c)-$t\epsilon[t_0;t_1]$, (d)-$t\epsilon[t_1;t_2]$, (e)-$t\epsilon[t_2;t_3]$, (f)-$t\epsilon[t_3;t_4]$.

a particular moment where the dead-times of two different phases (B and C) overlap each other. As depicted in Fig. 9f, the operation of the B-ASSI under this altered modulation results in a state where all three switches S_{a2}, S_{b2} and S_{c2} are OFF. If the inductor current is positive, this does not pose a problem for the topology and a discharge of the inductor will take place through the diodes. But if the inductor current is negative during this instant, it will create a discontinuity in the inductor current accompanied by an over-voltage across the switches, which can lead to their destruction. Since in this work the topology has to work in both motor and generator modes, the proposed logic function is created considering all the states where a discontinuity of the inductor current or a shoot-through of the DC-bus voltage may occur. In order to demonstrate the robustness of the proposed modulation, Fig. 10 illustrates a case where the discharge requested by the control can take place during the dead-time of any phase. Fig. 10 depicts the same case as in Fig. 8 but when the inductive discharge begins during the dead-time. To prevent any undesired phenomena, the logic function references the signals C_x^l with dead-time applied. This enables the circuit to perform under these specials occurrences without being damaged or without impacting the load.

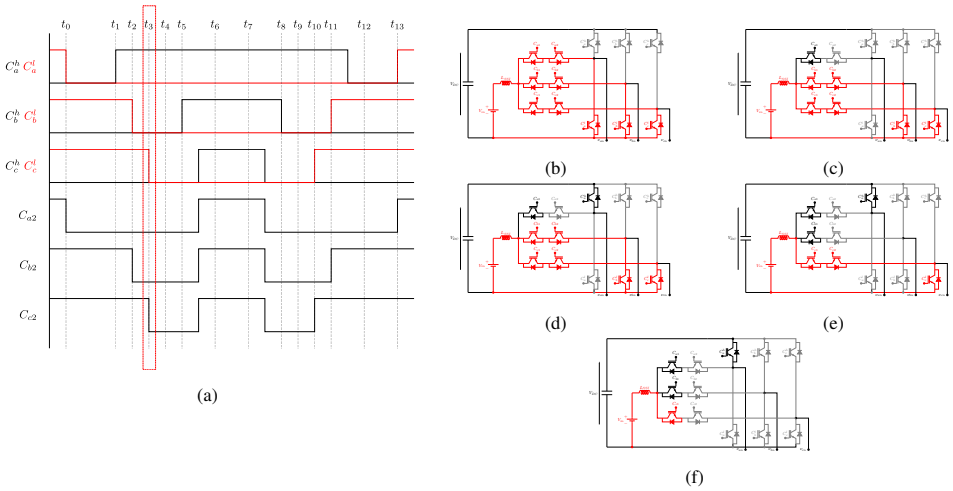


Figure 9: Fault appearance of the B-ASSI in non-saturated mode without the proposed command signals C_{x2} , (a) - Chronogram, (b)-$t\epsilon[0;t_0]$, (c)-$t\epsilon[t_0;t_1]$, (d)-$t\epsilon[t_1;t_2]$, (e)-$t\epsilon[t_2;t_3]$: discontinuity of the inductor current.

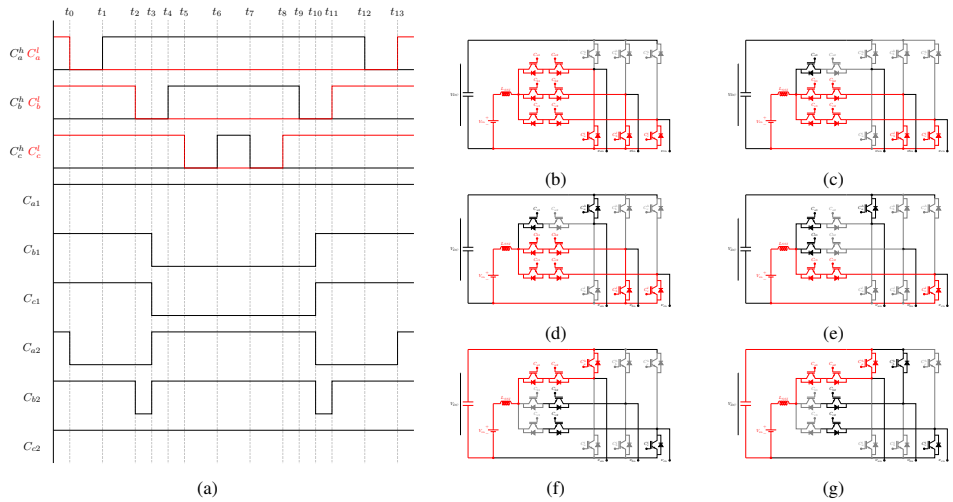


Figure 10: Operation of the B-ASSI with the proposed modulation under the worst-case scenario , (a)-Chronogram, (b)-$t\epsilon[0;t_0]$, (c)-$t\epsilon[t_0;t_1]$, (d)-$t\epsilon[t_1;t_2]$, (e)-$t\epsilon[t_2;t_3]$, (f)-$t\epsilon[t_3;t_4]$, (g)-$t\epsilon[t_4;t_5]$.

3.4. Voltage and current stresses and comparison with other single-stage topologies

This subsection aims to illustrate the degree of freedom gained by the proposed topology compared to other classical single-stage boosting topologies. This is done by considering the maximum attainable AC phase voltage at a given DC bus voltage for different topologies. It is equivalent to considering the voltage stresses across the switches. Two ratios are thus being considered : the boost ratio given by V_{DC}/V_{in} and the peak phase voltage V_ϕ normalized by the input voltage V_{in}. The calculated ratios for the studied topologies are summarized in Tab. 3.

Table 3: Input/Output relationship of classical two-level inverter and different considered single-stage topologies

Architectures	V_{DC}/V_{in}	V_ϕ/V_{in}
2L - VSI	1	$\frac{M_{ac}}{\sqrt{3}}$
ZSI - constant Boost [32]	$\frac{1}{\sqrt{3}M_{ac}-1}$	$\frac{M_{ac}}{2(\sqrt{3}M_{ac}-1)}$
SSI - SPWM [8]	$\frac{4\pi}{2\pi-3\sqrt{3}M_{ac}}$	$\frac{2\pi M_{ac}}{2\pi-3\sqrt{3}M_{ac}}$
SSI - MSPWM [8]	$\frac{1}{1-M_{ac}}$	$\frac{M_{ac}}{\sqrt{3}(1-M_{ac})}$
Proposed B-ASSI	$\frac{1}{1-M_{DC}}$	$\frac{M_{ac}}{\sqrt{3}(1-M_{DC})}$

The characteristics of the two-level inverter is also derived for comparison purposes, where the DC bus voltage cannot be increased and is fixed. The peak phase voltage can take values from 0 to the maximum modulation ratio in SVPWM $M_{ac} = 1/\sqrt{3} = 0.57$. The Z-source inverter can achieve the same peak phase voltage as the two-level inverter when the shoot-through time is set to zero. It can elevate the DC bus voltage with one of the proposed modulation (for instance, the constant Boost modulation [32]). The classical SSI with SPWM has an inherent boost ratio that is linked to the modulation index. The static gain can be derived from the average value of the lower envelope of the reference wave of the duty cycle. The use of MSPWM with the classical SSI can decoupled the boost ratio and the modulation index at a certain point. However, the condition stated in equation (8) must be respected. To minimize the voltage stress, the minimal DC bus voltage needed to achieve the desired peak voltage is used. Thus, the static characteristic of the SSI with MSPWM, originally given by $1/(1 - M_{DC})$, is transformed to $1/(1 - M_{ac})$ to respect equation (8) and minimize voltage stresses. Finally, for the proposed topology, the modulation index and the boost ratio are truly decoupled, (8) does not need to be respected. As a result, the required DC bus voltage for a given peak voltage can be much lower. The new limit of the converter resides in the minimal DC bus voltage needed when no elevation is required, as stated earlier in equation (18). Fig. 11 presents the static gain and the attainable peak voltages for the different discussed topologies. As stated, it can be observed

Table 4: Current stresses of the proposed topology

	B-ASSI
Upper Switch	$I_{max} = I_\phi$
Upper freewheeling Diode	$I_{max} = \frac{i_L+\Delta i_L}{3}$
Lower Switch	$I_{max} = i_L + \Delta i_L + I_\phi$
Lower freewheeling Diode	$I_{max} = I_\phi$
DC side additional Switches	$I_{max} = i_L + \Delta i_L$

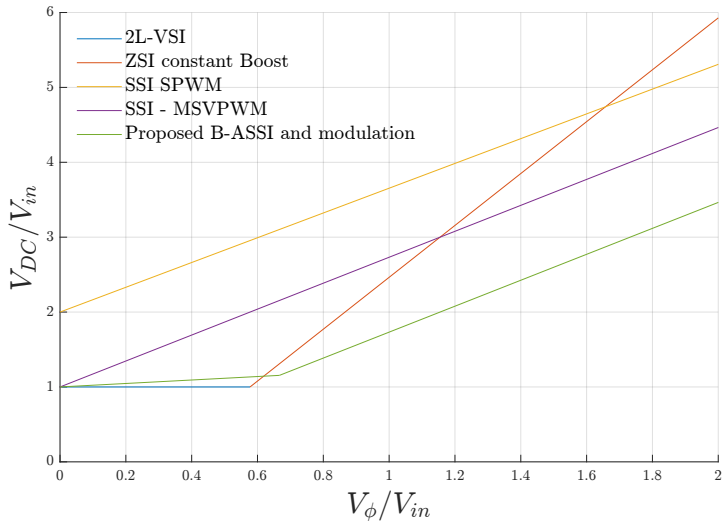


Figure 11: Voltage stresses : boost ratio V_{DC}/V_{in} versus normalized peak voltage V_ϕ/V_{in}

that the lower the curves, the less voltage stress is applied to the switches. This means that the proposed topology offers significantly more achievable operating points than previous SSI topologies and lesser voltage stress compared to any SSI-derived topology. The advantages in terms of voltage stresses becomes even more significant when compared to the first version of the ZSI proposed in [1]. With the topology, there is no needed for over-elevation of the DC bus voltage, unlike other single-stage boosting topologies. The current stresses, symbolized by the maximal current I_{max} seen by the switches of the proposed B-ASSI, are summarized in Tab. 4 where I_ϕ is the peak phase current, i_L is the mean input current flowing through L_{SSI}, and Δi_L is the current ripple. The current stresses are identical to those of the classical SSI. Lastly, Tab. 5 summarizes the added degree of freedom as well as the cost of the topology to put things into perspective. The proposed B-ASSI includes more active switches,resulting in an increase in losses and cost. All SSI topologies have the same boosting ratio, but the degree of freedom to control it entirely is only accessible to the ASSI and the B-ASSI. Thus, the proposed B-ASSI offers access to operating points that are not attainable with classical SSI topologies, which is needed for automotive applications. The B-ASSI also presents reduced voltage stress with the same current stress as the classical SSI. Furthermore, the very fast switching of the input diodes are necessary and becomes a problem for classical SSI. This problem is resolved with the use of active switches components such as Wide band Gap semiconductors like GaN or SiC.

Table 5: Comparison of the offered functionality by the proposed converter compared to other single stage topologies

Architectures	Passive elements required	Additional Active Switches required	Additional Passive Diodes required	single or three-phase	Bidirectional capability	Entire modulation ratio range in boosting mode
ZSI in [1]	2L - 2C	0	1	three	no	no
QZSI in [2]	2L - 2C	0	1	three	no	no
SSI in [8]	1L - 1C	0	3	three	no	no
ISSI in [11]	1L - 1C	2	0	single	yes	no
ASSI in [26]	1L - 1C	2	2	single	no	yes
Proposed B-ASSI topology	1L - 1C	6	0	three	yes	yes

4. Simulation Results

The sizing of the proposed converter can be done in the same manner as the SSI, considering the current ripple of the inductor and the voltage ripple of the DC bus voltage. For comparison purposes, the sizing process of the SSI with a classical SVPWM will be recalled. In the case of the SVPWM, the boosting ratio of a classical SSI will exhibit varations at six times the fundamental freqeuncy, mirroring the lower enveloppe of the duty cycle.

$$L_{ssi} \approx \frac{KV_{DC}}{6\omega_1 \Delta i_L} + \frac{V_{in} M_{DC}^{max}}{f_{sw} \Delta i_L} \qquad C \approx \frac{K i_L}{6\omega_1 \Delta V_{DC}} + \frac{i_L (1 - M_{DC}^{min})}{f_{sw} \Delta V_{DC}} \tag{21}$$

For the SSI operated with a MSPWM, as well as for the proposed B-ASSI, the boosting factor will be constant. The sizing of the component does not need to take into account the low-frequency ripple. The difference is that for the B-ASSI, the boosting factor is completely decoupled from the load operating condition and will not be as limited as for the SSI. The choice of values for L_{SSI} and C can be expressed in this case as follows :

$$L_{ssi} \approx \frac{V_{in} M_{DC}}{f_{sw} \Delta i_L} \qquad C \approx \frac{i_L (1 - M_{DC})}{f_{sw} \Delta V_{DC}} \tag{22}$$

It is important to note that a particular effort has been made to enable bidirectionnal power flow. The inductor current of the proposed B-ASSI with the modualtion can be negative. In fact, it is also reversible at near-zero currents, meaning that the proposed B-ASSI would always operate in Continuous Conduction Mode (CCM), which is not possible with the SSI. For this reason it has been chosen to undersize the inductor selection to effectively reduce the volume of the converter. The ripple of the inductor current will be significantly increased, but it will not affect the good operation of the converter since it operates in CCM in both motor and generator modes. The B-ASSI achieves a trade-off by reducing the size of passive elements in exchange for the increaed current ripple.

In this section, a simulation of the proposed converter is carried out with a Permanent Magnet Synchronous Machine (PMSM) in Matlab/Simulink and SimScape, and SimPowerSystems toolboxes. The motor is speed-controlled using classical Field Oriented Control (FOC), and the different parameters used for the simulation are reported in Tab. 6.

The dynamic models of the SSI and B-ASSI can both be derived from their state-space models using small-signals modelling. As a reminder the state-space models of the SSI and B-ASSI are derive in (5) and (12), respectively. In order to linearize the model, let us replace each state variable with its mean value plus a small perturbation signal. Those newly formulated state variables are presented in (23) :

Table 6: Simulated Motor and converter parameters.

Parameter	Symbol	Value
Battery Voltage	V_{in}	30V
Split source Inductor	L_{SSI}	16μH
DC bus Capacitor	C	200μF
Motor Nominal Voltage	V	60V
Switching frequency	f_{sw}	50kHz
Number of pole pairs	p	4
Motor Inductance	L_s	10μH
Motor Resistance	R_s	5mΩ
Flux linkage	ϕ_f	$9.5.10^{-3}$Wb
Motor inertia	J	$2.8.10^{-6} kg.m^2$
Friction coefficient	f	$5.2.10^{-6} N.m.s/rad$
Speed reference	ω^*	[0-15000 rpm]
Maximal load Torque	Γ_{ch}	15 Nm

$$\begin{aligned} v_{DC}(t) &= V_{DC} + \tilde{v_{DC}}(t) \\ i_L(t) &= I_L + \tilde{i_L}(t) \\ m_{DC}(t) &= M_{DC} + \tilde{m_{DC}}(t) \end{aligned} \tag{23}$$

Then the following linearized model for the B-ASSI in saturated Mode can be decribed as follow in (24) :

$$\begin{aligned} \tilde{i_L} &= -\frac{(1-M_{DC})}{L\cdot s + r_L}\tilde{v_{DC}} - \frac{V_{DC}}{L\cdot s + r_L}\tilde{m_{DC}} \\ \tilde{v_{DC}} &= -\frac{(1-M_{DC})}{C\cdot s + r_L}\tilde{i_L} - \frac{I_{load}}{C\cdot s}\tilde{m_{DC}} \end{aligned} \tag{24}$$

Where I_{load} and V_{in} are supposed constant. The transfert function of the DC side of the B-ASSI in saturated mode can be calculated from the given linearized model. Their expression are given in

$$\frac{\tilde{i_L}}{\tilde{m_{DC}}} = \frac{\mathrm{I_{load}} - C\,p\,V_{DC}}{\frac{L_{SSI}\,C}{(1-\mathrm{Mdc})^2}s^2 + \frac{\mathrm{rl}\,C}{(1-\mathrm{Mdc})^2}s + 1} \tag{25}$$

and

$$\frac{\tilde{v_{DC}}}{\tilde{m_{DC}}} = \frac{V_{DC}\,(1-\mathrm{Mdc}) + \mathrm{I_L}\,(\mathrm{rl} + L\,p)}{\frac{L_{SSI}\,C}{(1-\mathrm{Mdc})^2}s^2 + \frac{\mathrm{rl}\,C}{(1-\mathrm{Mdc})^2}s + 1} \tag{26}$$

with the natural frequency of the system and its damping factor that are given in (27) and derived from the caracteristic equation of the system.

$$\omega_n = \frac{(1-M_{DC})}{L_{SSI}C} \qquad \xi = \sqrt{\frac{C}{L_{SSI}}}\frac{r_L}{2(1-M_{DC})} \tag{27}$$

In this paper, a simple solution to control the DC link voltage and inductor current is proposed using cascaded PI controllers, as described in Fig. 12. The design considerations for the two PI

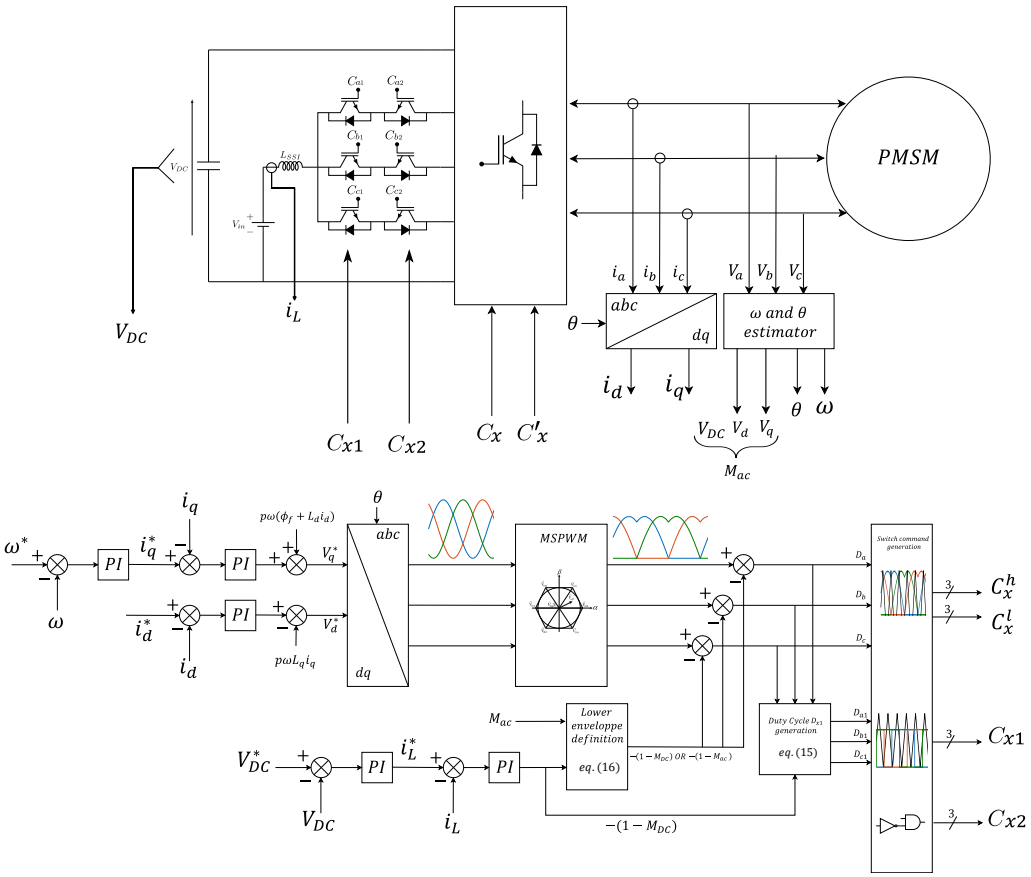
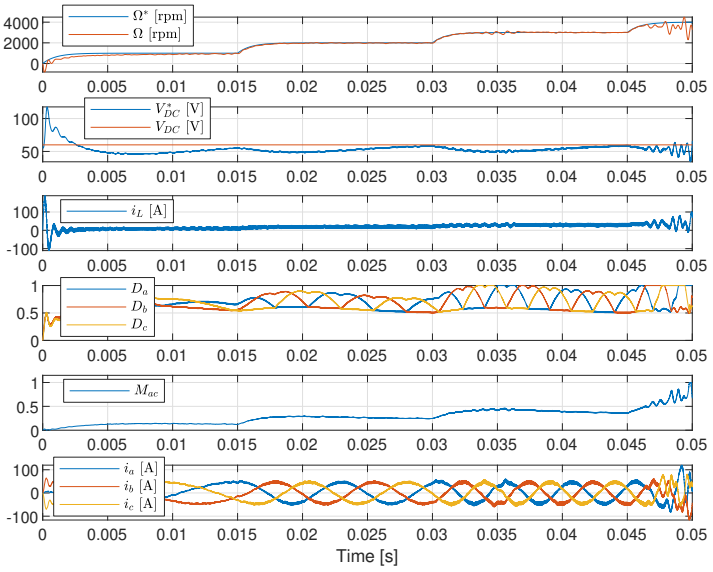


Figure 12: Schematic of the classical FOC implemented for the simulated inverter-fed PMSM.

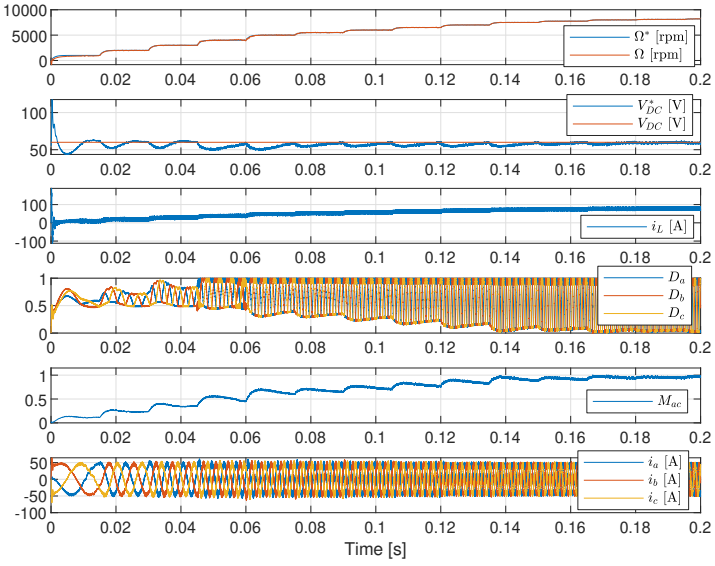
controllers should take into account the output current regulations, which will define the constant value I_{load} for a given operating point. Both controllers should present a bandwidth at least a decade apart from each other. The same is done for the input current and DC bus voltage PI controllers.

In Fig. 13 and Fig. 14, two main tests are carried out. A constant DC bus voltage reference is set to 60V, and the motor reference speed is gradually increased to increase the modulation index. In Fig. 13a, the MSPWM is used. It can be seen that, as long as the load operating conditions impose a modulation respecting the condition (8) the DC bus voltage can be controlled. Since V_{DC}^* is set to two times the input voltage, M_{DC} is set to 0.5. It can be seen that when the modulation index is increased above 0.5, the duty cycle becomes saturated, and the load cannot be controlled anymore. The results for the same conditions with the proposed modulation are plotted in Fig. 13b. Two cases can be distinguished. If the load operating conditions impose a modulation index that satisfies (8), then the lower envelope of the reference wave is chosen by the DC bus voltage controller. The clamping switches S_{a1}, S_{b1} and S_{c1} can remain ON. This is the same operation as a simple SSI with a MSPWM. When the modulation index is increased and when (8) is not satiffied, the lower envelope is set by the modulation index. This way, the

controllability of the load is ensured. The clamping switches are then driven accordingly to achieve the required DC bus voltage. Simulation results show that the load can be driven up to its base speed of $\omega_{BaseSpeed} = 8450rpm$ with a modulation index up to one, while maintaining the DC link voltage at a constant level. This base speed corresponds to a two-level VSI with a 60V battery. In contrast, for the proposed converter, the 60V motor can be driven from a battery delivering only 30V, as chosen for the simulation parameters. Thus, this converter can actually adapt the DC bus voltage from a wide variety of input DC voltage sources. Two more tests are carried out by simulations. Firstly, in Fig. 14a the DC bus voltage can be increased above 60V to drive the motor to a speed higher than the base speed of the vehicle, meaning that the entrance into the flux weakening region can be postponed. Lastly, Fig. 14b shows the obtained waveform for a step load change from $\Gamma_{ch} = +2.7N.m$ to $\Gamma_{ch} = -2.7N.m$. This validates the performance of the converter in generator mode, demonstrating the bidirectional power flow capability of the proposed converter.



(a)



(b)

Figure 13: Simulation results : (a)-Illustration of the limitation of the classical MSPWM used in SSI, (b) for the proposed modulation

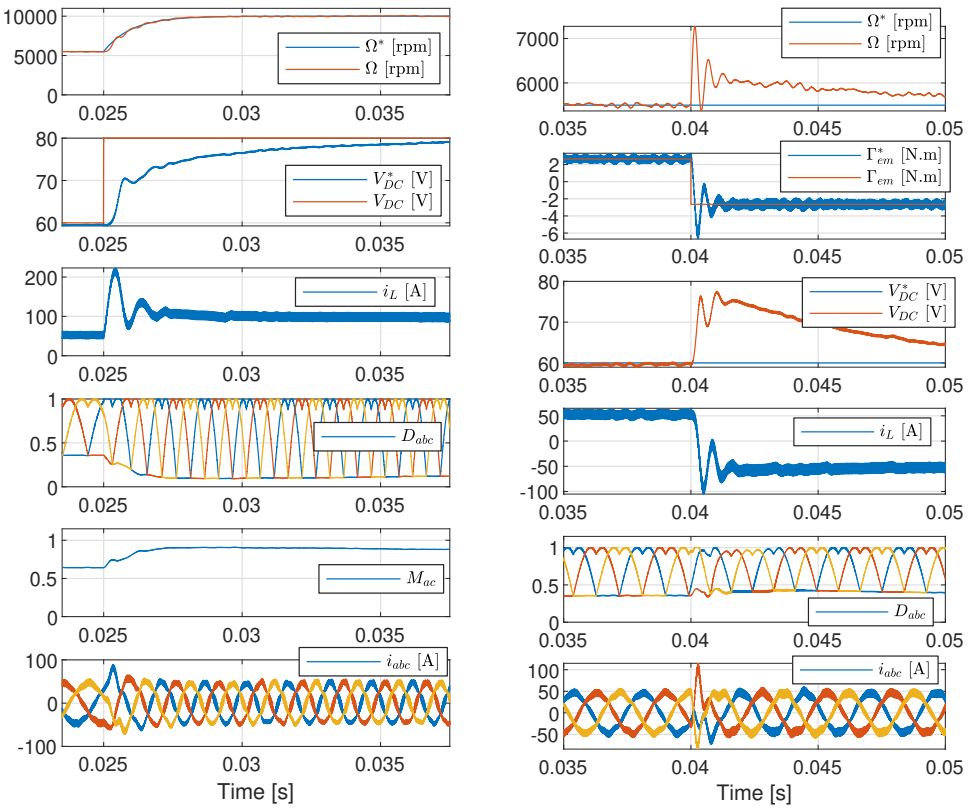


Figure 14: Simulation results : (a)-Above base speed operation with DC bus voltage increase, (b)-Step load change, from motor mode to generator mode.

5. Experimental Results

Table 7: Experimental Motor and converter parameter.

Parameter	Symbol	Value
Battery Voltage	V_{in}	20V
Split source Inductor	L_{SSI}	6μH
DC bus Capacitor	C	460μF
Motor Nominal Voltage	V	48V
Switching frequency	f_{sw}	30kHz
Number of pole pairs	p	1
Motor Inductance	L_s	5μH
Motor Resistance	R_s	3mΩ
Flux linkage	ϕ_f	0.9mWb
Speed reference	Ω^*	[0-30 000 rpm]
Maximal load Torque	Γ_{ch}	3 Nm

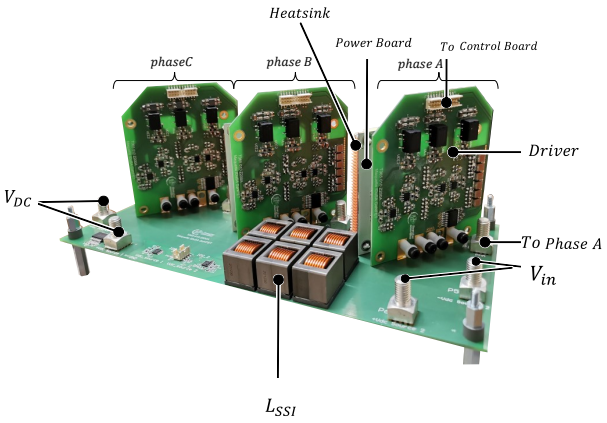
In this last section, a first experimental verification of the proposed three-phase Active Split Source Inverter is carried out. A prototype of a few kW of the converter is proposed and presented, and the setup on the test bench shown on Fig. 15. The values of the parameters of the motor, as well as the sizing for the passive components of the B-ASSI, are presented in Tab. 7. The converter is first tested in open-loop control operation to validate the good operation on a hardware point of view.

5.1. Open-loop operation validation

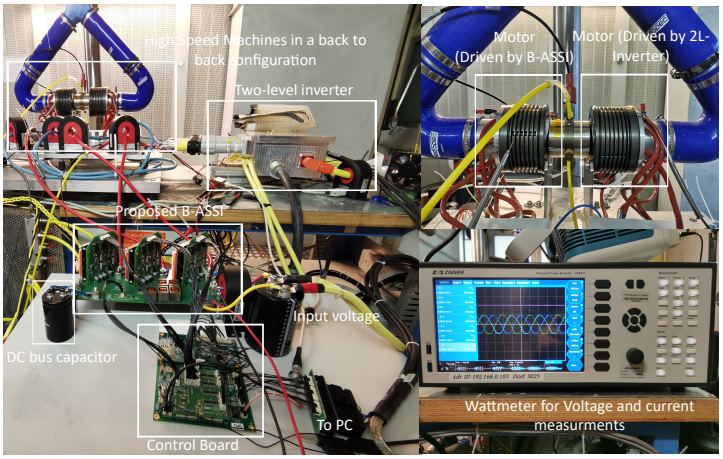
Three experiments are conducted. The first operating mode, called "non-saturate" mode, involves closing three switches S_a^h,S_b^h and S_c^h. In this mode, the duty cycles of the AC-DC conversion stage D_a,D_b and D_c are not saturated. Within this region, two tests are conducted. Firstly, the second set of switches S_{a2},S_{b2} and S_{c2} are forced open to simulate the behavior of diodes used in a classical SSI. The results obtained from this test are presented in Fig. 16. This test illustrates the limitations of a classical SSI for automotive applications, as it can only achieve discontinuous conduction mode. Then, the second switches S_{a2},S_{b2} and S_{c2} are controlled using the proposed logical function derived from the command signals C_a^h, C_b^h and C_c^h. This test thus verifies also the bidirectional power flow capability of the proposed converter in the non-saturated mode. The results of this test are plotted in Fig. 17. In this test, a constant elevation ratio of $D_{dc} = 0.65$ is applied, implying that the theoretical bus voltage $V_{DC} = 29.5V$ should be achieved without considering any losses. It is thus in agreement with the experimental voltage. These tests successfully confirm that the proposed control of the switches S_{a2},S_{b2} and S_{c2} indeed enables bidirectional power flow, even in close to zero operation region . Furthermore, the Boost operation with a constant elevation ratio using the MSPWM is verified.

Finally, the proposed converter in the saturated mode operation is illustrated in Fig. 18a, using the proposed modulation scheme and the experimentally applied duty cycles depicted in Fig. 18b. The input voltage is set to $V_{in} = 12V$, maintained a constant elevation ratio $D_{DC} = 0.8$, and an effective modulation index of $m = 0.24$ is used. These results successfully validate the open-loop operation of the converter, demonstrating that the modulation index can increase

above the limit initially imposed by the elevation ratio. As a result of this test, $D_{dc} = 0.8$ is achieved, and the experimental DC-bus voltage of $15V$ is verified.



(a)



(b)

Figure 15: Experimental validation : (a) – Proposed converter prototype, (b) – experimental setup

5.2. *Closed-loop operation validation*

The converter is tested in a closed-Loop control operation on the test-bench as depicted in Fig. 15. The test bench includes PMSM machines designed for very high-speed operations. To achieve four-quadrant testing capabilities, two machines are connected in a back-to-back configuration. One of the motor is connected to a classical two-level inverter and is controlled independently. This motor will impose the speed of the shared mechanical shaft between the two machines at a mechanical speed of $\Omega = 30000rpm$. The other motor is driven by the proposed B-ASSI. Both inverters are suplied with the same fixed input voltage $V_{in} = 20V$. The AC load is

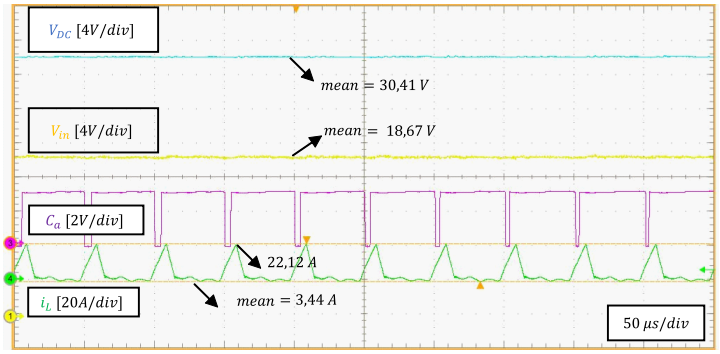


Figure 16: Experimental Results in Open Loop : Proposed converter operating in non-saturated mode with $C_{a1} = C_{b1} = C_{c1} = 1$ and $C_{a2} = C_{b2} = C_{c2} = 0$.

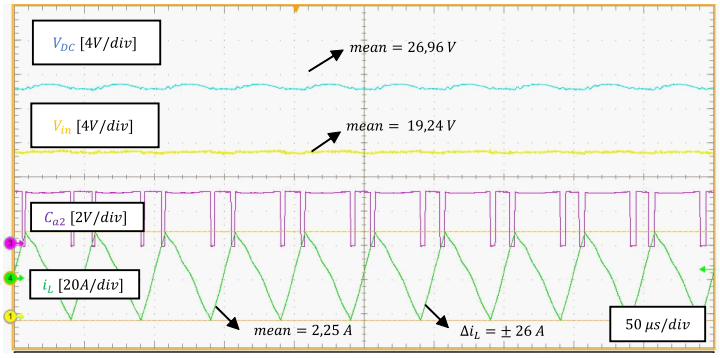
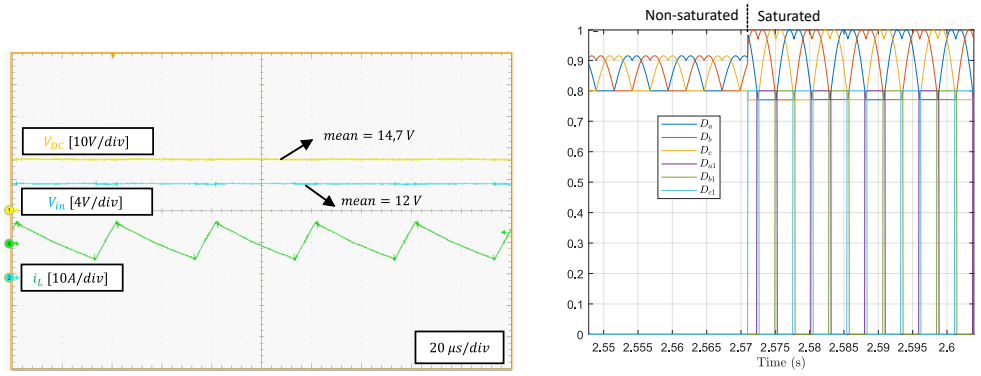


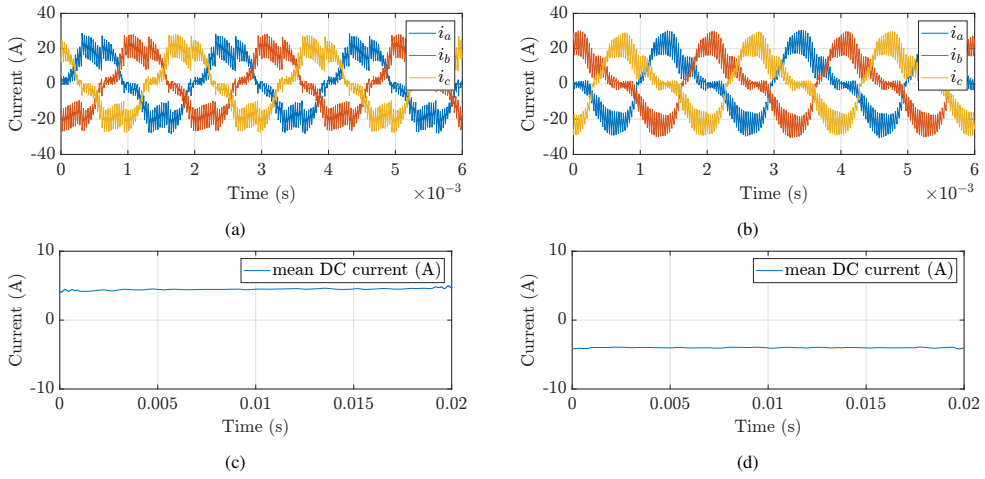
Figure 17: Experimental Results in Open Loop : Proposed converter operating in non-saturated mode for bidirectional power flow verification with only $C_{a1} = C_{b1} = C_{c1} = 1$.

operating in a closed-loop operation. In this second test, the DC bus voltage operated in an open-loop operation and is set to the minimum value required to achieve the necessary peak voltages. The amplitude of the peak currents is regulated at $I_\phi = \pm 20A$, enabling precise control of the torque, and allowinf the machine to operate in motor or generator modes. Fig. 19 illustrates the simulation of the operating point that was tested experimentally. In this simulation, the converter can operate in both motor and generator modes. This can be observed from the sign of the mean input DC current in the inductor of the SSI. The currents waveforms are plotted for comparison with the experiment in Fig. 20. This figure validates and demonstrates the bidirectionality of the proposed converter. The waveforms show good agreement with the simulation, although there is some low- frequency ripple, which can be explained by the very low modulation index of the operating point $M_{ac} \approx 0.15$. This can be further explained by that the dead-times are set to a value quite higher than necessary. It is also possible that the dead-time distortions induce more harmonics on the output compared to the two-level counterpart due to the complexity of the structure. However, the waveforms still show good agreement with the simulation and can be well explained. The proposed converter can thus operate a three-phase machine throughtout its entire operation range, making it bidirectional. Additionnaly, it offers a boost function of the DC bus voltage with a ratio identical to that of the classical DC/DC Boost converter.



(a) (b)

Figure 18: Experimental validation in open-loop of the proposed bidirectional Active Split source inverter in saturated mode (a)-Experimental waveforms, (b)- measured experimental duty cycles applied to the converter.



(a) (b)

(c) (d)

Figure 19: Simulated waveforms in closed-loop operation for the same experimental operating point : (a) – Phase currents in motor mode, (b) – Phase current in generator Mode, (c) – Mean input current i_L in motor mode, (d) – Mean input current i_L in motor mode

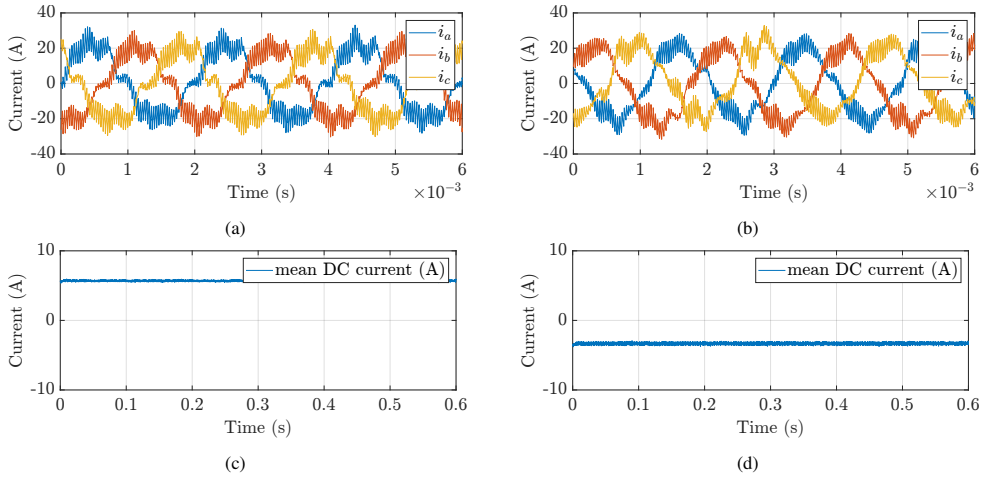


Figure 20: Experimental Waveforms in closed-loop operation at $\Omega = 30000rpm$: (a) – In motor mode, (b) – In generator mode for bidirectionality validation

Conclusion

In this paper, a novel single-stage two-level bidirectional boost inverter compatible with traction applications is presented. The topology is based on the SSI and its derivative, the Active split source inverter. These topologies have previously shown a low DC link voltage utilization ratio. This issue has been effectively resolved in this paper. By using a single inductor and six switches, the inverter functions as a single-stage boost inverter with the capability to independently adjust its DC bus voltage regardless of the load operating conditions. This can effectively offer an EV inverter, reducing constraints on the input sources and provinding robustness to voltage variations. Moreover, the controllable DC link voltage can provide a solution to postpone field weakening operation by increasing the DC link voltage once the initial base speed is reached. Furthermore, only the first set of switches requires additional PWM drivers, as the command for the second set of power switches is generated using simple logic gates based on the command signals of the other switches. Compared to its single-stage counterpart, the proposed B-ASSI presents lower voltage stresses, while maintaining consistent current stresses with the classical SSI. The validity of the proposed converter has been experimentally confirmed through a Proof of Concept prototype.

References

[1] F. Z. Peng, Z-source inverter, IEEE Transactions on Industry Applications 39 (2) (2003) 504–510. doi:10.1109/TIA.2003.808920.

[2] J. Anderson, F. Z. Peng, Four quasi-z-source inverters, in: 2008 IEEE Power Electronics Specialists Conference, IEEE, 2008, pp. 2743–2749. doi:10.1109/PESC.2008.4592360.

[3] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, Impedance-source networks for electric power conversion part i: A topological review, IEEE Transactions on Power Electronics 30 (2) (2015) 699–716. doi:10.1109/TPEL.2014.2313746.

[4] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, S. Yang, Impedance-source networks for electric power conversion part ii: Review of control and modulation techniques, IEEE Transactions on Power Electronics 30 (4) (2015) 1887–1906. doi:10.1109/TPEL.2014.2329859.

[5] D. Mande, J. P. Trovão, M. C. Ta, Comprehensive review on main topologies of impedance source inverter used in electric vehicle applications, World Electric Vehicle Journal 11 (2) (2020). doi:10.3390/wevj11020037.
URL https://www.mdpi.com/2032-6653/11/2/37

[6] A. Battiston, J.-P. Martin, E.-H. Miliani, B. Nahid-Mobarakeh, S. Pierfederici, F. Meibody-Tabar, Comparison criteria for electric traction system using z-source/quasi z-source inverter and conventional architectures, IEEE Journal of Emerging and Selected Topics in Power Electronics 2 (3) (2014) 467–476. doi:10.1109/JESTPE.2014.2298755.

[7] A. Abdelhakim, P. Mattavelli, G. Spiazzi, Split-source inverter, in: IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, IEEE, 2015, pp. 001288–001293. doi:10.1109/IECON.2015.7392278.

[8] A. Abdelhakim, P. Mattavelli, G. Spiazzi, Three-phase split-source inverter (ssi): Analysis and modulation, IEEE Transactions on Power Electronics 31 (11) (2016) 7451–7461. doi:10.1109/TPEL.2015.2513204.

[9] G. Cocco, F. Grigoletto, L. Scherer, R. Camargo, Modeling and control of hydro-pv hybrid power system with three-phase three-leg split-source inverter, Journal of Control, Automation and Electrical Systems 33 (03 2022). doi:10.1007/s40313-022-00911-4.

[10] A. Abdelhakim, P. Mattavelli, P. Davari, F. Blaabjerg, Performance evaluation of the single-phase split-source inverter using an alternative dc–ac configuration, IEEE Transactions on Industrial Electronics 65 (1) (2018) 363–373. doi:10.1109/TIE.2017.2714122.

[11] S. S. Lee, Y. E. Heng, Improved single-phase split-source inverter with hybrid quasi-sinusoidal and constant pwm, IEEE Transactions on Industrial Electronics 64 (3) (2017) 2024–2031. doi:10.1109/TIE.2016.2624724.

[12] S. S. Lee, A. S. T. Tan, D. Ishak, R. Mohd-Mokhtar, Single-phase simplified split-source inverter (s 3 i) for boost dc–ac power conversion, IEEE Transactions on Industrial Electronics 66 (10) (2019) 7643–7652. doi:10.1109/TIE.2018.2886801.

[13] S. S. Lee, A. S. T. Tan, D. Ishak, R. Mohd-Mokhtar, Single-phase simplified split-source inverter (s3i) for boost dc–ac power conversion, IEEE Transactions on Industrial Electronics 66 (10) (2019) 7643–7652. doi:10.1109/TIE.2018.2886801.

[14] A. Abdelhakim, P. Mattavelli, Analysis of the three-level diode-clamped split-source inverter, in: IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, IEEE, 23/10/2016 - 26/10/2016, pp. 3259–3264. doi:10.1109/IECON.2016.7793581.

[15] A. Abdelhakim, P. Mattavelli, G. Spiazzi, Three-phase three-level flying capacitors split-source inverters: Analysis and modulation, IEEE Transactions on Industrial Electronics 64 (6) (2017) 4571–4580. doi:10.1109/TIE.2016.2645501.

[16] S. H. Montazeri, J. Milimonfared, M. Zolghadri, A new modeling and control scheme for cascaded split-source converter cells, IEEE Transactions on Industrial Electronics 69 (8) (2022) 7618–7628. doi:10.1109/TIE.2021.3111559.

[17] S. H. Montazeri, J. Milimonfared, M. R. Zolghadri, Multidimensional pulsewidth modulation for cascaded split-source inverter, IEEE Transactions on Industrial Electronics 70 (1) (2023) 137–146. doi:10.1109/TIE.2022.3150087.

[18] M. S. Hassan, A. Abdelhakim, M. Shoyama, J. Imaoka, G. M. Dousoky, Parallel operation of split-source inverters for pv systems: Analysis and modulation for circulating current and emi noise reduction, IEEE Transactions on Power Electronics 36 (8) (2021) 9547–9564. doi:10.1109/TPEL.2021.3052676.

[19] M. S. Hassan, A. Abdelhakim, M. Shoyama, J. Imaoka, G. M. Dousoky, Three-phase split-source inverter-fed pv systems: Analysis and mitigation of common-mode voltage, IEEE Transactions on Power Electronics 35 (9) (2020) 9824–9838. doi:10.1109/TPEL.2020.2971374.

[20] A. Abdelhakim, P. Mattavelli, V. Boscaino, G. Lullo, Decoupled control scheme of grid-connected split-source inverters, IEEE Transactions on Industrial Electronics 64 (8) (2017) 6202–6211. doi:10.1109/TIE.2017.2677343.

[21] M. Chen, C. Yin, P. C. Loh, Magnetically coupled high-voltage-boost split y -source inverter without leakage-induced voltage spikes, IEEE Transactions on Industrial Electronics 67 (7) (2020) 5444–5455. doi:10.1109/TIE.2019.2931227.

[22] A. Abramovitz, B. Zhao, K. M. Smedley, High-gain single-stage boosting inverter for photovoltaic applications, IEEE Transactions on Power Electronics 31 (5) (2016) 3550–3558. doi:10.1109/TPEL.2015.2457454.

[23] F. Akbar, H. Cha, H. F. Ahmed, A. A. Khan, A family of single-stage high-gain dual-buck split-source inverters, IEEE Journal of Emerging and Selected Topics in Power Electronics 8 (2) (2020) 1701–1713. doi:10.1109/JESTPE.2019.2894384.

[24] M. Chen, C. Yin, P. C. Loh, Magnetically coupled high-voltage-boost split y-source inverter without leakage-induced voltage spikes, IEEE Transactions on Industrial Electronics 67 (7) (2020) 5444–5455. doi:10.1109/TIE.2019.2931227.

[25] S. M. Dabour, M. A. Alotaibi, A. A. Abd-Elaziz, M. A. Alshahat, M. Abdallah, A. M. Eltamaly, A. S. Abdel-Khalik, A. M. Massoud, S. Ahmed, Modeling and control of single-stage quadratic-boost split source inverters, IEEE Access 10 (2022) 24162–24180. doi:10.1109/ACCESS.2022.3153510.

[26] C. Yin, W. Ding, L. Ming, P. C. Loh, Single-stage active split-source inverter with high dc-link voltage utilization, IEEE Transactions on Power Electronics 36 (6) (2021) 6699–6711. doi:10.1109/TPEL.2020.3038688.

[27] S. M. Dabour, A. A. Aboushady, I. A. Gowaid, M. A. Elgenedy, M. E. Farrag, Analysis and control of simplified dual-output single-phase split-source boost inverters, in: 2022 23rd International Middle East Power Systems Conference (MEPCON), 2022, pp. 1–5. doi:10.1109/MEPCON55441.2022.10021748.

[28] G. M. Cocco, F. Ecke Bisogno, R. F. de Camargo, F. B. Grigoletto, Multi-input split-source inverter (missi), in: 2022 14th Seminar on Power Electronics and Control (SEPOC), 2022, pp. 1–6. doi:10.1109/SEPOC54972.2022.9976412.

[29] S. M. Dabour, A. S. Abdel-Khalik, S. Ahmed, A. Massoud, An optimal pwm technique for dual-output nine-switch boost inverters with minimum passive component count, IEEE Transactions on Power Electronics 36 (1) (2021) 1065–1079. doi:10.1109/TPEL.2020.3001372.

[30] M. K. Pinjala, R. Bhimasingu, Improving the dc-link utilization of nine-switch boost inverter suitable for six-phase induction motor, IEEE Transactions on Transportation Electrification 6 (3) (2020) 1177–1187. doi:10.1109/TTE.2020.3010337.

[31] S. M. Dabour, A. A. Aboushady, I. A. Gowaid, M. A. Elgenedy, M. E. Farrag, Performance analysis and evaluation of multiphase split-source inverters, Energies 15 (22) (2022). doi:10.3390/en15228411.
URL https://www.mdpi.com/1996-1073/15/22/8411

[32] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. Tolbert, D. Adams, Constant boost control of the z-source inverter to minimize current ripple and voltage stress, IEEE Transactions on Industry Applications 42 (3) (2006) 770–778. doi:10.1109/TIA.2006.872927.