Capacitive Deep Trench Isolation-Based CCD-on-CMOS Image Sensor Sensitivity to Total Ionizing Dose

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***Abstract*— This work presents a new type of charge-coupled device (CCD) manufactured using a CMOS process and featuring capacitive deep trench isolation (CDTI). The device is used in a multi-pinned phase mode (MPP) enabling almost constant oxide interface passivation. Flatband shift, dark current, and charge transfer inefficiency (CTI) induced by total ionizing dose (TID) are investigated. Despite the increase of interface states, results show that dark current can be efficiently mitigated by the use of short charge transfer duration, avoiding full interface depletion and free charge generation. It is further shown that trapping by interface states is only lightly affecting CTI as the buried channel keeps electrons far from interfaces. Finally, a clear correlation between flatband shift with full well charge (FWC) reduction is established.**

***Index Terms*— Capacitive deep trench isolation (CDTI), charge-coupled device (CCD), charge transfer inefficiency (CTI), CMOS image sensor (CIS), flatband shift, total ionizing dose (TID).**

I. Introduction

SPACE imaging is a very demanding field of activity requiring continuous technology improvements. CMOS image sensors (CISs), benefiting from constant advances in the manufacturing processes, naturally imposed themselves as the technology of choice to fulfill any space mission specifications. CIS thus supplanted charge-coupled devices (CCDs) offering a higher level of integration with ON-chip CMOS functions, lower voltage swings, and improvements in radiation hardness by design. However, CCD sensors still prove to be perfectly fit for applications requiring a large number of noiseless binning operations. One can cite high-resolution earth scanning imaging applications making use of time delay integration (TDI) [1]. This readout mode capitalizes on the CCD sensor's noiseless charge transfer feature by performing a simultaneous summation of charges with landscape scroll, allowing an artificial increase of exposure time. It leads to a significant improvement in signal-to-noise ratio (SNR) that a CMOS digital domain counterpart cannot achieve at a high line rate.

To take advantage of both technologies, a new kind of CCD manufactured in CMOS technology with a capacitive deep trench isolation (CDTI) used as gates to shape vertically the potential of an n-type buried channel has recently been developed [2]. Such device presents interesting properties in prerad conditions with charge transfer inefficiency (CTI) under 10^{-4}, full well charge (FWC) density of 2.6 ke-/μm^2 and a dynamic range of 78 dB mainly limited by surface trapping and dark current generated by Si/SiO_2 interface defects. Those interfaces which represent a dominant aspect of the register's design are passivated by the use of an inversion hole layer characteristic of a p-MOS junction negatively biased (low state). Thus, the transfer operation requiring a positive bias (high state) has been identified as the main contributor to dark current and CTI since it leads to interface depletion, which are therefore free to generate and trap electrons [3]. Total ionizing dose (TID) leads to the buildup of positive trapped charge in the oxides and increases the trap density at Si/SiO_2 interfaces. In CCDs, it results in large flatband voltage shifts, dark current, and CTI increases [4]. However, it has never been evaluated on a trench-based CCD of this kind.

This work aims at investigating the TID-induced degradation mechanisms in this original device to assess the potential of this technology in a radiation environment, such as space. After presenting the specifications of the two-phase charge transfer mechanism implemented, the experimental conditions used for irradiation and electrical measurements are presented. The final section dedicated to the results includes a comparative analysis of TID effects on flatband shift, dark current, and CTI up to 100 krad (SiO_2).

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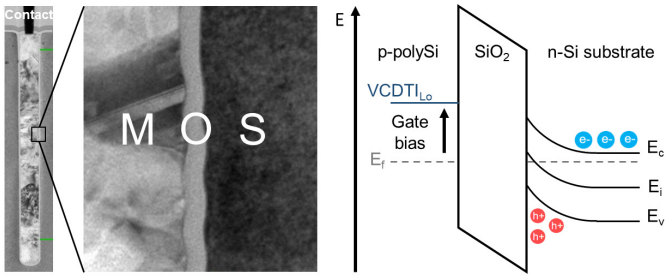


Fig. 1. SEM view of a CDTI with a zoom on the MOS interface (left). Corresponding band diagram when the interface is brought in inversion (right).

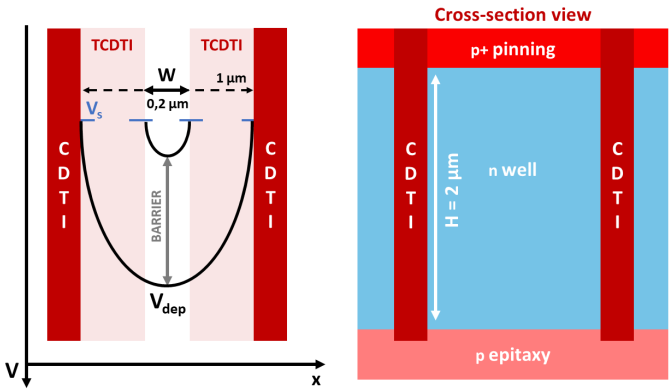


Fig. 2. Plotted the potential profile along the width (x) of the finger (left). A potential barrier is created with TCDTI by reducing W. A cross-sectional view of the register is sketched showing the doped regions (right).

II. Device Description

The device under study differs from classical planar CCDs by using CDTIs as vertical MOS gates. The CDTI is composed of biased p-doped polysilicon separated from the silicon by a thin oxide layer (see Fig. 1). Just like a p-MOS capacitor, the CDTI can be biased in inversion by applying a potential below the substrate voltage (VCDTI_{Lo}) or brought in depletion by applying a positive bias (VCDTI_{Hi}). When inverted, the CDTI interface is passivated meaning traps at midgap energy are populated by holes. As shown in Fig. 2, the pixel's buried channel is composed of an n-well pinched by two facing CDTI, a p-epitaxial layer at the bottom and a p^+ pinning implantation on top. The resulting potential shape in between the two CDTI (axis x) is given by solving the Poisson equation in 1-D using the depletion approximation

$$V(x) = \frac{-N_d q}{2\epsilon}\left(x^2 - Wx\right) + V_s \qquad (1)$$

where W is the space in between trenches, N_d is the concentration of donor atoms, q is the elementary charge, ϵ is the dielectric constant in Si, and V_s is the surface potential. A parabolic potential shape is found with a maximum at $W/2$ implying the attraction of free electrons to the center of the channel. The potential found in the middle is referred to as the depletion potential V_{dep}. The parameter W is reduced at the beginning of each phase to close the finger with a potential barrier by the use of transverse CDTI (TCDTI) with respect to the transfer direction. This barrier, also referred to as a virtual phase, prevents electrons to flow back out of the phase. Consequently, only two phases are required for storage and all phases remain inverted, i.e., passivated at low state. This

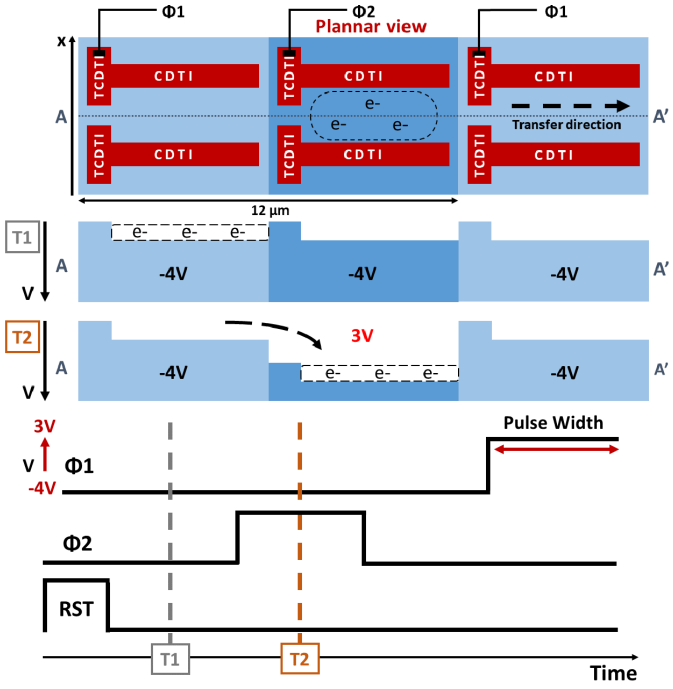


Fig. 3. Adapted from Touron et al. [2]. Planar view of three phases of the line register (top). Two-facing T-shaped CDTI encloses the channel laterally. The two-step transfer operation is sketched with respect to the potential level illustrating the MPP feature (middle). Associated two-phase clocking scheme with time markers associated with the charge transfer operation (bottom).

feature, known as multi-pinned phase (MPP) mode represents one of the main assets of the device. High integration time can be reached without increasing phase opening time where depleted surfaces contribute heavily to the thermal generation of electrons [5]. Charge transfer is obtained by applying a positive voltage to the CDTI gates of the following phase. It has the effect to shift the surface potential V_s proportionally and to switch the gates in depletion mode. The existing barrier created by TCDTI is lowered under the floor of the first phase to allow electrons to flow. The main mechanisms at play are fringing fields (potential gradient) and self-induced drift (charge concentration gradient). Consequently, the applied clocking scheme simply consists of the successive activation of Φ_1 and Φ_2 for transfer operation and reset (RST) at the beginning of each cycle (see Fig. 3).

III. Experimental Setup

The devices used in this study are manufactured and provided by STMicroelectronics. The chosen pixel pitch is 12 μm. In the tested conditions, cycle duration is fixed at 100 μs giving a line frequency of 10 kHz. By default, the transfer duration is set to 10 μs. However, it is considered in this study as a variable in the clocking diagram called PW for pulsewidth (see Fig. 3). High and low biases are set at 3 and -4 V, respectively, with rising and falling edge times equal to PW/10. Note that on other fabrication lots and very similar CDTI-based devices, a VCDTI_{Lo} of -1 V was found sufficient to reach strong interface passivation [2], [6]. Electrical tests are performed on three fingers of 220 pixels line register connected to an injection node and a sense node (see Fig. 4). The input stage consists of n^+ well implantation

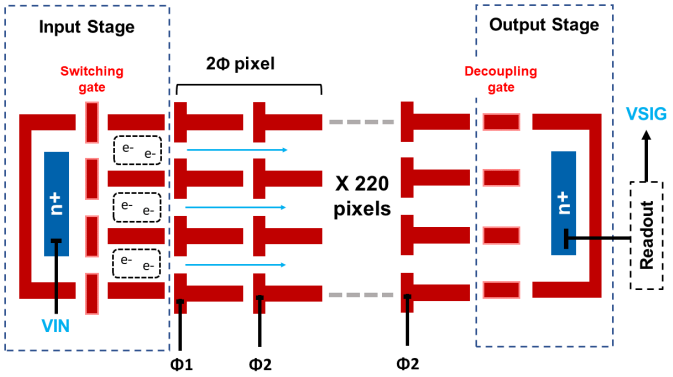


Fig. 4. Simplified representation of the entire test structure used in this study. The register is composed of 220 pixels enclosed in between an input stage to inject a signal and an output stage followed by a source follower readout circuit. Three rows are used to increase the quantity of transferred signals.

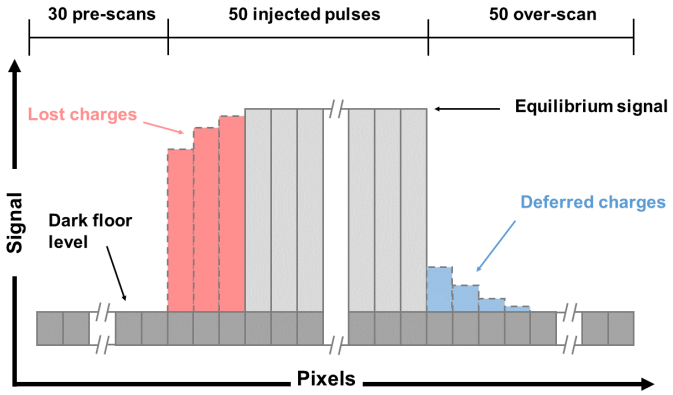


Fig. 5. Sketch of the CTI measure showing the dark ground floor and both lost and deferred electrons required, respectively, to measure FPER and EPER. A large number of scans is necessary to increase the integration of electrons and reduce temporal noise.

followed by a switching gate allowing the generation of synchronous charge pulses using the diode cutoff method. The output stage is composed of a dc biased decoupling gate followed by an n^+ floating diffusion implanted in the register's volume. Electrons dumped in the sense node lower the potential relative to the reference level. The amount of electron is retrieved with a measured conversion factor (CVF) of 22 μV/e-. Packaged devices are plugged into a PCB and driven by a pulse instrument data generator. Irradiation is performed in a temperature-controlled room (22 °C) with a tungsten tube X-ray source operated with peak energy 70 kV and 12.5 mA resulting in 37 krad(SiO_2)/h of dose rate. The device is biased as in-flight conditions during irradiation with the aforementioned timing diagram (PW = 10 μs) and biases. It is well known [7] that the charge yield of X-rays is lower than that of the Co-60 gamma rays used for radiation hardness assurance qualification tests. To maximize the charge yield and minimize possible discrepancies compared to gamma-ray irradiation, worst-case bias conditions have been used here. By doing so, the charge yield achieved in this experiment is expected to be very close (less than a factor of two difference) to the charge yield obtained with gamma rays. Hence, the magnitude of the presented effects at a given TID is assumed to be comparable to what would be obtained with gamma rays with a possible slight underestimation. Electrical tests are carried out right after irradiation in the exact same configuration. Measurements are performed by sequencing the device and triggering each signal acquisition. To be able to read a representative signal of the complete register, at least 220 transfers are required to reach an equilibrium signal. Each point is averaged on >1000 acquisitions and on at least two individual irradiated chips.

CTI is measured using the front pixel edge response method (FPER) and the extended pixel edge response (EPER) [8], [9]. FPER is a measure of the direct signal losses along the transfer path from injection to the output node. It is hence considered an absolute measure of CTI. EPER is a measure of delayed electrons from trapping and re-emission mechanisms. It manifests as a deferred trail following the input signals. Fifty equal charge packets are injected into an empty register and transferred to the output node. The measure is summarized in Fig. 5. CTI is given by the following formulas:

$$\mathrm{CTI_{FPER}} = \frac{\Delta \mathrm{V_{front}}}{n\mathrm{V_{sig}}} \mathrm{CTI_{EPER}} = \frac{\Delta \mathrm{V_{edge}}}{n\mathrm{V_{sig}}} \tag{2}$$

where n is the number of stages, V_{sig} is the equilibrium signal reached by the 50 pulses, $\Delta V_{\mathrm{front}}$ is the sum of lost electrons of the firsts pulses relative to V_{sig}, and ΔV_{edge} is the total amount of deferred electrons. Those charges are integrated on 50 over-scan pixels while the dark floor level is determined by averaging 30 prescan pixels. The mean dark floor value is subtracted from the signal in order to differentiate deferred electrons from dark-generated electrons. In order to obtain the worst-case scenario CTI, every sequence is separated by 220 transfers at identical clocking (22 ms) in order to completely empty the register and let enough time for de-trapping to occur.

Potentials in the depletion and interface surface are measured using the potential barrier measurement. This method is based on direct observation of the input voltage required to overcome the highest potential barrier along the transfer path up to the sense node. From the barrier potential V_b found at the TCDTI is extracted the surface potential V_s by using (1). Due to the thin width W_b (0.2 μm), we retain the hypothesis of a perfect parabolic potential giving a downshift to V_b to retrieve V_s as follows:

$$V_s = V_b - \frac{N_d q W_b^2}{8\epsilon} = V_b - 77.5 \text{ mV}. \tag{3}$$

The depletion potential V_{dep} is obtained using a specific test structure deprived of TCDTI. Hence, the only barrier remaining along the transfer is indeed located at the center of the finger. For potential barriers over 3.3 V, the readout circuit is out of its linear response and it was chosen not to overdrive the transistors which would not have provided a reliable response. Therefore, for VCDTI ranging from 1.25 to 3 V, V_{dep} was estimated using a linear extrapolation based on the data acquired for VCDTI = 0 to 1 V.

IV. Results and Discussion

A. Flatband Shift

It is well known from the literature that TID induces positive trapped charge buildup in oxides [10]. When an electron–hole

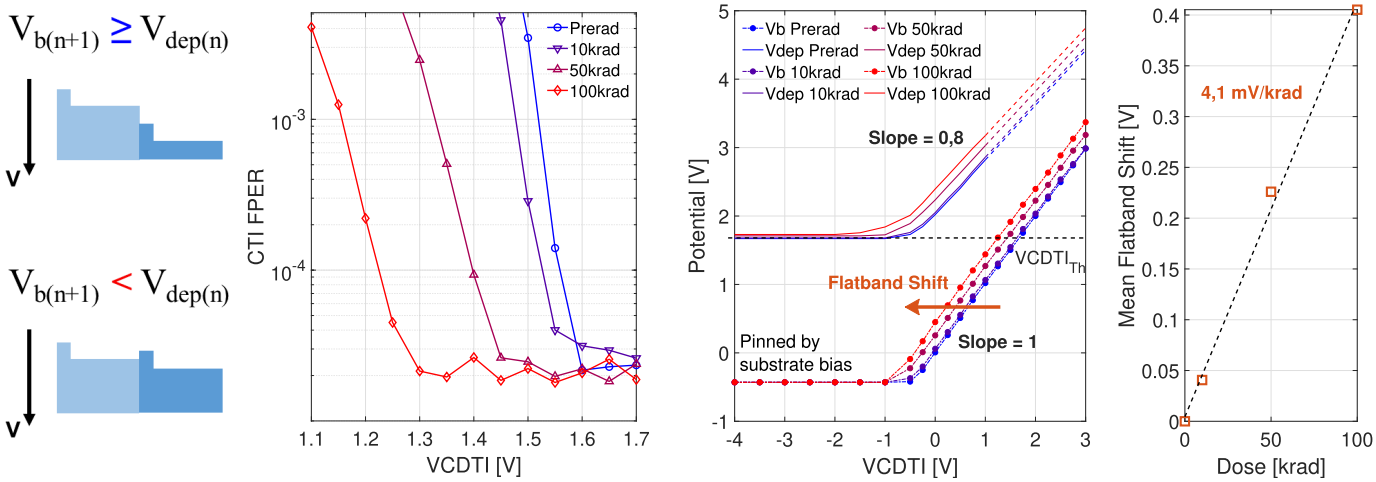


Fig. 6. (a) Sketched the transfer condition on VCDTI along with (b) FPER measures indicating the transfer efficiency threshold. (c) Flatband shift is illustrated by measuring the potential barrier in the prerad and irradiated devices. The surface potential is obtained by analytical derivation from (1) and the measure of the TCDTI barrier potential. The depletion potential is partially estimated using a linear fit for the reasons mentioned in Section III.

pair is generated by an ionizing ray whose energy is over the SiO_2 bandgap, electrons are quickly dispersed either to the gate or to the silicon nearby. On the other hand, holes are carried toward deep stable trap states by hopping transport through a localized high state either at the oxide interface given a positive bias or close to the electrode in the opposite case. The accumulation of trapped holes in the oxide results in a positive voltage shift (V_{fb}) that affects the surface potential and so indirectly the depletion potential. Such consequences on transfer conditions and potential well depth are investigated.

Charge transfer is unaffected by potential pockets as long as the barrier of the following phase reaches a higher voltage than the depletion potential of the current storage phase: $V_{b(n+1)} \geq V_{\text{dep}(n)}$. This condition is illustrated on Fig. 6(a). As a consequence of the flatband shift, the condition of charge transfer is moving with TID. In Fig. 6(b) can be observed a direct measure of the charge transfer efficiency with respect to VCDTI and TID. Under this case of study, the FPER method is more relevant to retrieve the flatband shift as potential pockets are inducing immediate charge losses. The minimum high bias allowing a clean charge transfer is found as expected being gradually reduced with TID. As the condition shifts toward lower CDTI bias, it can be concluded that flatband shift does not induce potential pockets at $\text{VCDTI}_{\text{Hi}} = 3$ V. One can even consider reducing VCDTI_{Hi} to fulfill the power supply constraint. However, the possible effects of CTI are not investigated in this article.

A more accurate observation of V_{fb} is brought by measuring V_{dep} and V_{b} with respect to VCDTI and TID [see Fig. 6(c)]. For low biases, until -0.5 V, V_s is pinned by the inversion layer to the substrate potential and as a consequence V_b and V_{dep} are also unchanged. In other words, the total charge accumulated in the oxides has no effect on the well-potential when interfaces are inverted. It must be pointed out that trapped electrons at the interfaces and in the oxides are expected to induce a threshold shift on top of the flatband shift. With the limited accuracy of the measure, no clear additional shifts were observed at the threshold on V_b, which can mainly be attributed to the fact that it is an indirect measure of V_s. Above -0.5 V (which is considered as the prerad threshold voltage), the barrier and depletion potential increases with VCDTI. The VCDTI threshold (VCDTI_{th}) measured on Fig. 6(b) can be retrieved by prolonging the storage depletion potential toward VCDTI_{Hi} until it meets the barrier potential.

Flatband shift is measurable for positive VCDTI as the inversion voltage pinning disappears. A trend of 4.1 mV/krad is measured by taking the mean V_b barrier difference (assuming a slope of 1). This measure showcases that the barrier potential V_b, i.e., the surface potential V_s increases more than the depletion potential with VCDTI as the extracted slopes are uneven (1 against 0.8). The 1-D potential well approximation does not stand in this complex 3-D architecture. Border effects on CDTI, doping non-uniformity and vertical pinning were neglected. Therefore, the observed shift on V_{dep} is equal to $0.8 \times V_{\text{fb}}$. As the FWC is surface limited, the potential difference $V_{\text{dep}} - V_s$ defines the well depth, hence it is strongly related to the pixel's saturation. As a result, the pixel's FWC is expected to be limited at a high state and even more diminished with flatband shift (see Section IV-D on FWC). Though flatband shift deserves to be investigated considering annealing effects, it is interesting to compare the obtained value of 4.1 mV/krad with classical CCDs usually suffering from flatband voltage shifts of 100–200 mV/krad, nowadays optimized down to 6 mV/krad [11].

B. Dark Current

As TID increases, defects are generated at the Si/SiO_2 interfaces. It is the result of protons released from the SiO_2 lattice during the hole hopping transport and dragged toward the interface. For instance, a dominant mechanism occurring is the reaction of a hole with a hydrogen passivated Si atom (Si-H) which results in a dandling bond [12]. Those

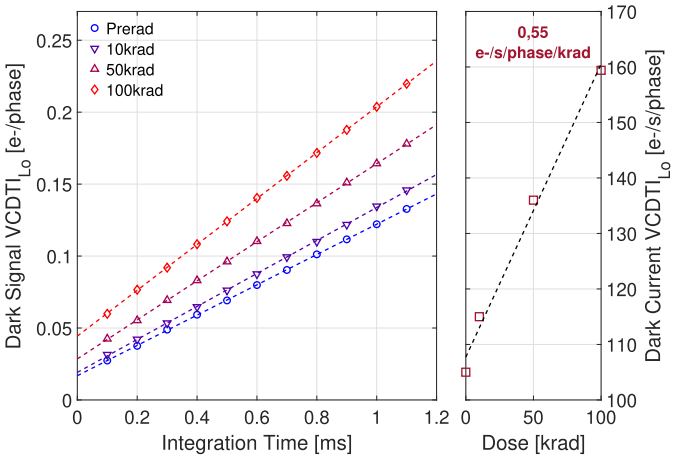


Fig. 7. Mean dark current measured when all phases are at a low state in prerad conditions and after 10, 50, and 100 krad irradiation. A quasi-linear relationship with TID is observed in this dose range.

called Pb centers are responsible for more thermally generated electrons, i.e., dark current as they offer a midgap energy level facilitating the transition from the valence to the conduction band.

It is chosen to differentiate dark current generated at a low state and high state in order to better correlate the mechanisms involved with the physical state of the register. As stated in the introduction, a particular look is given to the device properties of interface state passivation. Different clocking scheme configurations are tested using the parameter pulsewidth (PW) as the variable (see Fig. 3). It defines the duration of a single switch to a high state for the transfer operation. First off, the line register is maintained at a low state so that every phase is inverted. It is followed by a single 1 μs transfer pulse to transfer the accumulated signal onto the next pixel. The value is averaged 1000 times and determined for increasing integration time (see Fig. 7). The prerad measure shows an expected linear behavior with a slope of 105 e-/s/phase. It must be noted that the source value is slightly shifted upward for increasing TID as the dark current generated during the single transfer at high state rises too. At this stage, it is impossible to differentiate dark current induced by bulk traps or diffusion from interface traps, so we can assume the prerad value is composed of these contributions. The measured rates remain reasonable when compared to the prerad value, indicating that the interface passivation is still efficient. The slight degradation of dark current can either be related to a deterioration of the surface hole layer, a geometrical contribution from weakly inverted CDTI regions, or diffusion from upper level SiO_2 layers. A better understanding is brought by the Shockley Read Hall equation yielding the net generation rate at an interface populated with a surface defect density N_{it} [13]

$$U = \frac{\sigma_n \sigma_p v_{\text{th}} N_{\text{it}} \left(\text{np} - n_i^2\right)}{\sigma_n \left[n + n_i \exp \frac{E_t - E_i}{\text{kT}}\right] + \sigma_p \left[p + n_i \exp \frac{-E_t - E_i}{\text{kT}}\right]}. \quad (4)$$

With σ_n and σ_p the electron and hole capture cross sections of the defects, v_{th} the thermal velocity, $E_t - E_i$ the defects energy with respect to the intrinsic Fermi level and kT the thermal energy of the carriers. When interfaces are switched in strong inversion, a local injection of holes originating from the p-epitaxial and p^+ pinning implant occurs. It results in non-equilibrium conditions yielding $\text{pn} < n_i^2$ with $p \gg n_i$ and $n \approx 0$. By use of this hypothesis and assuming $\sigma_n = \sigma_p = \sigma$, the theoretical generation rate becomes [4], [14]

$$U = -\frac{\sigma v_{\text{th}} N_{\text{it}} n_i^2 E_g}{p}. \quad (5)$$

E_g being the Si bandgap. The hole concentration reached during inversion ($p \approx 10^{18}$ cm^{-3}) turns most traps below the Fermi level into a positive state as they are emptied from electrons. The n_i^2 temperature-dependence justify for the increased activation energy found in the literature up to the Si bandgap [6]. Note that this situation stands as hole and electron quasi-Fermi levels are uneven. If we assume equilibrium conditions (i.e., the potential well is full of electrons) $\text{pn} = n_i^2$, the surface generation velocity would virtually be $U = 0$ [15] as it would balance with recombination. For the ionizing dose range explored, this analytical explanation corroborates with a quasi-linear dark current increase scaling with N_{it} [16]. This observation is not fully conclusive at this stage of the investigation since we cannot withdraw the hypothesis of a contribution originating from enhanced diffusion from upper oxide layers. Investigation over activation energies or design parameters is left for future studies. The bottom line remains that charge generation is greatly reduced despite the TID-induced interface trap increase thanks to the important inversion layer hole concentration.

Switching to a high state has the consequence of completely depleting the interfaces with $n \ll n_i$ and $p \ll n_i$. Assuming $\sigma = (\sigma_n \sigma_p)^{1/2}$ the condition on U becomes [8]

$$U = -\frac{\sigma v_{\text{th}} n_i \pi k T N_{\text{it}}}{2}. \quad (6)$$

A dependence in n_i is found, meaning a midgap activation energy is required to enhance the generation process since electrons are able to thermally hop through interface traps. Indeed, the SRH generation is described as a two-step mechanism which first one is the transition of an e- from a valence band to a mid-gap SRH center. Energywise, during inversion holes are able to overlap midgap states and empty them of their electrons by forcing recombination. It means that for the charge generation to resume, interfaces states initially emptied during inversion need to be repopulated by electrons. Burke et al. [17] theorized this phenomenon using the SRH hypothesis showing that several milliseconds are required for the free charge generation to recover its steady-state value. It is described by the simplified hole emission time constant equation ($E_t = E_i$ within 0.3 kT) [17]

$$\tau_e = \frac{1}{\sigma v_{\text{th}} n_i}. \quad (7)$$

Assuming at ambient temperature $\sigma = 10^{-15}$ cm^{-2}, $v_{\text{th}} = 2.67 \times 10^6$ cm $\cdot$ s^{-1} and $n_i = 1.5 \times 10^{10}$ cm^{-3}, a value of roughly 25 ms is obtained. If interfaces are switched back in inversion before, the process can be dynamically suppressed. To properly characterize the device, dark current at a high state is measured taking into account the transfer pulse duration.

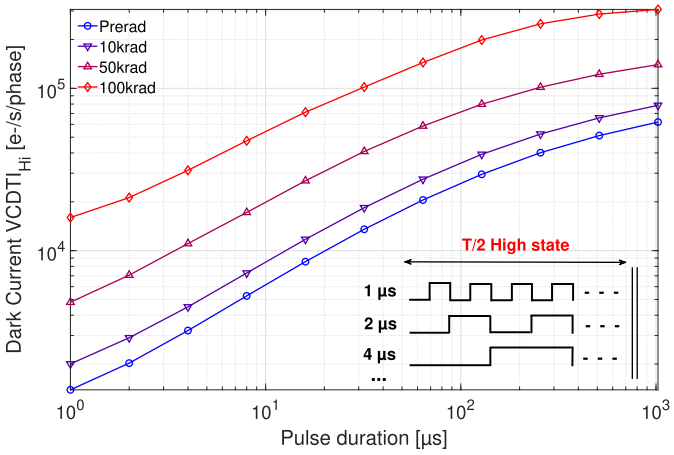


Fig. 8. High state mean dark current measured for increasing transfer pulse duration in prerad conditions and after 10, 50, and 100 krad irradiation. Although transfer duration changes, the dark signal at a high state is integrated over the same integration time.

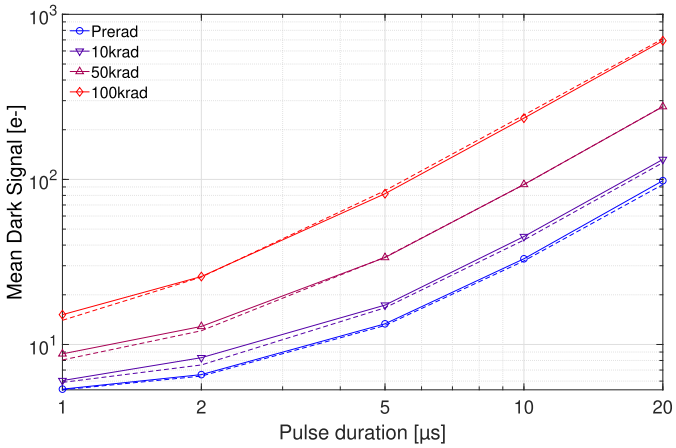


Fig. 9. Mean dark current measured in flight operating conditions with extrapolation from low state and high state data superimposed. For pulse widths shorter than 5 μs, it is the low-state component that dominates dark current for prerad, 10 and 50 krad devices.

To do so, while phase 2 is maintained at a low state to act as a channel stop, phase 1 is switched back and forth from a high to a low state and accumulates a dark signal. The pulse duration is reduced while keeping the total integration time the same: 50% at the high state and 50% at the low state. The signal accumulated is then transferred to the following pixel, and so on until reaching the sense node where the equilibrium signal is measured. As can be seen in Fig. 8, a significant dark current reduction is observed for short pulse duration even though the integration time spent at high state is the same. As expected, dark current is neatly increased with TID even in a partially inverted state. As pulse duration increases and gets close to the order of magnitude of the hole emission time constant, dark current tends toward the steady state value. Whereas for short transfer pulses, the trend softens but struggles to reach full inversion dark current. Indeed in the prerad case at 1 μs, the value is still an order of magnitude above the low state dark current determined in Fig. 7. From this observation, one can derive two possible conclusions. Either the interfaces are less passivated due to the pulsing operation. Or else, another parasitic signal is at play such as spurious charges. Both effects can be worsened with TID as observed on the plot due to the increased amount of interface traps and the increased gate bias (flatband shift). Since the pulse duration is four orders of magnitude smaller than the hole emission time constant, a passivation failure must be explained considering other parameters.

Overall, there is a double benefit in applying short phase aperture time: 1) for reducing total integration time at a high state and 2) for suppressing the free charge generation process. When compared to the value of the low state mean dark current, it is indeed observed that the value is multiplied by a factor of 10 or more which emphasizes the need to mitigate the high state contribution to dark current.

The mean dark signal measured while applying the operational clocking scheme with increasing transfer pulsewidth is plotted in Fig. 9. The signal is integrated over the 440 transfers required to reach the sense node. A calculation of this accumulated dark current is retrieved using a combination of previous data at a low state and high state according to the clocking diagram. It is superimposed to the direct measure and matches correctly. This correlation enables us to determine the respective weight of each contribution at a low state and high state with respect to the total dark signal accumulated. It hence gives an indication of the MPP efficiency depending on the applied clocking. For instance, by using 1 μs transfer pulses, the dark current generated at a high state only counts for 12% of the total prerad dark current. For comparison, at 10 μs the contribution of the high state component is 86% and the dark current accumulated is superior to the one measured at 100 krad with 1 μs transfer pulse. Therefore dither clocking is crucial to optimize the device performance as it almost completely cancels the interface effects on dark current. Results show that TID up to 100 krad seems not to significantly deteriorate the interface passivation. However, the time spent at high-state dark current is directly affected by radiation-induced interface defects as their dynamic suppression loses efficiency.

C. Charge Transfer Inefficiency

One must ensure the proper capacity of the device to operate charge transfer for short phase aperture time. To do so, CTI using the EPER method is measured for an increasing injected signal with pulse widths of 1 and 10 μs (see Fig. 10). FPER CTI measures were also performed to confront the obtained values with those of EPER. Because FPER is a direct measure of CTI, it is often considered an absolute value of CTI, while EPER can be more optimistic by missing some lost charges that have recombined and do not appear in the deferred trail. As FPER gives the same result as EPER while being a noisier measure due to the reduced integration time of lost electrons, it was chosen for clarity to display solely the EPER CTI measure.

As a general trend, fixed losses are observed for low injections (output signal <10 ke-) before transiting to proportional losses which traduce into a CTI plateau of almost constant value. It is interesting to note that this transition point between fixed and proportional losses does not move with increased

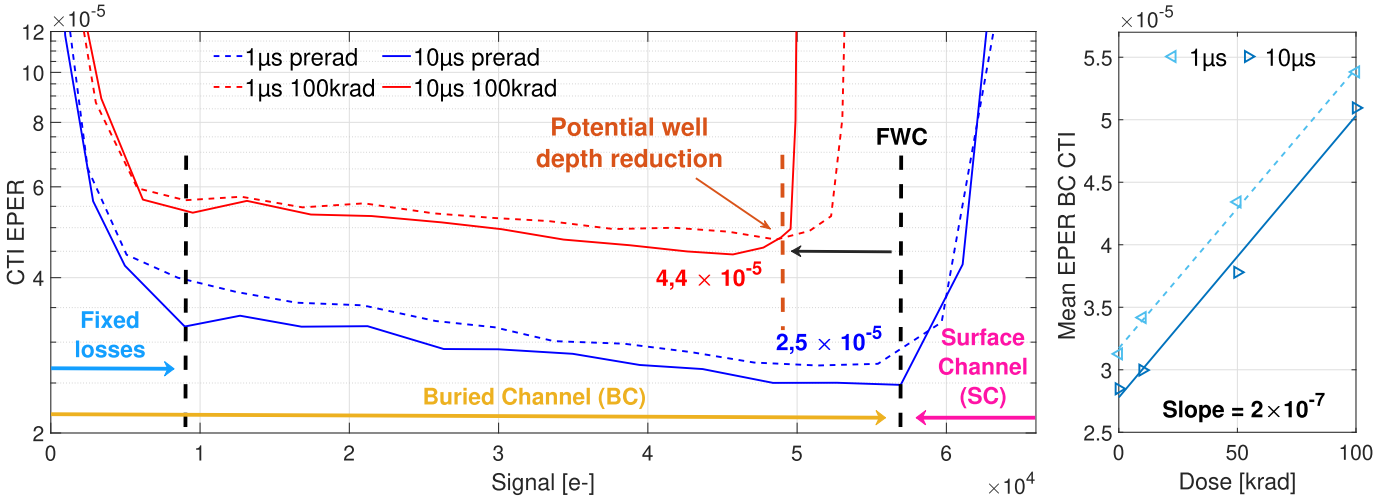


Fig. 10. CTI by EPER is plotted with respect to increasing signal injection on a semilog scale to show distinctly the CTI variation in between both 1 and 10 μs clocking setup and for different irradiation levels. The values are individually averaged 1000 times to reduce probing errors and reduce temporal noise. The different transfer regimes are identified and TID effects are visible on both the buried channel and the surface channels. The BC CTI increases with TID in both 1 and 10 μs cases following a 2×10^{-7} slope. SC CTI is shifted to lower signal injection inducing an FWC reduction, seemingly more important in the 10-μs case.

TID. This observation correlates with the hypothesis of a flat bottom well effect induced by bulk traps [18]. At around 58 ke-, charge transfer switches from a buried storage regime (BCCD) to a surface storage regime (SCCD) promoting charge loss by surface trapping. This transition is induced by the total accumulated charge in the channel that eventually balances the potential well, thus allowing the Si-SiO_2 electric field to attract the free electrons at the interface [3]. This specific amount of signal is referred to as the optimum FWC and corresponds to a quasi-flatband regime.

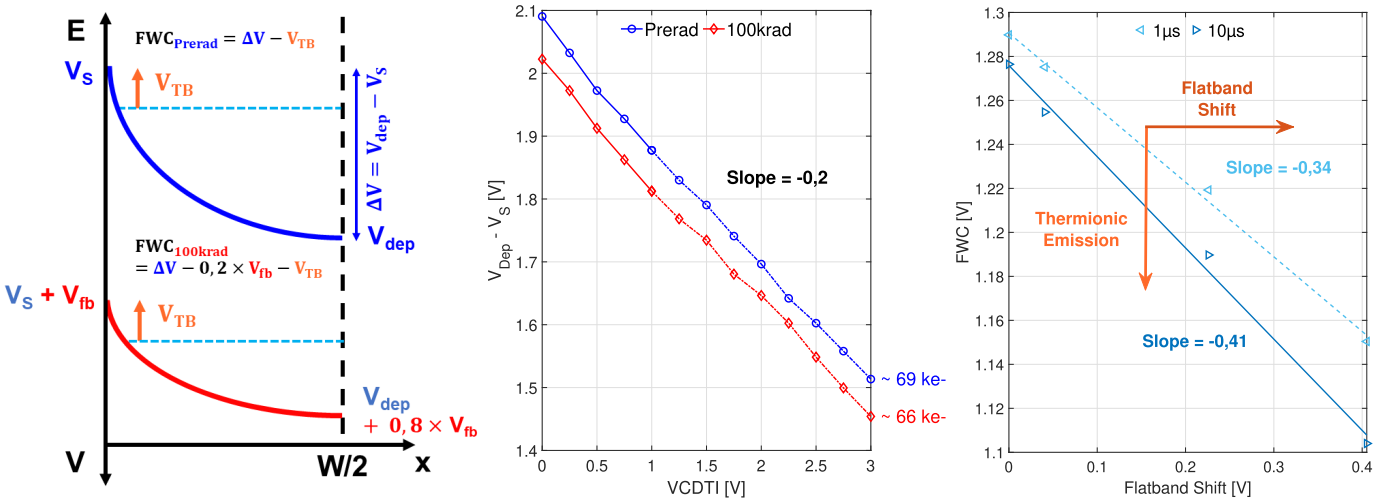
Regarding TID effects, CTI increases steadily as surface trap density is enhanced meaning more electrons are being delayed by the trap capture-release mechanisms. Mean buried channel CTI values are ranging from 2.5×10^{-5} prerad up to 4.4×10^{-5} at 100 krad yielding a 2×10^{-7}/krad deterioration slope. Even so subtle, this CTI degradation is unexpected in the buried channel as the parabolic potential shape (introduced in Section II) prevents the electron packet to interact with the interfaces. Moreover, the capture processes are limited by the hole passivation layer canceling the interface traps. However, electrons flow through the TCDTI during transfer where the potential well depth is much smaller than in the finger as calculated in (3). For charge packets over 4 ke-, interface contact is possible although on a very small surface with regards to the complete register. This may contribute to the CTI increase observed in the buried channel. CTI measured with a 1 μs clocking setup is also plotted on Fig. 10. Despite fewer traps activated, CTI is slightly degraded when compared to the 10 μs measure. The slight rise in CTI could be explained by the increased slew rate of the transfer clock edges. In particular, at the very end of the transfer, long falling edge times help transfer the last remaining electrons by thermal diffusion. Charge transfer degradation due to reduced falling and rising edge times has already been observed on CCDs [8] and CCD-on-CMOS structures [19].

D. Full Well Charge

FWC on the other hand is very neatly affected by TID and transfer duration. Fig. 11(a) represents the mechanisms at play. The loss of FWC is a combined consequence of flatband shift induced by TID and thermionic emission. As seen in Section IV-A, flatband shift engenders a reduction of the potential well depth $V_{\text{dep}} - V_s$ hence a switch to the surface regime at lower FWC. According to the potential well depth estimated from Fig. 6, FWC should follow a $-0.2 \times V_{\text{fb}}$ trend as can be seen on Fig. 11(b). On top of this, the surface regime is expected to be reached a few hundred of mV before filling completely the potential well. This threshold corresponds to the thermal potential barrier V_{tb} at ambient temperature that electrons are able to overcome with their thermal energy kT. In the literature, values of 0.3 mV are reported in the case of surface thermal barrier [20]. Quite obviously, the quantity of electrons escaping the potential well scales with the time spent during transfer [21]. On Fig. 11(c), the experimental FWC values for 1 and 10 μs transfers indeed exhibit a clear difference. However, instead of following the expected -0.2 trend with flatband shift, it appears the surface capture of electrons intensifies which has the effect to induce a larger FWC decrease. One way to explain such an effect is to assume that the capture probability of a thermally excited electron is yielded by the amount of unpassivated interface traps. Therefore it follows that electrons are more likely to escape the potential well and find a trapping site with increasing TID-induced interface traps. The level of interface passivation must then be accounted for with regard to the transfer duration. Considering only the hole emission time constant, the probability of a trap getting emptied is as follows:

$$P_e = 1 - e^{-\frac{\text{PW}}{\tau_e}} \tag{8}$$

τ_e for midgap traps is obtained from (7) and is equal to 25 ms. PW $= 10$ μs yields a probability of 4×10^{-4} whereas for



(a) (b) (c)

Fig. 11. (a) Schematic of the potential well in the prerad and 100-krad case. It is represented by both flatband shift and thermal barrier effects on FWC. (b) Potential well depth $V_{dep} - V_s$ extracted from the potential barrier measurement. Over 1 V plotted data are extracted half from the experimental measure, the other half from a linear extrapolation. The potential depth follows a -0.2 trend versus VCDTI. A similar trend is observed in (c) where the optimal FWC measured in Fig. 10 is plotted with respect to flatband shift. FWC values are shifted down compared to the estimated potential well depth because of the potential barrier. The 10 μs clocking setup exhibits a more accentuated FWC loss with TID.

TABLE I

STATE-OF-THE-ART CCD-ON-CMOS COMPARISON

	This work f = 10 kHz, PW = 1 µs				**Marcelot et al. TED 2015 [22]**		**Boulenc et al. ICSO 2016 [23]**	**Pratlong et al. ICSO 2018 [24]**
Pixel size (µm × µm)	12×3				1,3×1		5×5	5×5
TID Source and Biasing	X-ray tungsten tube / Biased				X-ray source / Unbiased		-	-
TID	Prerad	10 krad	50 krad	100 krad	Prerad	100 krad	-	-
FWC (ke-)	58.6	57.9	55.4	52.3	-		20	30
Flatband Shift (mV)	0	41	226	405	-		-	-
Noise (e-)	7	8	11.3	13.5	-		20	12
Dark current at RT (nA/cm^2)	0.28	0.31	0.46	0.79	0.24	1.43	3.5	3.7
Dynamic range (dB)	78.4	77.2	73.8	71.8	-		60	68
Mean EPER CTE	0.999971	0.99997	0.999962	0.999949	0.9992	0.9976	>0.99995	>0.99999

PW $= 1$ μs the probability is 4×10^{-5}. For any other trap energy, since PW is small compared to τ_e, the hole emission is always roughly ten times less likely for PW $= 1$ μs compared to PW $= 10$ μs. On the other hand, once a trap is emptied from a hole, the electron capture is almost instantaneous (few ns) meaning the capture rate is almost systematic. As such, it is presumed that the amount of trapped electrons scales also with P_e. Following similar reasoning, rather than direct thermionic emission, trap-assisted tunneling can also be considered as a good candidate to explain the observed FWC variations with transfer duration and N_{it}. Furthermore, investigations could also highlight the role of positively charged interface traps (involved in the threshold shift) further shifting the surface potential.

As a conclusion of this section, by putting in correlation the value of 4.1 mV/krad found in Section V-A with the FWC loss observed on the CTI measure (Fig. 10) we find a trend that cannot only be explained by the potential well depth reduction. Trapping occurs at the onset of filling the potential well, at a threshold defined by a thermal barrier, which has the consequence to precipitate prematurely the transfer into a surface regime. It is postulated that the probability for an electron to get trapped at the interfaces is enhanced for a long time spent unpassivated and for increased surface trap density. Therefore, using fast transfer clocking presents the following assets: 1) charge transfer is enabled with no critical CTI deterioration and 2) FWC reduction is mitigated by preventing surface regime to happen before getting close to filling the potential well. Accordingly, it is a good trade-off when considering also 3) dark current mitigation.

V. CONCLUSION

The electrical properties of an innovative CDTI-based CCD-on-CMOS have been described for space environment by use of dark current, CTI, and flatband shift measurements with respect to TID. The device shows good radiation tolerance with a short phase aperture time, capitalizing both on MPP operation and dynamic suppression of dark current. It was proven that with a pulse duration of 1 μs charge transfer remains efficient with a CTI $\leq 10^{-4}$ at 100 krad at 75% of the prerad FWC. Overall results are competitive when compared to state-of-the-art CCD-on-CMOS devices relying on classical planar architecture as can be seen in Table I. The contribution of the new CDTI architecture can be seen on FWC and hence on the dynamic range thanks to an improved buried channel. The FWC density on the tested device is 1.6 ke-/μm^2 which

appears to be lower than on [2] (2.6 ke-/μm^2). It is nevertheless a significant improvement when compared to MPP CCDs (n-MPP and p-MPP) limited in well capacity because of the doping implant under the gates. Dark current, which was to be expected due to the large area of interface states introduced by the CDTI, is efficiently contended. It must be pointed out that the measured values in prerad conditions are above the dark current level reached in recent MPP CCD, which are more toward a few pA/cm^2. Concerning TID effects, the device shows a weak dark current increase comparable to that of state-of-the-art Rad-Hard MPP-CCDs [11] and exhibits benefits inherited from the CMOS technology such as thin oxides and high-quality silicon bulk leading, respectively, to weak flatband shift (4.1 mV/krad) and high CTE. This CCD-on-CMOS device also presents the possibility to be integrated along with any CMOS function on a chip with a low power supply. This work shows that CDTI does not exhibit critical weaknesses that would prevent their use in a radiation environment.

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