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Design and Optimization of an Integrated Modular Motor Drive for Low Voltage High Power Permanent Magnet Synchronous Motor

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Keywords

«Integrated motor drives», «DC-AC converter»,
«Design Space Optimization», «Decentralized
control structure», «Electric Vehicle».

Abstract

This paper presents a design of an Integrated Modular Motor Driver (IMMD) for an open-winding permanent magnet synchronous motor (OW-PMSM). A losses calculation method to validate both electrical and thermal design is proposed. Loss calculation method takes account of losses in both transistors and conductors. Obtained calculation results are compared with experimental results to validate the proposed losses calculation method. Observed losses discrepancy between the proposed method and experimental measurements is 3.6 %. Maximum efficiency of IMMD prototype is measured at 97 % for an output power of 1.63 kW.

Introduction

For several years, sales of electric vehicles have been growing rapidly over the world. The higher power density requirements have challenged the manufacturing methods of permanent magnet synchronous motors (PMSM). In these applications, the supply voltage is limited by the battery and the speed can exceed 6,000 rpm for an

ever-increasing torque demand. The resulting high phase currents force manufacturers to increase the conductor cross-section. This implies a reduction in the winding turn number and a lower fill factor [1], which leads to higher losses. In addition, the increased wire diameter is responsible for additional Joule losses due to the skin effect. Existing solutions consisting of dividing the windings into several parallel wires imply technological difficulties for large-scale industrialization (burying in the slots and soldering the connections).

Several solutions are possible to overcome the winding challenges and gain power density. The most common method, doubling the battery voltage, reduces the current in the motor windings and increases the motor power in the flux-weakening region. However, the motor design becomes more complicated because of the additional insulation required to limit partial discharges [2]. A second method found in mid to high-end cars is to use multiple motors to power the vehicle such as the Tesla Model S dual motor or the Koenigsegg Gemera.

However, another method is to increase the number of phases in the motor. In applications where the supply voltage is limited, polyphase motors are a solution to reduce the phase current. In this case the diameter of each conductor is reduced, which increases the copper fill factor of the stator and thus the efficiency of the motor. In

addition, the increase in the number of phases in PMSMs leads to better reliability [3].

To further improve the reliability of multiphase motors, the windings of each phase are divided into subgroups and driven by different converters. The most reliable system is achieved when each winding is supplied independently by an inverter. However, such electric motors must be powered by specific converters. These converters can be integrated into the motor to improve the power density of the drive system and are called Integrated Modular Motor Drivers (IMMD).

In the literature, many works present prototypes of multiphase motors powered by IMMD [4-9]. However, none of them were designed to independently drive the coils of an open wound permanent magnet synchronous motor (OW-PMSM), with a full bridge inverter. To highlight the benefits of IMMDs for OW-PMSMs over conventional three-phase motors, the IMMD presented in this document was designed to drive a 48 V 85 kW PMSM. At this voltage, the power of the three-phase PMSM hardly exceeds a few tens of kW with a good efficiency because of the winding limitations mentioned earlier.

Presentation and requirements of the IMMD

The IMMD presented in this document is designed to drive an OW-PMSM consisting of n phases, with p coils per phase, which represents a total of np converters. Each converter consists of a power board, a control board and a heatsink, and the entire IMMD must fit within the stator diameter of the electric motor, which is 180mm. Each module of the IMMD will have to fit in a sector with the same angle as the stator pitch and a maximum length equal to the motor radius.

Figure 1 shows a profile view of the electrical powertrain. The IMMD will be mounted on the rear flange of the motor and the stator coils will be soldered directly to the IMMD PCBs. The heatsink and PCBs are parallel to the z-axis and the dimensions are bounded by the maximum distance between the opposite side of the triangle and the hypotenuse. The position of the module elements on the y-axis impacts their maximum length. The further the elements are far from the base of the triangle, the more the length decreases.

To maximize the integration, the converter will be divided into 2 overlapped boards: One for the control circuit and one for power components (as close as possible from the heatsink). The

thickness of the heatsink, the PCBs and the distance between the control and power board therefore determine the maximum length of the heatsink and PCBs. The length of the PCBs in the x-axis is not constrained, but it does affect the total volume of the IMMD and thus the power density. As the copper-colored power connectors are offset from the control board and heatsink in the x-axis, they do not collide with adjacent modules.

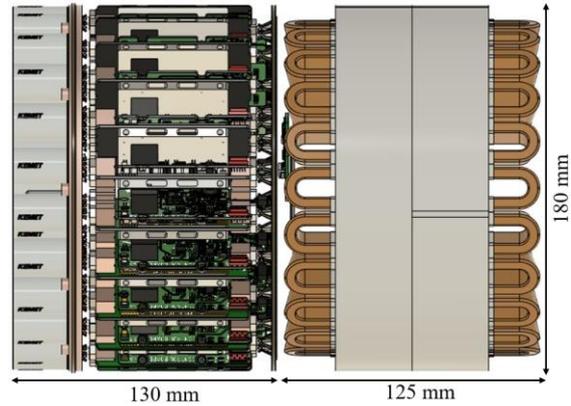


Fig. 1: 3D CAD of the IMMD and OW-PMSM.

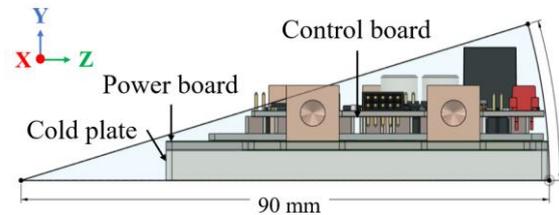


Fig. 2: Integration layout of an IMMD module.

The mechanical power and torque curves obtained from the finite element simulation of the polyphase OW-PMSM are presented in Figure 3.

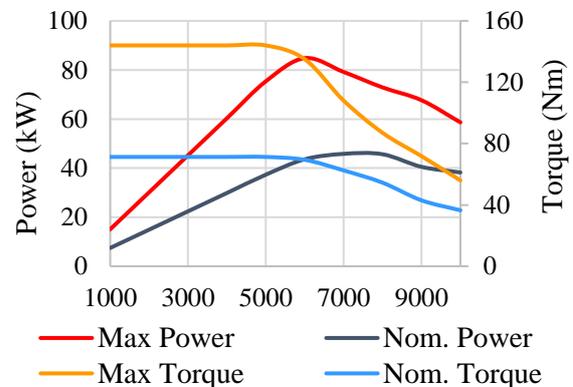


Fig. 3: Mechanical output power and Torque for nominal ($65 A_{RMS}$) and maximal ($150 A_{RMS}$) phase current versus rotor speed.

According to the results, each converter will have to provide a nominal electrical power of 2.2 kW and a maximum power of 4.1 kW for 30 seconds which represent a maximal current of 150 A_{RMS}. Phase voltage, current and load phase angle are calculated for each points of the mechanical power curves. This values are used to calculate the inverter's operating point.

Converter design

The DC-AC converter has been designed to minimize losses, i.e., maximize efficiency, while ensuring module integration and motor control. The losses considered in the calculation of the efficiency are the following:

- MOSFET conduction and switching losses.
- Body Diode conduction and switching losses.
- Power PCB DC and AC traces losses.

The transistors chosen for this study are the BSC021N08NS5 (Si technology) because they have the lowest R_{DS(on)} MOSFET in TDSO-8 package. SiC or GaN transistors are not selected because they do not exist in compact packages or can't withstand the maximal current. Furthermore at low frequencies, Silicon MOSFETs are more efficient than GaN, thanks to their lower R_{DS(on)} [10]. The latest power MOSFET technology for low voltage applications enables significant performance with greatly reduced R_{DS(on)} and Q_G. Last but not least, For IMMDs powering OW-PMSMs, the amount of transistor needed is too great for GaN to be a cost-competitive solution.

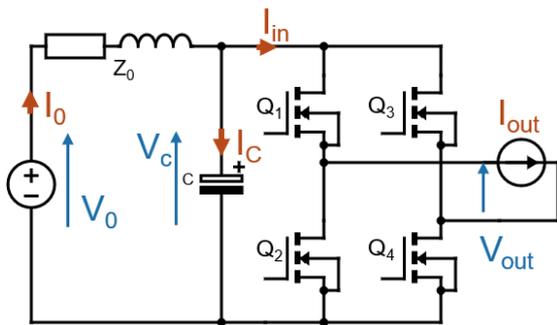


Fig. 4: Circuit diagram of the inverter.

The circuit diagram for one IMMD converter presented in figure 4. The voltage V₀ is fixed by the battery voltage at 48 V, while the output current I_{OUT}, the output voltage V_{OUT} and the

phase between the first harmonic I_{OUT-(0)} and V_{OUT-(0)} are fixed by the motors. The output current and voltage can be adjusted to calculate the inverter losses for different operating points. The control of the MOSFETs is achieved using unipolar modulation (UPWM) as detailed in Figure 5. The switching of the transistors is shifted by 180 degrees between the two legs of the bridge, which doubles the switching frequency seen by the load. As a result, the current ripple in the motor and therefore the ripple torque can be greatly reduced without increasing switching losses in the converter.

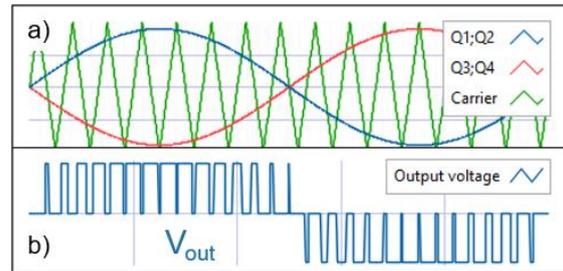


Fig. 5: a) Modulation and carrier waveforms and b) Output voltage V_{OUT} for UPWM.

Inverter power losses calculations

The calculation is based on the method presented in [11] which provides a mathematical tool for the calculation of power losses in MOSFET-based power electronics converters. To optimize the losses, each switching cell is composed of *n* MOSFETs in parallel. The conduction losses being proportional to the square of the drain current I_{DS}, increasing *n* allows to reduce the conduction losses but the surface of the switching cells increases as well as the required gate current. This leads to an additional volume of the IMMD modules and a reduction of their volume density. The best compromise between the reduction of the losses and the routing surface has been evaluated. The use of two transistors in parallel reduces the total losses by 25 % compared to a single MOSFET, for an output current of 65 A_{rms}. This difference reach 49% for 150 A_{rms}. The power losses in the inverter are calculated for different output current values. The equivalent R_{DS(on)} of a switching cell being constant, for a given junction temperature, the conduction losses are plotted as a function of the output current in figure 6. They represent 1.1 W per MOSFET at 65 A_{RMS} and 5.93 W at 150 A_{RMS}. The switching losses depend both on the switching frequency of the transistor and the drain to source current. They

are plotted on figure 6 for a PWM frequency of 25 kHz. Calculated switching losses are higher than the conduction losses at this frequency which reduces inverter efficiency. Reducing the switching frequency would increase inverter efficiency. However, in the case of the multiphase OW-PMSM with low phase impedance, reducing switching frequency can degrade the motor efficiency, control, and performance of the motor due to the output current ripple. In addition, reducing the switching frequency requires increasing the capacitance value of the DC-link capacitor to smooth the DC bus voltage.

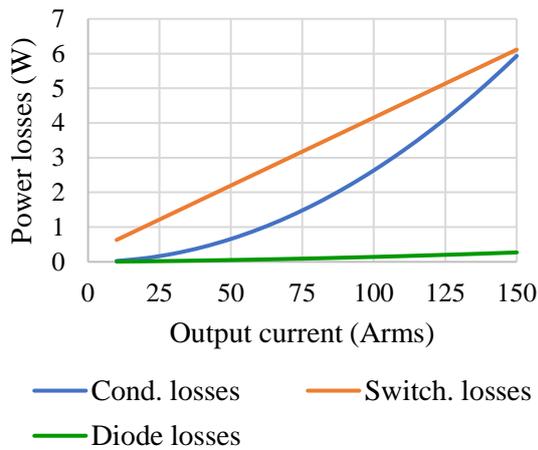


Fig. 6: Detailed losses in a switching cell as a function of output current for 25 kHz of PWM frequency.

DC-link capacitor design

To guarantee a stable supply voltage for the IMMD inverters, it is necessary to add a capacitor bank at the converter input. In the case of an IMMD, the proper sizing of the DC-link is crucial since capacitors represent up to 30% of the total volume of the IMMD [12]. The DC-link's objective is to filter the AC currents draw from the inverter. The sizing of the DC-link capacitors can be done analytically based on the modulation index and load phase angle [13]. The input current I_{IN} of the converter has three relevant components: a DC component, a low frequency AC current at twice the fundamental frequency and a high frequency component at the switching frequency. In a single-phase inverter, filtering the low frequency component requires a high value capacitance which means a considerable size capacitor. However, by increasing the number of phases n and the number of parallel converters p in an IMMD, the capacitance required to filter the currents can be reduced considerably [14] [15].

The total current in the DC bus is equal to the sum of the input currents of each inverter. In an IMMD with n , p inverters, there are p identical I_{IN} currents and n I_{IN} currents that are equal in magnitude but phase-shifted. It is possible to further reduce the size of the DC-link by using an interleaving method to control the p inverters of a same phase. However, this method will not be used because of IMMD's fully decentralized structure.

Using the current harmonics calculation method detailed in [13], a Fourier analysis has been done on the total current in the IMMD DC bus. The waveforms for the input current obtained in the circuit detailed earlier are shown in Figure 7a and the IMMD DC bus current is shown in Figure 7b. The results show that the low frequency current at twice the fundamental frequency has disappeared by connecting all the converters to the DC bus. The resulting current has a DC component and even harmonics, whose first harmonic is equal to twice the switching frequency.

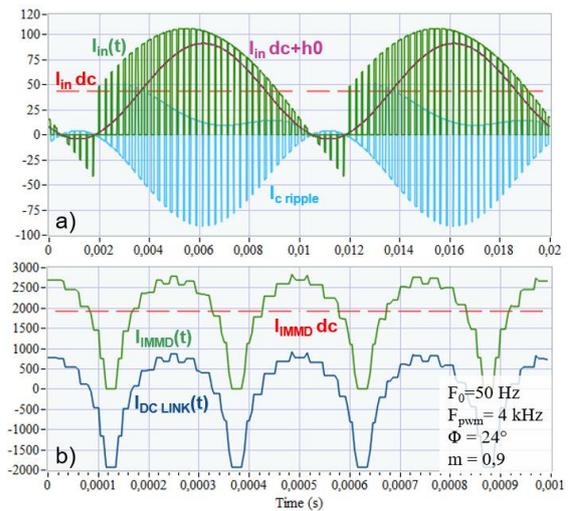


Fig. 7: a) Waveforms of the input current and its three components: the DC current $I_{IN DC}$, the double fundamental frequency harmonic $I_{IN H0}$ and the high frequency ripple current I_C . b) Waveforms of the total current I_{IMMD} in the IMMD with its average value and the current ripple $I_{DC LINK}$.

The aim of the DC-link will be therefore to filter the calculated DC bus current harmonics. From the switching frequencies selected in Figure 6, the frequency of the first harmonic will be in the worst case at 50 kHz, for a 25 kHz PWM frequency. By changing the modulation index and the load phase angle, the IMMD current ripple can be calculated for the worst-case $\phi = 0^\circ$ and $m = 0.5$. The RMS ripple current value in one

converter at maximum power is $57.5 A_{RMS}$ for a dc current I_{DC} of 50 A. For a peak-to-peak ripple voltage of less than 2 % of the nominal battery voltage and a PWM frequency equal to 25 kHz, the minimum capacity required is $750 \mu F$ per converter. As each board embed a part of the total DC-link capacitor, the converter DC-link capacitance is equal to the total capacitance divided by the number of converters. Double the switching frequency allows to halve the required capacity but the losses at nominal operating point increase by 66 %.

For the DC-link, the capacitors chosen are PHH227MLL3800, which are High CV conductive polymer hybrid capacitors. These capacitors can supply a continuous ripple current of $36 A_{RMS}$ for a capacity of $800 \mu F$. These capacitors are mounted on a busbar supplying each IMMD module. According to the surface area available on the busbar, it is possible to integrate up to 33 capacitors for a total capacity of 26.4 mF. The IMMD DC-link is shown in the figure 8.

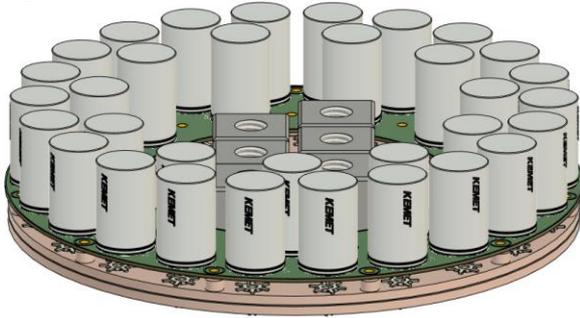


Fig. 8: 3D CAD of the proposed IMMD DC-link capacitor. Capacitors are mounted on a PCB connected to the IMMD DC side busbar.

Using the motor's electrical parameters, the DC bus voltage ripple is calculated for the nominal and maximum operating points as a function of speed. As shown in Figure 9, the maximum voltage ripple is at 3000 rpm. At this speed, the modulation index is close to 0.5 and the phase ϕ is at 31.2° and 40.8° respectively for nominal and maximum power. At rated power, the maximum voltage ripple is 0.77 % and at maximum power it is 1.55 %. In addition, the maximum current ripple for each inverter is $45 A_{RMS}$, while the DC-link capacitors can supply a total of $52 A_{RMS}$ per module.

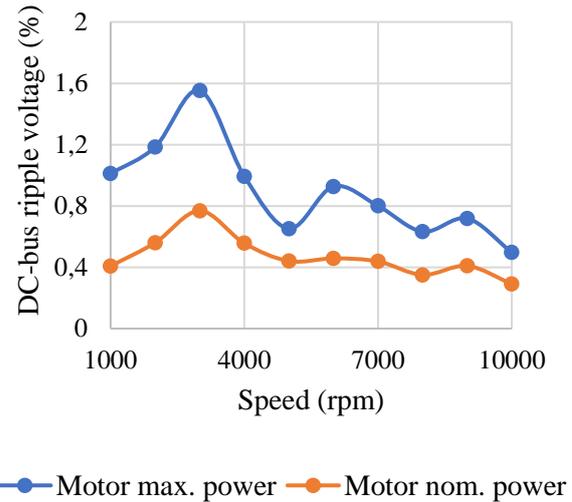


Fig. 9: Peak-to-peak ripple voltage of the IMMD DC bus. Each point is calculated based on the motor's operating points.

PCB Traces losses Calculation

The high currents flowing in the traces of the power PCB generate Joule losses. These losses are even greater in the case of a high-current integrated converter, where the trace width and dissipation area are limited. In addition, the currents flowing in the converter traces are composed of multiple high-frequency harmonics due to the fast switching of the MOSFETs. Due to the skin effect and the proximity effect, the current is distributed unevenly in the conductor, which increases its effective resistance. This results in additional losses in the PCB traces [16]. To evaluate the conductor losses, trace impedances of the power PCB must be characterized and a frequency analysis of the currents in each mesh of the circuit must be performed. The method used to calculate the losses in the tracks is described in Figure 10. The FEM calculation was performed on the power board from the 3D CAD file shown in Figure 11. The impedance of each mesh was calculated between the connectors and pads of the MOSFET.

For each traces m , the harmonics h of the currents flowing in it were extracted and the impedance of the trace was interpolated for these frequencies f . The total losses in the power PCB are the sum of the losses of each track m for each current harmonic h , as described in formula (1). The losses in a m trace for a frequency f corresponding to the harmonic h of current $I_{M,H}$ are the product of the resistance $R_{M,H}$ and the square of the current.

$$P_{\text{traces}} = \sum_m \sum_h R_{m,h}(f) \cdot I_{m,h}(f)^2 \quad (1)$$

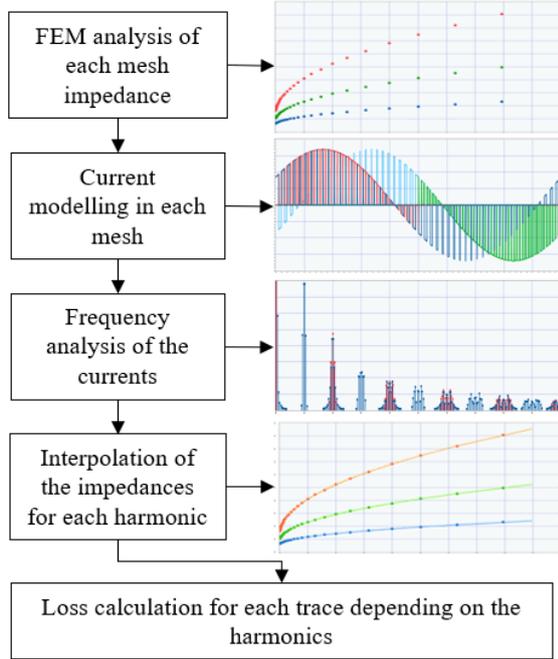


Fig. 10: Method used to evaluate the losses in the power PCB traces.

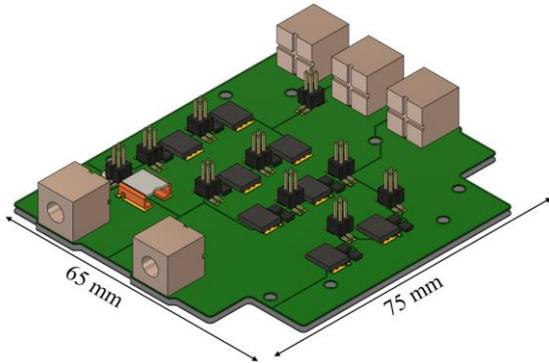


Fig. 11: 3D CAD of the power board of the inverter module.

In Figure 12, the trace losses have been calculated as a function of the output current for different switching frequencies. The difference between the curves confirms the role of the harmonics in increasing the losses. However, the additional losses are small, as increasing the output switching frequency from 10 kHz to 100 kHz only increases the losses in the traces by 17%. However, the losses in the inverter conductors are not negligible as they represent 34% of the total losses at 65 A_{RMS} and 47% at 150 A_{RMS} .

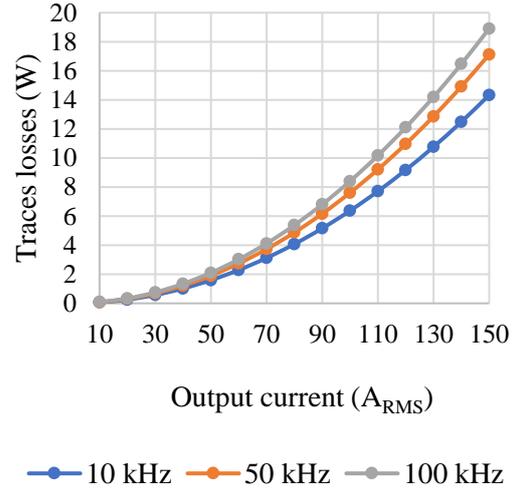


Fig. 12: Power losses in PCB traces, depending on the output current for different output switching frequencies.

Thermal modelling of losses

The last step in the IMMD sizing process is to validate the ability of a module to evacuate its losses. For this purpose, the steady-state heat dissipation was evaluated by constructing the equivalent thermal circuit of the IMMD module, shown in Figure 13. Each resistor in the model corresponds to the thermal resistance opposing the heat flow in the different layers of the system. The resistances for each layer were calculated using formula (2) by dividing the thickness e by the surface area S and the thermal conductivity coefficient of the material λ .

$$R_{\text{th}} = \frac{e}{\lambda S} \quad (2)$$

The copper thermal resistance of the PCB traces was separated into two resistances $R_{\text{TH CU1}}$ and $R_{\text{TH CU2}}$. $R_{\text{TH CU1}}$ is the thermal resistance associated with the copper surface under the MOSFETs to add the contribution of the trace losses P_{TRACES} , to the transistor losses P_{INV} . To simplify the model, it is assumed that heat is transferred vertically to the fluid and that there is no horizontal heat transfer in the layers except in the Al layer corresponding to the PCB substrate which is made of Aluminium. The layers corresponding to $R_{\text{TH JC}}$, $R_{\text{TH SN}}$ and $R_{\text{TH CU1}}$ have the same area S_1 corresponding to the contact area of the transistor. The resistors in the $R_{\text{TH ISO}}$, $R_{\text{TH AL}}$, $R_{\text{TH TIM}}$ and $R_{\text{TH CP}}$ layers use an S_2 area which corresponds to the PCB surface. The resistor $R_{\text{TH CU2}}$ uses an area which is the difference between the areas S_2 and S_1 .

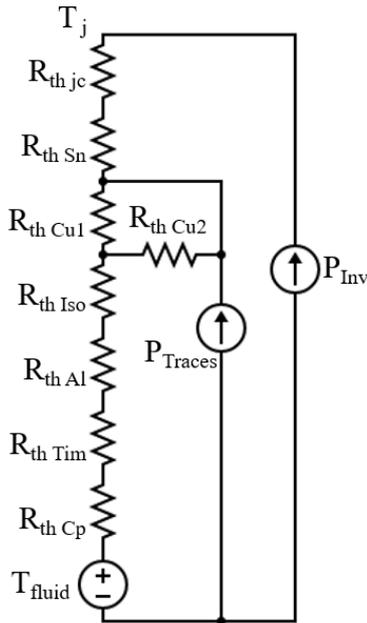


Fig. 13: Equivalent thermal circuit of the power PCB and heatsink.

The thermal gradient, shown in Figure 14, was calculated under worst-case conditions, for the maximum operating point and a fluid temperature of 60 °C. The temperature between two nodes of the model, i.e., across a thermal resistor, was calculated with formula (3). The result is a temperature difference of 37 °C, which gives a T_j of 97 °C. The maximum temperature T_j of the MOSFETs specified in the datasheet is 175 °C, so the thermal dissipation is sufficient to evacuate the losses from the converter.

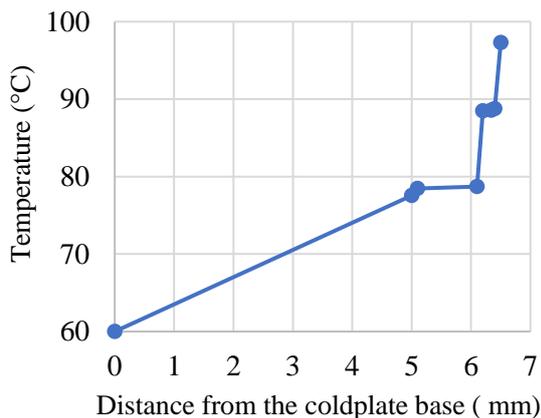


Fig. 14: Temperature gradient of the thermal model, calculated for the worst case ($I_{OUT} = 150 A_{RMS}$, $F_{PWM} = 25 kHz$, $\phi = 0^\circ$ and $m = 1$) Each point corresponds to the temperature of a node in the model.

$$T_B = \frac{P_{AB}}{R_{th AB}} + T_A \quad (3)$$

On the thermal gradient, the most important temperature variations are in decreasing order on: $R_{TH JC}$, $R_{TH ISO}$, $R_{TH TIM}$ and $R_{TH CP}$. While it is not possible to change $R_{TH JC}$, it is possible to modify $R_{TH ISO}$ by choosing an IMS PCB with a better thermal conductivity for the insulating layer. For $R_{TH TIM}$, there are different types of thermal pastes with lower thermal resistances that can be applied in thinner layers. Finally, $R_{TH CP}$ can be reduced by improving the exchange coefficient of the cold plate.

Experimental results

Experimental measurements have been performed on the prototype IMMD module. The test platform is detailed in Figure 15. The converter is powered with a 48 V 3 kW power supply and loaded with an adjustable RL load. Four gate signals are generated by a sinusoidal UPWM modulation implemented on FPGA, allowing to control the inverter. Currents and voltages are measured at the input and output of the inverter.

Measured Currents and voltages obtained during operation are presented in figure 16. As only one phase of the IMMD was tested, there is a current ripple on the DC bus at twice the fundamental frequency. A 60 DC-link capacitor where used to reduce the input ripple voltage. The PWM voltage at the output of the inverter is digitally filtered to extract the fundamental to measure the phase relative to the output current. The modulation index is set by the PWM generator, while the amplitude and phase of the output current depend on the RL load.

To validate the inverter loss calculation, the efficiency of the inverter was measured using a Power Analyzer LMG671. The results obtained are presented in Figure 17. The inverter was tested at 4 different operating points for a fixed switching frequency and load impedance. Data and signals obtained were then used to recalculate the losses and thus compare the calculated efficiency with the measured efficiency.

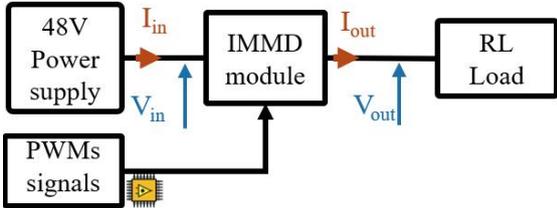
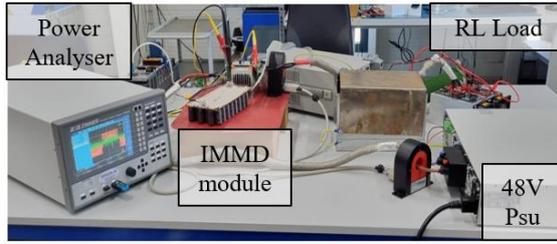


Fig. 15: Image of the converter efficiency measurement platform and system diagram.

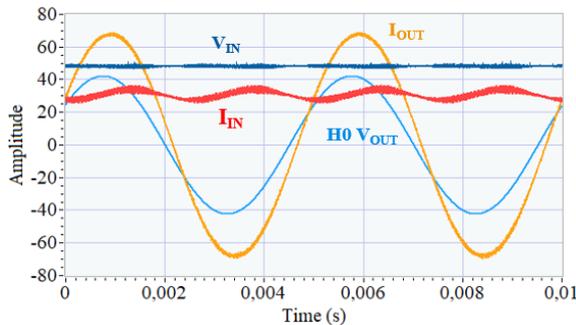


Fig. 16: Waveforms measured on the inverter in operation for $I_{OUT} = 48 A_{RMS}$, $F_{PWM} = 25 \text{ kHz}$, $\phi = 11.14^\circ$ and $m = 1$.

The maximum difference in efficiency between the two methods is 0.2 points, which represents a 3.6 % difference between measured and calculated losses. Calculated losses are lower than measured losses up to $90 A_{RMS}$. Above that, calculated losses are higher. This means that current-proportional losses, such as conduction losses in the inverter and traces, are overestimated by the model, compared to experimental measurements. There are several possible explanations for this difference. Firstly, the $R_{DS(on)}$ used in the calculation is the maximum value given by the datasheet. Secondly, there is uncertainty about the resistance value measured on the power connectors. For low current values, calculated losses are lower than measured ones. In this case, conduction losses are lower than switching losses. This difference can be explained by an underestimation of switching losses, caused by a discrepancy between actual and calculated switching energy.

Over the whole set of measurements, the maximal efficiency of 97 % was measured for the nominal current, for a load phase angle of 15.4° and a

PWM frequency of 25 kHz. Increasing the switching frequency to 70kHz reduces inverter efficiency to 96 %, for the same operating point.

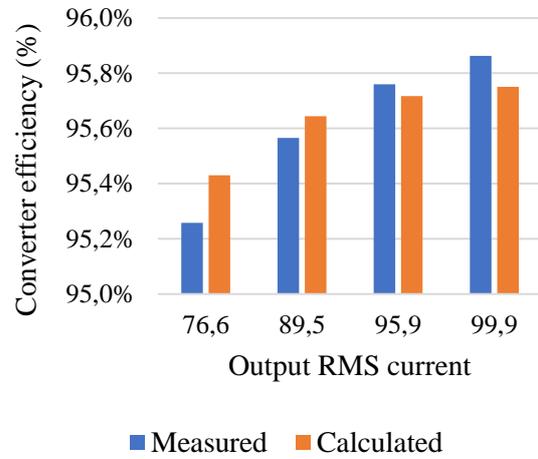


Fig. 17: Comparison of the inverter efficiency measured with the power analyzer and calculated with the proposed method, for different output current values I_{OUT} , for $F_{PWM} = 25 \text{ kHz}$ and $\phi = 24,6^\circ$.

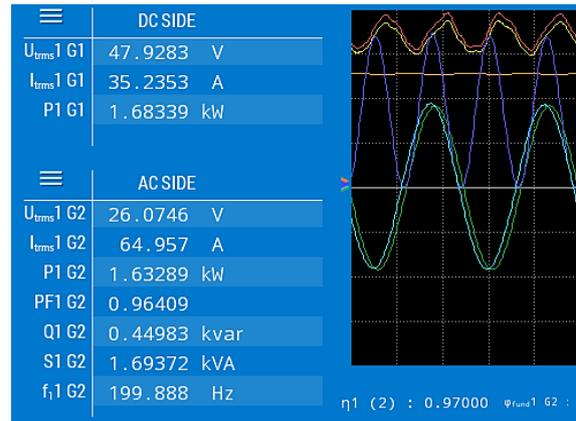


Fig. 18: Measurements made with the power analyzer for $I_{OUT} = 65 A_{RMS}$, for $F_{PWM} = 25 \text{ kHz}$ and $\phi = 15.4^\circ$. The green and blue plots are the current and the fundamental of the output voltage respectively.

Conclusion

An IMMD design for high current, low voltage multiphase OW-PMSM has been presented, based on the motor electrical requirement. The losses calculation in the selected transistors was performed using a calculation method based on the transistor parameters from their datasheet. The proposed method for calculating the losses in the traces allowed a fast evaluation of the losses in the conductors, while considering the skin and proximity effects. A simple thermal model of the

converter was used to estimate the junction temperature of the transistors from the calculated losses and thus validate the thermal dissipation. Experimental tests were carried out on a prototype inverter of IMMMD, with a maximal output power of 2.9 kW. Inverter efficiency was measured at a frequency of 25 kHz up to 100 A_{RMS}.

The measured efficiency of the prototype is 97 % at the nominal operating point for a switching frequency of 25 kHz. The efficiency discrepancy observed between the experimentation and the proposed method is 0.2 points which represent an error of 3.6%. This discrepancy is due to a difference between the values of the parameters used to calculate losses and the actual values.

As a result, the proposed calculation method can be used to calculate the losses to be dissipated from the transistor datasheet and therefore to better design the power converter heatsink. By characterizing the inverter parameters more precisely, it is possible to improve the accuracy of the results obtained.

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