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Keywords

"Resonant converter", "High frequency power converter", "Gallium Nitride (GaN)", "Lighting", "High power density systems".

Abstract

This paper presents the design of a 100W 1MHz single-switch GaN-based resonant converter for high power density LED driver. The proposed prototype is based on the class E topology and performs Zero Voltage Switching (ZVS) as well as inherent Power Factor Correction (PFC) capability. The design procedure using analytical equations is detailed. A high frequency model of the converter including PCB parasitic is achieved and simulation results are confronted to measurements. The designed converter shows an efficiency of 81 % for an output power of 100W at 1MHz.

Introduction

In a today context of green energy usage, Light Emitting Diodes (LEDs) are gradually replacing incandescent light bulbs and fluorescent lamps in most of the applications. This is mainly due to their higher efficiency, robustness and their control capabilities [1]. However, the forward voltage of LEDs can vary according to several parameters such as temperature, ageing… Therefore, the most efficient solution for lighting is to use a power converter, called LED driver, that is able to regulate the current through the LEDs.

Along with the increasing use of LEDs, there is an increasing demand for efficient, compact and high power density LED drivers. Increasing the switching frequency is the most viable way to reduce the size of passive components and to increase the power density of power converters [2]. This is now enabled by the emergence of Wide BandGap (WBG) power semiconductors such as Gallium Nitride (GaN) transistors and Silicon Carbide (SiC) diodes.

As Switching-Mode Power Supplies (SMPS) are nonlinear systems, current harmonics tend to be injected to the AC grid when rectifying the grid voltage for supplying the LEDs. The IEC 61000-3-2 limits the percentage of current harmonics for LED driver with a power greater than 25W. Therefore, a Power Factor Correction (PFC) circuit is required to ensure quasi sinusoidal current absorption. The conventional two-stage of a LED driver is then given in Fig. 1 [3]. It is constituted of a full bridge rectifier converting AC to DC, a PFC DC/DC converter and a step-down DC/DC converter to supply the LEDs and possibly regulate the output current.

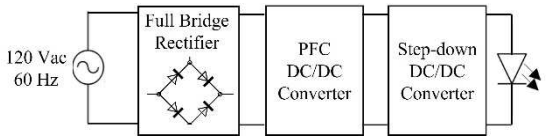

Fig. 1: Conventional 2-stage LED driver

Most of the time the PFC converter is a current source input topology controlled to absorb a rectified sinusoidal current [3], which explains the need of an additional converter in the structure to regulate the LED current. Recently, authors in [4] have shown that a resonant class E-based converter is able to perform inherent PFC function without any specific control strategy. The tested prototype uses a 1200V SiC MOSFET with a switching frequency of 90kHz. The converter shows an efficiency of 88% for an output power of 211W. Some other related works have emerged these last years. A 10W class E/F prototype operating at 200kHz is

presented in [5]. The converter achieves high power factor with an efficiency around 80%. A 50W 1MHz resonant converter based on the association of a charge pump circuit and a class DE inverter is proposed in [6]. The prototype achieves PFC functionality inherently with a maximal efficiency of 88%.

In this paper, it is proposed to design and model a 1MHz 100W single-stage LED driver based on a class E/D DC/DC converter as presented in Fig. 2. The several advantages of the proposed converter are the following:

- High switching frequency (1MHz) for higher power density capability
- Soft switching (ZVS) for reduced power losses and lower Electromagnetic Interference (EMI)
- Inherent PFC capability in order to avoid the need of an additional converter

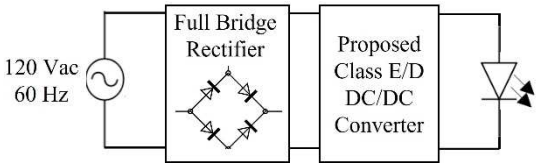

Fig. 2: Proposed LED driver structure based on a class E/D DC/DC converter

This work also highlights the importance of high frequency modeling of the power converter taking into account the effects of the printed circuit board (PCB) [7]. The proposed modeling method enables to predict the performances of the converter before manufacturing and potentially to optimize the design. An original EM-Circuit model of the proposed converter is built in this work.

The following section focuses on the characterization of a commercial 100W LED driver in order to collect the specifications for the design of the proposed converter. The third section details the design procedure of the Class E/D topology. The fourth section presents the modeling method of the designed high frequency converter by taking into account the PCB layout effects. The fifth section gives a comparison between experimental and simulation results of the proposed Class E/D DC/DC converter. Then, the performances of the proposed resonant LED driver are presented. Finally, a conclusion discusses on the obtained results and gives prospects on future work.

Characterization of a Commercial LED Driver

In order to collect some specifications for the designed power converter in this work, it is proposed to characterize a commercial LED driver with a conventional 2-stage topology. The tested converter is the XC-100W3A-HTP shown in Fig. 3. It is a 100W LED driver with a fixed average output current of 3A and an output voltage between 29V and 35V. A power factor of 0.95 and an efficiency of 90% are specified by the manufacturer. The power density is estimated to be 350W/l.

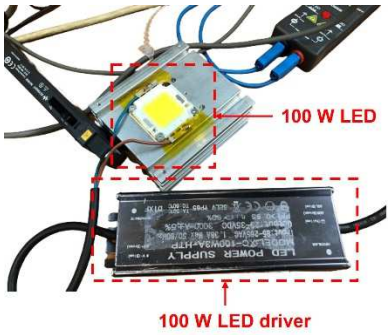

Fig. 3: Experimental test bench of the commercial LED driver

Fig. 3 presents the experimental test bench used to characterize the LED driver. A 100W LED with a nominal current of 3A is used to load the power converter. The input and output current are measured and the obtained waveforms are given in Fig. 4. The input voltage is 120V.

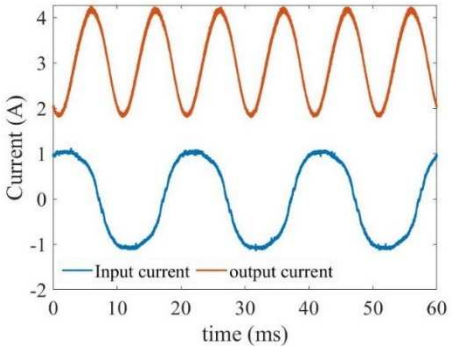

Fig. 4: Input and output current waveforms of the commercial LED driver

The experimental power factor is 0.94 and the measured efficiency is 90% which validates the specified values given by the manufacturer. The

equivalent resistance of the LED, R_{LED}, is estimated to 11Ω. This value shall be used in the design of the proposed resonant converter.

Design of the Class E/D Converter

The electrical scheme of the proposed class E/D DC/DC converter is given in Fig. 5. It is constituted of a class E inverter and a class D rectifier linked through an L-C resonant circuit.

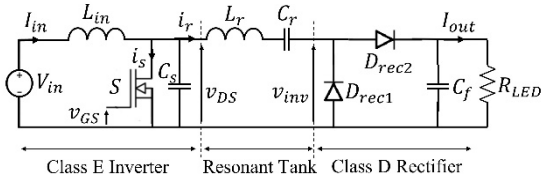

Fig. 5: Electrical scheme of the proposed class E/D DC/DC converter

This section presents the design of the resonant DC/DC converter. To achieve this goal, some design assumptions shall be made:

- The input inductance is considered large enough to consider a constant input current I_{in}
- The current i_r in the resonant L-C tank is considered sinusoidal and its rms value is noted I_r
- All components are considered ideal (no parasitic included in the design equations)

First, the class D rectifier can be modeled by its equivalent input resistance R_e expressed as in (1) [8]. Then, the electrical scheme in Fig. 5 can be simplified as shown in Fig. 6.

$$R_e = \frac{2}{\pi^2} R_{LED} \tag{1}$$

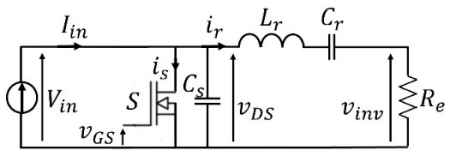

Fig. 6: Simplified equivalent scheme of the resonant converter for the class E inverter design

Then, the driving duty cycle D of the transistor is obtained by resolving equations (2) and (3) that are established to satisfy ZVS and ZVdS conditions at turn-on [4].

$$\frac{2\pi(1-D)}{cos(2\pi D+\phi)-cos(\phi)} = V_{in}\sqrt{\frac{2}{R_e P}} \tag{2}$$

$$\phi = \pi + atan\left(\frac{cos(2\pi D)-1}{2\pi(1-D)+sin(2\pi D)}\right) \tag{3}$$

Where P is the desired transferred power and ϕ is the phase shift between i_r and the switch turn-on instant.

Knowing that the average voltage of v_{DS} is V_{in}, the capacitance C_s is calculated using equation (4). This demonstration is well detailed in [4].

$$C_s = \frac{P\Delta}{V_{in}^2 \omega} \tag{4}$$

Where, $\omega = 2\pi f$ is the angular frequency at the desired switching frequency and Δ is a parameter that only depends on the duty cycle D. The expression of Δ is given in (5).

$$\Delta = \frac{(1-D)[\pi(1-D)\,cos(\pi D)+sin(\pi D)]}{tan(\pi D+\phi)\,sin(\pi D)} \tag{5}$$

The components of the resonant tank L_r and C_r are sized for a given loaded quality factor Q and using the First Harmonic Approximation (FHA) as represented by the equivalent circuit in Fig. 7. The FHA hypothesis is valid as long as the resonant current i_r is sinusoidal, which means that the power is transmitted only at the switching frequency.

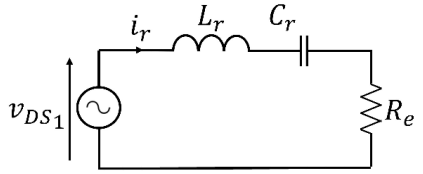

Fig. 7: Equivalent circuit of the class E output circuit using FHA

Thus, L_r and C_r are the solutions of the 2-equations system given in (6). Where V_{DS_1} is the RMS value of the first harmonic of v_{DS}. V_{DS_1} can be expressed by (7). Where γ is a parameter that depends only on the duty cycle D. The expression of γ is given through equations (8) to (12).

$$\begin{cases} Q = \dfrac{1}{R_e}\sqrt{\dfrac{L_r}{C_r}} \\ \dfrac{V_{DS_1}^2 R_e}{P} = \left(L_r\omega - \dfrac{1}{C_r\omega}\right)^2 + R_e^2 \end{cases} \quad (6)$$

$$V_{DS_1} = \frac{\gamma P}{V_{in} C_s \omega} \quad (7)$$

$$\gamma = \sqrt{\frac{\gamma_a^2 + \gamma_b^2}{2}} \quad (8)$$

$$\gamma_a = \frac{1 - cos(2\pi D) - (2\pi D + \lambda)\, sin(2\pi D)}{\pi} + \frac{\beta[2\pi\, cos(\phi)\,(1 - D)]}{2\pi} + \frac{\beta[(sin(\phi) - sin(4\pi D + \phi))]}{4\pi} \quad (9)$$

$$\gamma_a = \frac{1 - cos(2\pi D) - (2\pi D + \lambda)\, sin(2\pi D)}{\pi} + \frac{\beta[2\pi\, cos(\phi)\,(1 - D)]}{2\pi} + \frac{\beta[(sin(\phi) - sin(4\pi D + \phi))]}{4\pi} \quad (10)$$

$$\beta = \frac{2\pi(1 - D)}{cos(2\pi D + \phi) - cos(\phi)} \quad (11)$$

$$\lambda = \frac{\pi(1 - D)}{tan(\pi D + \phi)\, tan(\pi D)} - \pi(1 + D) \quad (12)$$

Finally, similarly to the conventional Boost converter, the input inductance L_{in} should be sized to limit the input current ripple ΔI_{in} as given in (13). The output capacitor C_f is sized using equation (14) to limit the output voltage ripple ΔV_{out} and ensure a constant current in the LED during the switching period.

$$L_{in} = \frac{V_{in} D}{\Delta I_{in} f} \quad (13)$$

$$C_f = \frac{D}{\Delta V_{out} f}\sqrt{\frac{P}{R_{LED}}} \quad (14)$$

For the design of the proposed converter, the power P is set to 100W, the switching frequency f is 1MHz, the input voltage is 100V (average rectified value) and the loaded quality factor Q is chosen to be equal to 7. The required passive components values and characteristics are listed in Table I.

Table I: Passive components values and requirements

	Value	Requirements
C_s	10nF	C0G, > 400V, $f_{res} \gg 1MHz$
C_r	15nF	C0G, > 400V, $f_{res} \gg 1MHz$
L_r	3.9µH	Air core, > 7A, $f_{res} \gg 1MHz$
L_{in}	100µH	Ferrite core, > 2A, $f_{res} > 1MHz$
C_f	1µF	X7R, > 100V, $f_{res} > 1MHz$

The maximal voltage $V_{DS_{max}}$ applied to the switch depends on the duty cycle as given in (15). For this application the maximal voltage is evaluated to 250V using (15).

$$V_{DS_{max}} = \frac{\alpha P}{V_{in} C_s \omega} \quad (15)$$

Where α is a parameter that only depends on the duty cycle D. To obtain the α parameter, it is first necessary to calculate the angle θ_{max} to which the v_{DS} voltage reaches its maximal value. The expressions of θ_{max} and α are given by equations (16) and (17) respectively.

$$\theta_{max} = 2\pi - \phi + \text{asin}\left(\frac{1}{\beta}\right) \quad (16)$$

$$\alpha = \theta_{max} - 2\pi D + \beta[\cos(\theta_{max} + \phi) - \cos(2\pi D + \phi)] \quad (17)$$

The RMS current I_S in the transistor is calculated using (18) . It should be noted that this expression is only valid for low duty cycle values.

$$I_S = \frac{P}{V_{in}}\sqrt{\frac{D}{3}} - \sqrt{\frac{2DP}{3R_e}}\sin(2\pi D + \phi) \quad (18)$$

According to these constraints, the selected GaN device is the GS66504B 650V 15A with a $R_{DS_{on}}$ of 100mΩ and an output capacitance C_{oss} of 80pF at 100V.

The reverse voltage V_{RRM} applied to the rectifier diodes and the RMS diodes current I_D can be calculated using (19) and (20). The selected SiC Schottky diodes for this work are the FFSD1065A 650V 10A.

$$V_{RRM} = \sqrt{R_{LED}P} \tag{19}$$

$$I_D = \frac{\pi}{2}\sqrt{\frac{P}{R_{LED}}} \tag{20}$$

EM-Circuit Simulation Model of the Class E/D Converter

In this section an EM-Circuit simulation model of the resonant DC/DC converter that takes into account the influence of the PCB is proposed. The followed procedure to build the simulation model is given in Fig. 8. First, the passive and active devices are characterized and their equivalent circuit models are determined. Then an EM model of the PCB is built in Advanced Design System (ADS®) software. All models are finally lumped in a transient simulation to analyze the electrical performances of the power converter.

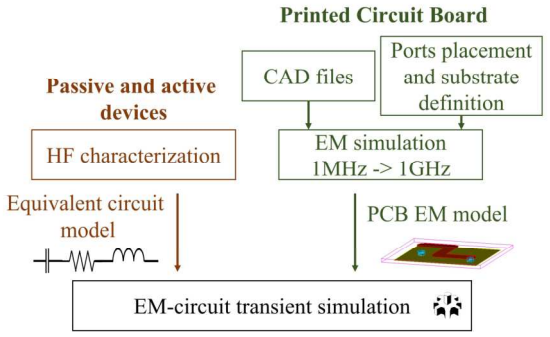

Fig. 8: EM-Circuit simulation procedure

Passive Devices Modeling

The input inductor, L_{in}, and the resonant inductor, L_r, are characterized with the impedance analyzer E4991B-100 within a frequency range of 1 MHz to 100 MHz. Both inductors are then modeled by the equivalent circuit given in Fig. 9(a) by fitting the experimental impedance curves versus frequency [9]. Table II summarizes the inductors model parameters.

The impedance curves of the multilayer ceramic capacitors C_s, C_r and C_f are extracted from data given by the manufacturer. All capacitors are then modeled by the equivalent circuit given in Fig. 9(b). Table III summarizes the model parameters of the capacitors.

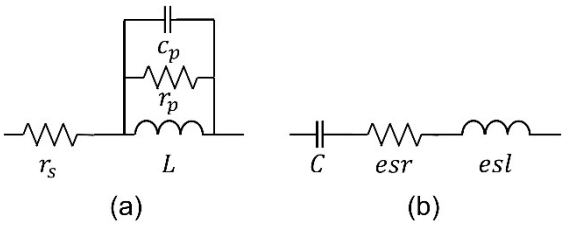

Fig. 9: Equivalent circuit model of inductors (a) and capacitors (b)

Table II: Inductors model parameters

	L (µH)	r_s (mΩ)	r_p (kΩ)	c_p (pF)
L_{in}	100	120	8.8	9.4
L_r	3.6	343	41	3.8

Table III: Capacitors model parameters

	C (nF)	esr (mΩ)	esl (nH)
C_s	10	15	2
C_r	15.5	10	2
C_f	1000	5	0.65

Active Devices Modeling

A complete methodology to build the high frequency models of packaged GaN transistors and SiC Schottky diodes using S-parameter and pulsed I(V) measurements has already been presented in previous work [10], [11]. This method is rigorously followed in this work to get the simulation model of the GaN transistor GS66504B and the SiC diodes FFSD1065A.

PCB EM Modeling

The realized prototype of the Class E/D DC/DC converter and its PCB layout are presented in Fig. 10. The power converter is designed on a 0.4 mm thick FR4 substrate with 35 µm top and bottom copper layers. The bottom layer is dedicated to a ground plane in order to minimize the parasitic inductances in the commutation loops [12].

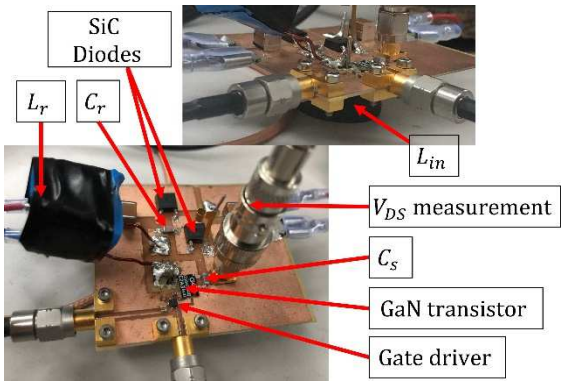

Fig. 10: Prototype of the Class E/D DC/DC converter

The procedure detailed in Fig. 8 is followed to build the EM model of the designed PCB using ADS Momentum. The main parameters for the EM simulation are given in Table IV.

Table IV: EM simulation model parameters

EM simulation	Mesh frequency	Mesh density
RF Mode	1GHz	350 cells/m

Gate Resistors Selection

In this converter, the most critical commutation loop is the gate circuit. Therefore, the gate loop is minimized as shown in Fig. 11.

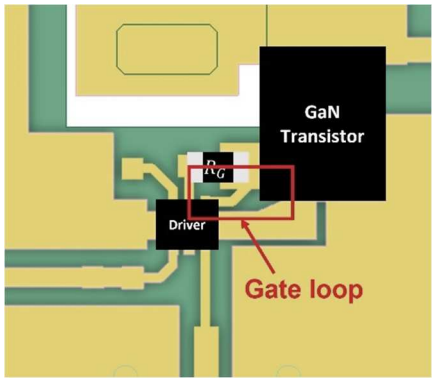

Fig. 11: Gate loop of the designed converter

A S-parameter simulation is performed on the EM model of the PCB in order to determine the gate loop parasitic inductance l_G [7]. The parasitic inductance is estimated from the imaginary part of the gate loop impedance and its evolution over frequency is shown in Fig. 12. A parasitic gate loop inductance $l_G = 2.4\text{nH}$ is found at 1MHz and it can be observed that this value is stable between 1MHz and 100MHz.

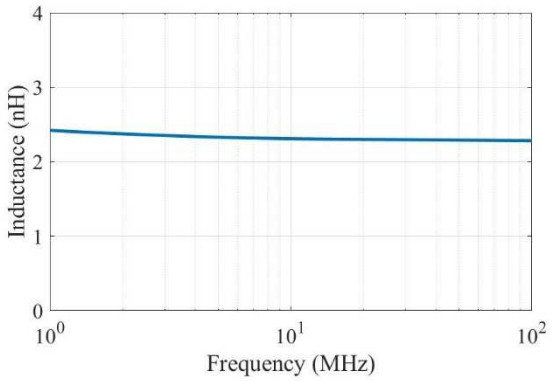

Fig. 12: Parasitic gate loop inductance l_G versus frequency (EM Simulation)

Using the extracted l_G, the gate resistor R_G is selected according to equation (21) in order to limit v_{GS} overshoots without excessively slowing down the switching process [13].

$$R_G = \sqrt{\frac{l_G}{C_{iss}}} \tag{21}$$

Where C_{iss} is the input capacitance of the GaN transistor.

All the active and passive devices are modeled by equivalent circuits and the EM Model of the PCB is obtained. Then, a transient simulation can be performed on the complete EM-circuit model of the resonant converter. The next section highlights the main experimental and simulation results obtained in this work.

Experimental and Simulation Results

A comparison between experimental and simulated waveforms of v_{DS}, I_{in} and I_{out} is performed at the test conditions listed in Table V.

A DC resistive load of 11.3Ω is used to emulate the power LED. It is constituted of a series-parallel connection of several power resistors TKH45P50R0FE and TKH45P2R00FE (Ohmite). The rated power for the DC load is 225W.

The results are presented in Fig. 13. It can be seen that the proposed simulation model permits to estimate the experimental waveforms with good accuracy. A non-perfect ZVS switching is obtained as shown in Fig. 13(a).

This can be due to the shift on the L_r value and the presence of parasitic (devices, PCB…) that were not taken into account in the design process. Another observation is that the maximal voltage constraint on the GaN transistor is 2.5 times higher than the input voltage. This can be verified with equation (15).

Table V: Nominal test conditions

Input voltage	100V
Switching frequency	1MHz
Duty cycle	18%
DC load resistance	11.3Ω

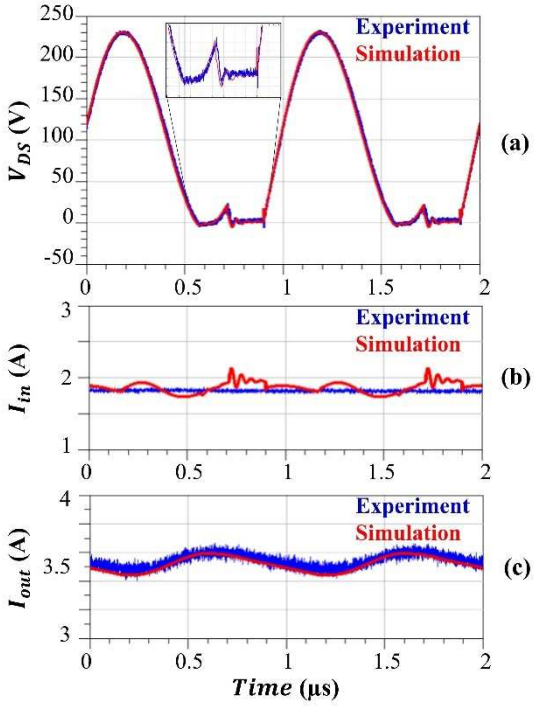

Fig. 13: Experimental vs simulated waveforms: (a) v_{DS} (b) I_{in} (c) I_{out}

The obtained output power is 160W for an input voltage $V_{in} = 100V$. While a theoretical power of 100W was used in the design procedure. The difference is explained by the design hypothesis that are not completely verified. Indeed, the current through the input inductance presents a ripple of 200mA while the resonant current presents a slight harmonic distortion. Furthermore, the presence of parasitic elements in the circuit and the tolerances, in particular on the resonant inductor value, impact the rated power of the converter. This last point highlights the fact that the design procedure must be improved in future work to take parasitic effects and devices imperfections into consideration.

The voltage waveform at the output of the class E inverter stage, v_{inv}, is given in Fig. 14. The simulation model permits to estimate the voltage rise time and ringing at 140MHz with good precision as shown in Fig. 14.

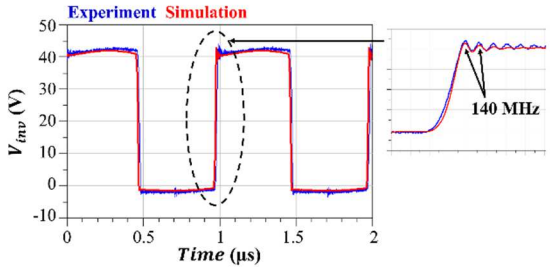

Fig. 14: Experimental vs simulated waveform of the voltage v_{inv}

The efficiency of the designed class E/D DC/DC converter is estimated by measuring the DC input and output powers. Fig. 15 presents the evolution of the efficiency versus the output power level. An efficiency of 81% is reached for an output power of 100W ($V_{in} = 80V$).

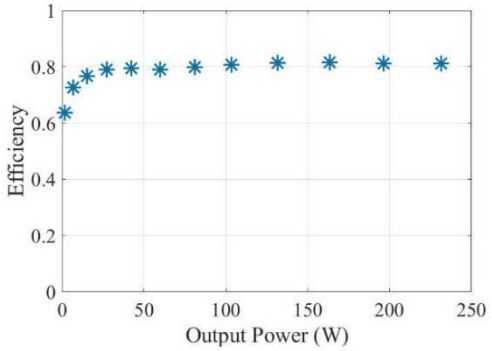

Fig. 15: Efficiency vs. output power

Fig. 16(a) shows that the input current I_{in} and output current I_{out} are both evolving linearly with the input voltage V_{in}. These results highlight the inherent PFC operation of the proposed power converter (resistive behavior). Using these results, the AC input current resulting from a rectified AC input voltage of 120V 60Hz can be estimated over an AC grid period as presented in Fig. 16(b). In future work, this waveforms shall be verified experimentally.

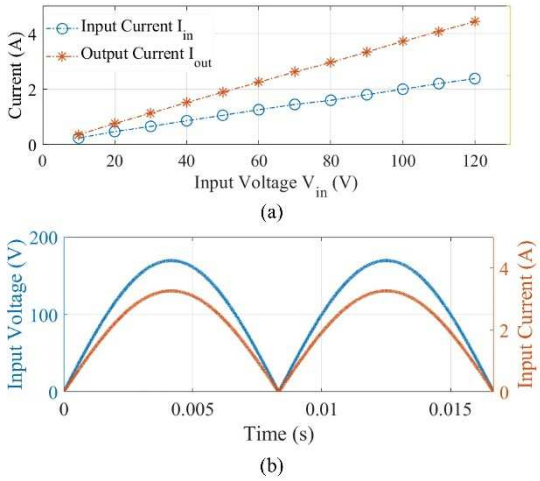

Fig. 16: (a) Input and output current vs. input voltage (b) AC input current vs. AC input voltage

Conclusion

This paper proposed a complete design procedure for a 100W 1MHz GaN-based class E/D DC/DC converter with the objective of replacing the conventional two-stage topology of LED drivers for improved power density. It has been demonstrated that the designed resonant converter is able to perform ZVS and PFC functionality inherently. This work also highlighted the importance of high frequency modeling. An EM-circuit simulation model taking into account the PCB layout parasitic has been developed and demonstrated a good capability to predict voltage and current waveforms.

Experimental results have shown an efficiency of 81% at 100W output power. Future work will focus on improving this efficiency. Using the developed HF simulation model, the air-core resonant inductor L_r could be designed on PCB in order to better manage the inductance value and the parasitic. An integration of L_r in a PCB assembly is considered as a perspective. Also, the diodes of the Class D rectifier shall be replaced by lower voltage rating Schottky diodes with better dynamics and lower losses. Finally, a major future prospect is to improve the design procedure by considering circuit and devices parasitic as parts of the converter topology.

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