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ABSTRACT: We demonstrate experimentally the dual beam optical drive of an interconnect-free 2-input, 2-output 1-bit adder implemented inside a single gold plasmonic cavity focused ion milled in an ultrathin single crystalline gold microplate. To obtain this result, we have set a coherent 2-beam excitation scheme up that allows to independently and arbitrarily set the intensity, polarization and relative phase shift of two femtosecond-pulsed laser spots. The spots are focused on any chosen location of the micrometer-sized plasmonic cavity. The nonlinear photoluminescence (NPL) response of the cavity encodes the Boolean output, while the Boolean inputs are borne by the linear polarization of the excitation. A generic map analysis tool is developed to pinpoint the realized Boolean functions and to assess their robustness. This tool is used to demonstrate the experimental implementation of the elusive XOR gate and its combination with an AND gate, in the same cavity, to perform the full 1-bit adder. The analysis of 160,000 instances of the 1-bit adder clearly shows the soundness of our approach and reveals some underlying mechanistic features of the remotely-generated NPL. These results establish the first practical step of a general approach to interconnect-free all-optical arithmetic and logic units.

INTRODUCTION

Information processing involves data storage, in memory, and processing instructions, usually handled by a central processing unit (CPU) in which the Control Unit (CU) instructs the arithmetic and logic unit (ALU) to perform actual binary data computations. Current information technology relies primarily on the von Neumann architecture, in which the CPU accesses both the data and instructions, that are stored in the same memory unit, through a single bus. While this simple, thus cost-effective, implementation has been massively applied in most microelectronic systems, it also creates a fundamental limitation known as the von Neumann bottleneck: during the slow data reading/writing, the CU/ALU partially idles and further information processing is delayed. In the so-called "Harvard architecture" alternatives, data memory and instruction memory are independently accessible from the CU that can continuously instruct the ALU to process information. The potential for faster and more efficient processing is however compromised by the complexity of the required circuitry. Even though the concept has been used for basic signal processing, dedicated micro-controllers and embedded in modern von Neumann architectures by adding two on-chip caches dedicated to instructions and data,[1] the overall performance gain remains modest.[2] Note that the recent tremendous progress in deep-learning relies on handling a vast amount of data, for which a third architecture, namely in-memory computing based on artificial neural network hardware,[3-5] including optical versions,[6-8] may be a better alternative. Yet the compulsory initial learning phase is not suitable for all information processing needs.

The recent advances of fast and low-loss optical data transfer down to on-chip trafficking[9-10] will provide a major asset to independently fetch data and instruction if (1) universal optical processing schemes would provide all-optical ALU and (2) if the circuit footprint of the CU and ALU could be significantly reduced to simplify the routing

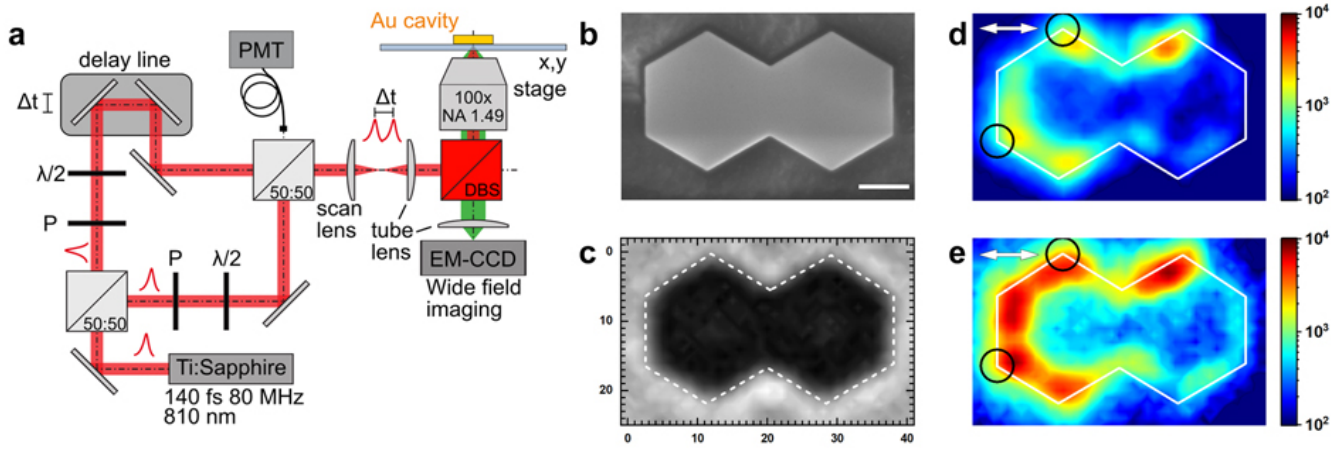

Figure 1. (a) Experimental set-up for driving the delocalized NPL response of a two input ALU. The 810 nm, 140 fs pulses are splits in two beams of equal intensity. The polarization of each beam is chosen independently by a pair of polarizer (P) and half-wave plate (λ/2). Beam 1 is focused onto the first input port. The pulses of Beam 2 are first delayed by Δt with respect to Beam 1 before being stirred onto the second input port. The wide-field NPL image is channeled onto a CCD camera by a dichroic beam splitter (DBS). (b) SEM image of a 2.5-μm wide double hexagon (DH) device milled by FIB from a crystalline Au microplate. (c) Optical transmission image under halogen lamp illumination of the DH on the XY stage of the NPL microscope (42 x 27 pixels). (d, e) Wide field NPL map of the DH excited by Beams 1 and 2 positioned in the top and lower left apices (black circles) with a horizontal linear polarization (0°). In (d) the delay Δt is set such that both pulses do not overlap and correspond to an incoherent excitation condition. In (e), Δt is tuned to maximize the pulse overlap resulting in a marked difference of the NPL response in the coherent excitation condition. (b-e) share the same 500 nm scale bar shown in (b).

implementation. We have recently proposed that two-dimensional plasmonic cavities carved from ultrathin and crystalline gold microplates could be operated as reconfigurable all-optical ALU.[11] A proof-of-concept was established by recording the non-linear photo-luminescence (NPL) response of the cavity upon excitation of a single location of the cavity edge with one fs-pulsed focused laser spot. The agile reconfigurability was experimentally demonstrated and several logic gates were reported. Yet, one critical step of this new paradigm was demonstrated numerically only: the implementation of one missing essential Boolean function, the XOR gate, and its combination into multiple input/output ALU.

In the present Article, we bring forward the experimental demonstration of the first 2-beam excitation of the plasmonic cavity and support all data with numerical Green Dyadic Method (GDM) simulations. Moreover, we develop a systematic search protocol to identify earmarked Boolean functions realized by the cavity and assess their robustness. This approach allows us to realize the missing XOR gate and to combine it with an AND gate into the first experimental 2-input, 2-output all-optical 1-bit adder. These results establish the first step of a general method to construct interconnect-free optical ALUs, that may enable the construction of an all-optical Harvard computing architecture.

RESULTS AND DISCUSSION

The principle of coherent excitation of the 2D plasmonic cavities is described in Figure 1. The two-dimensional resonant surface plasmon (SP) modes borne by these cavities result in extended near-field patterns that promote a distributed non-linear photoluminescence (NPL) response, even away from the excitation spot, under focused pulsed laser excitation.[11] The NPL is both energy shifted with respect to the excitation and spatially better resolved than any linear signal, without the impediments of near-field techniques.[12] Hence, NPL mapping provides a convenient observable to probe the modal optical response of the micrometric ALU devices. The NPL is obtained by exciting the ultrathin crystalline gold structure with a tightly focused 140 fs pulsed Ti:Sapphire laser beam (80 MHz repetition rate). Two independent coherent beams are obtained by splitting the laser output along two distinct paths (Fig. 1a). One of them is stirred through a delay line. The temporal synchronization of the two laser beams, Δt, achieved by moving the delay line, is monitored by a photomultiplier (PMT) aligned on the recombining beam-splitter. The temporal coincidence of the two beams is characterized by a maximal intensity recorded on the PMT as detailed previously.[13] The power, polarization and position of each beam are controlled independently with a pair of polarizer (P) and half-waveplate (λ/2). The diameter of the laser spots in the sample plane is about 300 nm with a Gaussian profile.

The two-dimensional (2D) plasmonic cavity studied here is composed of two juxtaposed regular hexagons of 715 nm side (Figs. 1b,c). The 2.5 × 1.1 μm structure is carved by focus ion beam (FIB) into an ultrathin crystalline Au microplate deposited on a 22 × 22 × 0.15 mm ITO/glass

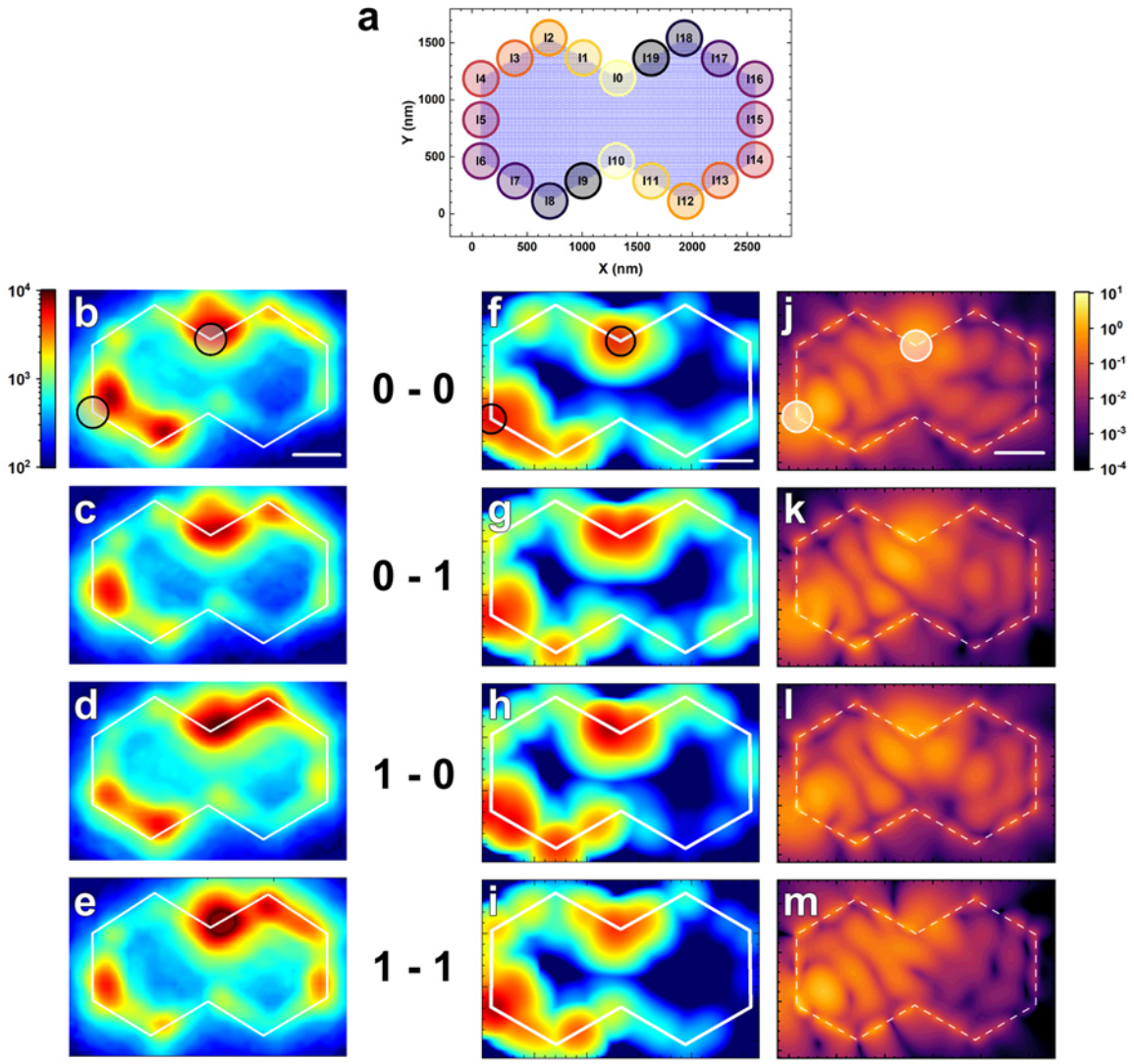

Figure 2. (a) Numerical model of the DH sample shown in Fig. 1b and used for all GDM simulations. The 20 input ports considered along the DH edge are marked with 300 nm diameter circles. (b-e) Experimental coherent wide-field NPL maps recorded when port I_0 and I_6 are excited in all four possible configurations with polarizations 0° and 30° encoding the "0" and "1" Boolean inputs. (f-i) Emulated NPL maps derived from (j-m) as detailed in the text. The logarithmic color scale is identical to (b-e). (j-m) Simulated near-field maps computed at 14 nm away from the structure when the DH is coherently excited, from the glass substrate side, by two linearly polarized beams focused in I_0 and I_6. The polarizations are 180° ("0") and 30° ("1"). A relative phase of 110° is set between the two beams. Scale bars are 500 nm.

coverslip.[11, 14] The Au microplate is grown in solution accord ing to the protocol described by Guo et al.[15] Figure 1c shows a bright field image of the double hexagon (DH) cavity taken with the 100x objective (N.A. 1.49) also used for the delocalized NPL excitation. Note that bright-field imaging is performed with a Köhler diascopic illumination not shown in Figure 1a. The wide-field image is collected by an ultra-sensitive Electron Multiplying CCD (EM-CCD) camera, which has a resolution of about 71 nm/pixel in this configuration. The dashed white line in Figure 1c highlights the outline of the structure observed by scanning electron microscopy in Figure 1b. When excited by the focused laser beam in a fixed position, wide-field NPL images are recorded on the EM-CCD by averaging 20 repeated acquisitions with an exposure time of 1 s each and an EM gain of 10, as displayed in Figures 1d and 1e. Note that the near-infrared pulsed excitation (λ = 810 nm) is filtered out from the NPL maps with a dichroic beam splitter (DBS). Figure 1d shows a NPL map recorded when the two laser beams are polarized along the horizontal direction (0°) and focused on the two apices marked by black circles. The delay Δt is chosen such that the two pulses arrive on the DH structure without any temporal overlap. In this non-coherent excitation case, the NPL map is the incoherent sum of the NPL generated by the first beam and that of the second integrated over exposure time. Remarkably, the response occurs not only at the excitation area but is delocalized over the entire structure, primarily along its perimeter. When tuning Δt to maximize the temporal overlap but keeping all other parameters identical, as shown in Figure 1e, a ten times more intense response is recorded and the spatial distribution of the NPL intensity is modified. This coherent excitation condition was thoroughly explored in a previous study,[13] where we

showed that the NPL intensity in a specific location can be finely tuned by controlling the coherent superposition of surface plasmon modes, when adjusting the delay Δt.

Here, we apply the global adjustment of all excitation parameters, including the delay, to enhance the output signal of multiple all-optical logic gates realized by the same reconfigurable cavity. To this end, the two focused laser beams impinging on the sample from the silica substrate side carry the "0" or "1" input Boolean information encoded in their respective linear polarization. We define a set of 20 input positions along the DH edges and apices (Fig. 2a). For two chosen inputs, this leads to four coherent excitation configurations corresponding to the Boolean entries "0-0", "0-1", "1-0" and "1-1" as exposed in Figures 2(b-e). First, let us consider the inputs I_0 and I_6 and the polarizations 0° ("0" state) and 30° ("1" state). The four maps show contrasted and different delocalized NPL patterns with marked intense spots in remote apices. Interestingly, the NPL intensity in the core regions of the two hexagons is two orders or magnitude lower and almost reach the background signal observed away from the DH cavity. Several recent works have established that the NPL originates from the radiative decay of an out-of-equilibrium electron gas formed after the absorption of an intense laser pulse,[16-18] the spatial distribution of which, in the case of plasmonic metals, is closely related to the electromagnetic near-field. In order to predict the linear electromagnetic response of the DH cavity, we are using the Green Dyadic Method (GDM)[19] and its open-source Python implementation (pyGDM).[20-21] Our numerical model consists in two linearly polarized Gaussian beams focused on the glass/DH interface with a beam waist of 300 nm in a paraxial approximation. In agreement with the experimental configuration, the input ports are set to I_0 and I_6 and a phase shift between the inputs is set to 110°. We assign Boolean values of "0" and "1" to linear polarizations of 180° and 30° respectively. Note that the relative phase is assigned to the second input port with respect to the first one, while the polarizations are interchanged during ALU operation. This implies that polarization angles modulo 180° are not equivalent even though they cannot be distinguished experimentally. In simulations, polarizations angles where not restricted to the [0°; 180°[interval but explored the entire [0°; 360°[possibilities. The corresponding simulated near-field maps, computed 14 nm (i.e. one discretization cell) below the DH structure, are presented in Figures 2(j-m). Even though variations of the near-field are clearly discernable as the input polarizations are flipped between the two values, the direct comparison with the experimental NPL maps of Figs. 2(b-e) is not straightforward. In order to facilitate this comparison, and in the absence of a comprehensive model of the delocalized NPL generation mechanism, we have developed a phenomenological model of the spatial distribution of the near field to NPL conversion described in Supporting Information section S1.[13, 16] The processing of the simulated near-field maps through our phenomenological model results in the images presented in Fig 2 (f-i). The four emulated NPL maps globally reproduce the main features of the corresponding experimental maps, even in the absence of any adjustment parameter. The high NPL intensity spots along the DH perimeter as well as the low signal regions in the central regions of the two hexagons are adequately accounted for. Also, as the polarizations are exchanged, the intensity of the emulated NPL along the DH perimeter evolves significantly as observed experimentally. Nevertheless, in contrast to confocal map simulations,[14, 22] some minor differences are visible in the relative intensities at the apices. While the assumptions of the phenomenological description of the plasmon-to-photon transduction and some standard approximations in the near-field simulation model may partially account for these differences, they underline the still lacunary knowledge of the mechanism of the remote generation of NPL photons in spite of recent theoretical advances.[23-24]

Meanwhile, the design, identification and location of ALU functions with increasing Boolean complexity implemented within plasmonic cavities is a tedious and time consuming task. Yet a fast and systematic survey of the existence, localization and performance of Boolean functions for a given cavity and excitation conditions has been developed as detailed in Figure 3 for the case of two inputs. Let us consider an OR gate: the outputs of the "0-1", "1-0" and "1-1" configurations are "1" when the output of the "0-0" configuration is "0" (Fig. 3a). This could be imperfectly realized as shown in Figure 3b. A realistic OR gate could be generally defined by ensuring that the output signal for "0-1", "1-0" and "1-1" exceeds the output for "0-0". The excess, i.e. the difference between the highest signal encoding a "0" output and the lowest signal encoding a "1" output, is named the Boolean contrast, $\varepsilon \geq 0$. An OR gate is defined by a system of inequalities that have to be simultaneously realized. Figure 3c shows the three differences maps obtained by subtracting the near-field map of Fig. 2j ("0-0") from the near-field maps of Figures 2k ("0-1"), 2l ("1-0") and 2m ("1-1"). The OR gate will be realized only where and when all three difference maps simultaneously exceed ε. A composite map is equivalently deduced by applying the following formula in each pixel:

$$\varepsilon = Max[Min(\text{"0-1"}; \text{"1-0"}; \text{"1-1"}) - \text{"0-0"}, 0]$$

The resulting gate location map in Figure 3d color-codes the Boolean contrast and reveals the existence of the OR gate in several regions across the DH structure, wherever ε is non-zero. A first-level assessment of the gate quality is provided by the map intensity: the darkest regions correspond to the highest Boolean contrast, i. e. the most robust logic response. In the white areas, the OR gate is not realized. The exact same Logic Gate Positioning Search protocol (LGPS) is applied, in Figure 3e, to the corresponding experimental set of NPL response maps (Figs. 2b-2e). The most striking difference between the experimental and simulated LGPS maps is that the former shows finite Boolean contrast close to the edge only. This is consistent with the emulated NPL model and the reported observation that plasmon-mediated NPL emission requires an abrupt hot electron momentum

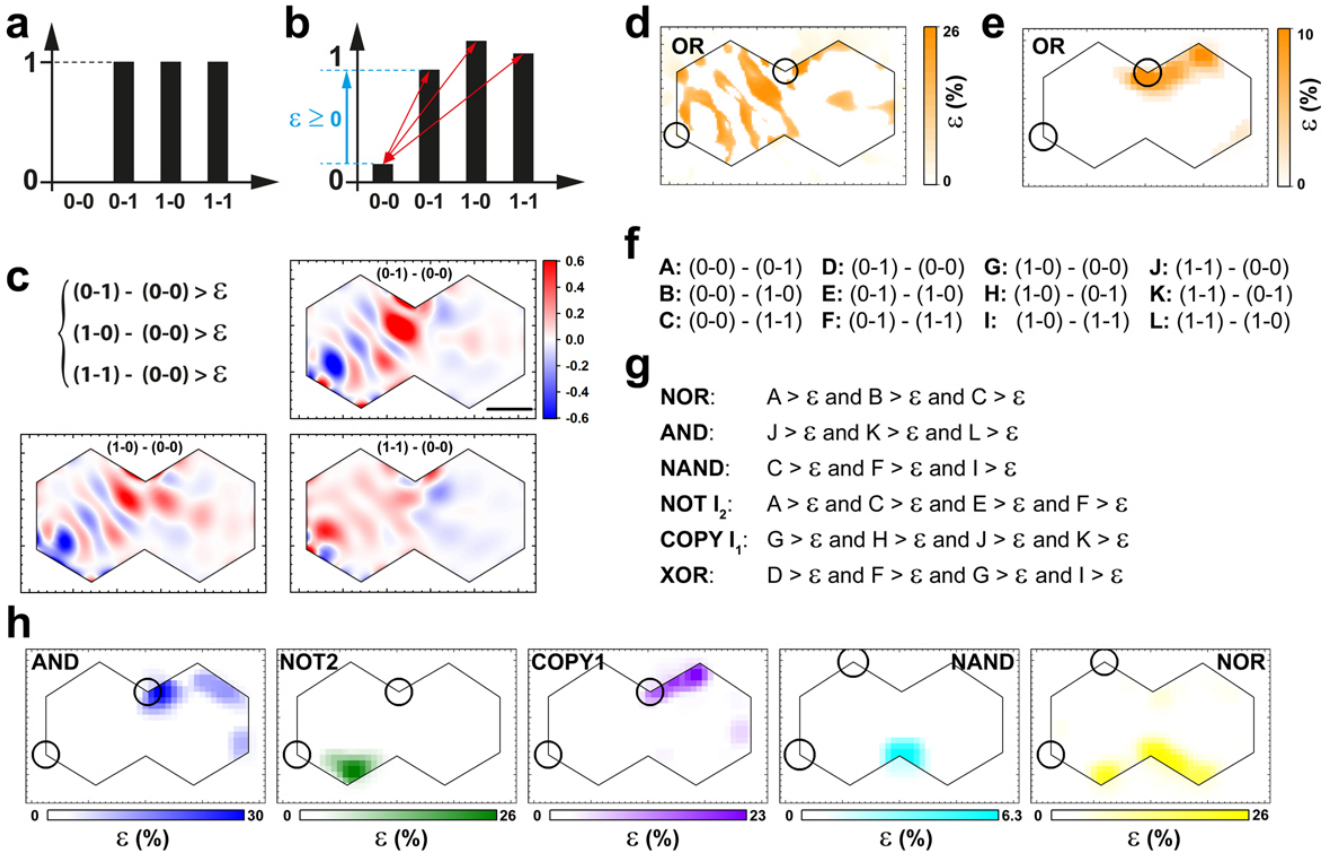

Figure 3. Boolean gate search methodology. (a,b) Bar representation of (a) a formal and (b) a non-ideal 2-input OR gate for which the Boolean "0" output signal is finite and all analog signals encoding a "1" output may not be identical. The quality of the non-ideal gate can be characterized by its Boolean contrast, ε, which is the difference between the smallest "1" signal and the largest "0" signal. (c) An OR function will be realized if all the differences between any analog signals encoding "1" outputs and any signal encoding "0" outputs are greater than ε. The three difference maps correspond to the OR gate function and are based on the simulated near field maps shown in Figs. 2j-m. An OR gate is realized only in regions that are simultaneously exceeding ε ≥ 0 in all three maps. (d, e) Color-encoded Boolean contrast (ε) map of the OR gate resulting from the combination of difference maps based on near-field and NPL maps from Fig. 2j-m and Fig. 2b-e respectively. (f) Exhaustive list of map differences required to systematically locate all possible 2-input gates. (g) Combinations of conditions based on difference maps in (f) to reach some of the classical 2-input 1-output gates. (h) Gate location maps identifying AND, NOT, COPY, NAND and NOR gates in different areas of the DH device. In (d), (e) and(h), input locations are marked by black circles and the color scales indicate the min/max Boolean contrast values.

variation, which is conveniently provided by collisions with the cavity edges. If one ignores the core region of the DH in Figure 3d, the Boolean contrast of the OR function is sizeable along the edge between I_{17} and I_0, primarily, which coincides with the maximal Boolean contrast in the experimental LGPS map (Fig. 3e). To a lesser extent, the same coincidence is observed between I_{14} and I_{15}. The absence of experimental observation of the OR gate in I_1, I_2, I_3, I_4 or I_{10}, where the near-field LGPS map suggests its occurrence, indicates, here again, that the sole knowledge of the near-field distribution does not allow a quantitative prediction of the NPL emission pattern. We therefore have focused the systematic search of logic gates on experimentally recorded data. The LGPS protocol can be generalized to all possible 2-input Boolean functions by first computing the twelve possible difference maps detailed in Fig. 3f. The existence of any Boolean function can then be determined by a system of inequalities where a subset of the A to L difference maps are compared to a chosen Boolean contrast. Figure 3g lists the conditions required for some of the main 2-inputs logic gates. It is straight forward to automate such a methodology and to apply it to sets of maps obtained for all Boolean input configurations. As an example, Figure 3h displays the LPGS maps for the AND, NOT and COPY gates derived from Fig. 2b-e but also the NAND and NOR gates obtained for a different set of input ports (I_2, I_6) and polarizations (0° for "0", 150° for "1"). The systematic search for gates confirms the effective Boolean reconfigurability of our DH cavity

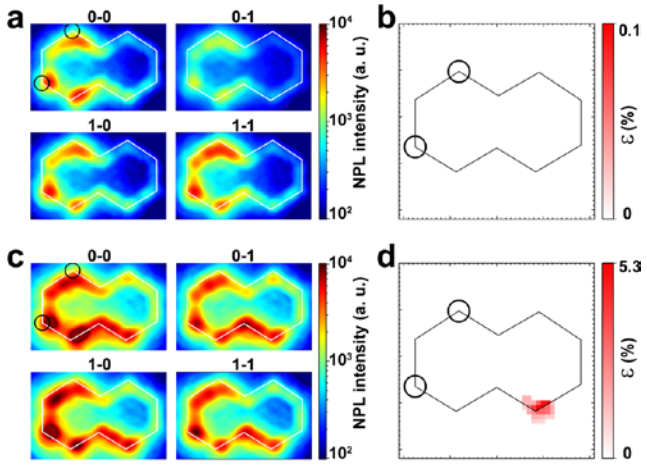

Figure 4. (a) Wide-field NPL maps for the four Boolean configurations of the DH non-coherently excited in I_2 and I_6 with linear polarizations 0° (input "0") and 150° (input "1"). (b) Corresponding gate location map that fails to show any presence of the XOR gate output. (c) Wide field NPL maps and (d) corresponding gate location map in the exact same excitation condition but with a delay that allows a maximal pulse overlap to produce a coherent excitation. The XOR gate is clearly realized in I_{12}.

device in a coherent excitation scheme as initially demonstrated in numerically-processed sequential excitation.[11] The LGPS tool allows to rapidly identify, locate and assess elusive non-additive Boolean functions such as the XOR and NXOR logic gates. Indeed, such functions are not achievable in an incoherent, sequential excitation scheme but we numerically predicted that it could be obtained if destructive plasmon interferences were exploited to limit the NPL emission rate for both "0-0" and "1-1" compared to the "0-1" and "1-0" configurations of the XOR gate.[11] Such a fine control of the dual-beam excitation of the cavity plasmon modes is technically enabled by the addition of the delay line shown in Figure 1.[13] In Figure 4, we compare the NPL output maps and XOR LGPS maps when the pulses geared to the two DH inputs (I_2, I_6) are temporally decoupled (Figs. 4a-b) and when Δt is adjusted to maximize the plasmon interferences (Figs. 4c-d). Clearly, the sole tuning of the excitation coherence, all other parameters being kept constant, leads to a large increase of the output signal over the entire cavity perimeter and to a significant spatial redistribution of the high NPL intensity regions (Fig. 4c vs Fig. 4a). More importantly, whereas no XOR gate is detected in the non-coherent excitation case, the coherent excitation leads to the effective realization of the XOR gate in I_{12}. This first proof-of-concept completes the set of all 2-input, 1 output gates experimentally realized in the same DH plasmonic cavities. It also opens the way to create interconnect-free arithmetic devices by combining several outputs since the XOR gate is performing the Boolean Sum function. For example, we have shown numerically that our approach would enable the implementation of a 1-bit full-adder ALU if the XOR were combined with the AND gate, that can be considered as a Boolean Carry function. Numerical simulations were carried out and systematically analyzed with the LGPS tool for the XOR and AND gates. Figure 5a displays a combined AND (blue) and XOR (red) LGPS map when the DH device is coherently excited in inputs I_6 and I_{10} with polarizations 190° ("0") and 40° ("1") and relative phase of 170°. The spatial location of both gates is complementary as it is impossible, for a given pixel, to comply simultaneously with both sets of inequalities: for AND, the condition $L > \varepsilon$ must be observed (Fig. 3f). It implies that $I < -\varepsilon$ but, for XOR, one of the conditions is $I > \varepsilon$, which are mutually excluding. Similarly, the experimental exploration of the excitation parameters, including the pulse delay, led to the first technical demonstration of a 1-bit full adder with two inputs and two outputs based on the all-optical excitation of a plasmonic 2D cavity, shown in Figures 5b and 5c. In the LGPS maps of Figure 5c, the XOR gate, in red, is indeed realized in I_0, between I_2 and I_3 and in I_{18}, while the AND gate, in blue, is located between I_{11} and I_{12} with a comparable Boolean contrast. In order to probe the robustness of this first ALU device, each of the four NPL maps in Figure 5b has been recorded twenty times and we have computed the AND and XOR LGPS maps for all 160,000 (20^4) possible quadruplets of experimental maps. Figure 5d collects the averaged Boolean contrast per pixel for the AND (blue) and XOR (orange) gates. The similarity between Figures 5c and 5d demonstrates the robustness of the two logic gates that are primarily emitted from the locations identified in Figure 5c. When accommodating a more moderate Boolean contrast, the AND gate can also be found in I_{14} and the XOR between I_4 and I_5 and in I_{15}. Interestingly, the locations in the NPL maps, where the experimental gates are observed, match the regions where these gates are predicted by numerically computing the optical near-field. Yet, some regions of the near-field LGPS map showing a valid gate output do not appear in the experimental map. This residual discrepancy between simulated and experimental maps is attributed, again, to the lacunary theoretical description of the plasmon-to-NPL photon transduction

For a given Boolean function, the LGPS protocol identifies and quantifies which pixels are active with a non-zero ε value. Ideally, a device response with a few, high-ε pixels is preferable to a vast region of low ε pixels. We define a numerical figure of merit for each map, the Average Boolean Contrast per active pixel ABC_{AP}, that compares the Boolean contrast integrated over the entire map to the number of active pixels, i.e. pixels that comply with the logic gate existence conditions.

For the i^{th} map, with i = 1 to 160 000,

$$ABC_{AP}(i) = \frac{\sum_{k=1}^{N_{pix}} \varepsilon_k^{(i)}}{N_{pix} - n_i^{(\varepsilon=0)}}$$

For the i^{th} map, $\varepsilon_k^{(i)}$ is the Boolean contrast of the k^{th} pixel and $n_i^{(\varepsilon=0)}$ is the number of pixels with null Boolean contrast. Each LGPS map comprises N_{pix} 70-nm pixels, so that $N_{pix} - n_i^{(\varepsilon=0)}$ is the number of active pixels, for which ε is non-zero, of the i^{th} LGPS map.

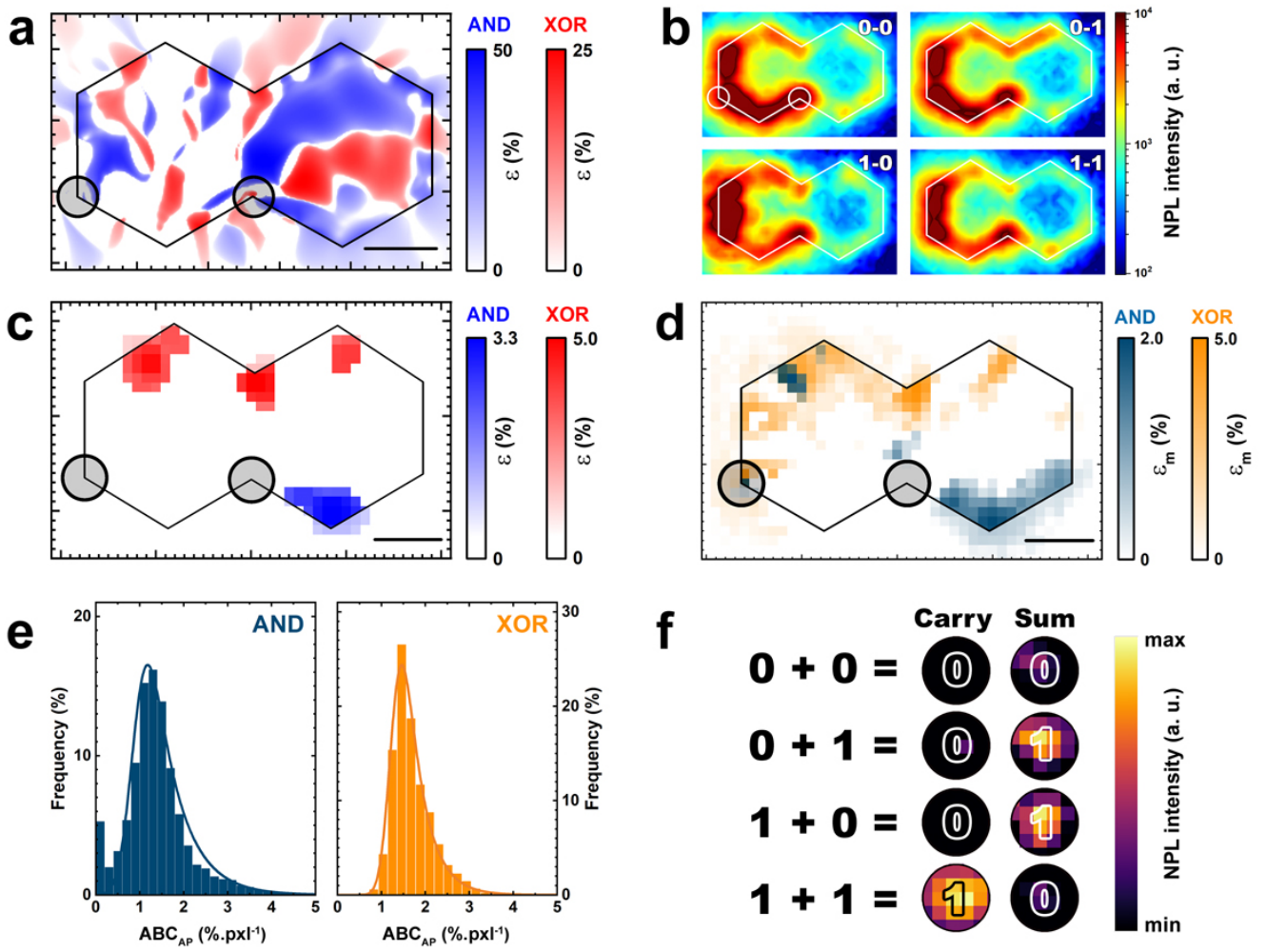

Figure 5. Experimental implementation of a single cavity 1-bit full adder. (a) Gate location maps showing the Boolean contrast, ε, of the AND (blue) and XOR (red) based on near-field calculated for excitation in inputs I_6 and I_{10} with polarizations 190° ("0") and 40° ("1") and a phase shift of 170°. (b) Experimental coherent wide-field NPL maps recorded when port I_6 and I_{10} are excited in all four possible configurations with polarizations 0° and 40° encoding the "0" and "1" Boolean inputs. (c) Experimental gate location maps showing the Boolean contrast of the AND (blue) and XOR (red) derived from (b) and exhibiting simultaneous Boolean outputs in I_0, I_2 and I_{18} for XOR and I_{12} for AND. (d) Gate location maps of the AND (blue) and XOR (orange) based on the mean Boolean contrast per pixel, ε_m, averaged over 160 000 possible 1-bit full adder response derived from 20 independent repeats of each Boolean input configuration. (e) Distribution histograms of the ABC_{AP} figure of merit (Averaged Boolean Contrast per active pixel) for the AND (blue) and XOR (orange) gates. Continuous lines are exponentially modified Gaussian fits (see text for details). (f) Direct unprocessed experimental readout of the 1-bit full adder table of truth showing the binary addition of the two 1 bit inputs. The sum is provided by the XOR in I_0 and the carry by the AND in I_{12}.

For extreme cases of maps comprising only high-ε or only low-ε pixels, ABC_{AP} is close to the individual $\varepsilon_k^{(i)}$ values and so will be larger for maps showing larger Boolean contrast. For the general case, where the maps show a wide range of $\varepsilon_k^{(i)}$ values, the smaller of which could be considered as background signal and the larger of which constitute the useful signal, ABC_{AP} provides a weighted average in which the few high-ε pixels contribute to increasing ABC_{AP} and the numerous low-ε pixels tend to decrease ABC_{AP}. This single criterion does not guarantee that the active pixels are contiguous. Yet the NPL signal is monotonous and smoothly varying over spatial coordinates, thus the difference maps do not show discontinuities. Moreover, the system of inequalities for a given Boolean function simply carves sub-regions in each difference map and the simultaneous compliance consists in intersecting these sub-regions. Consequently, gate existence locations show sharp boundaries but are seldom restricted to isolated pixels. Hence, active areas are usually commensurate with optical detection as confirmed in Figure 5d. In Figure 5e, we plot the distribution histograms of this figure of merit applied to the 160 000 repeats of the AND and XOR maps. The distribution histograms for both the AND and the XOR gates are very similar and show a narrow asymmetric

distribution peaking at 1.51 ± 0.67% and 1.67 ± 0.46%, which confirms the very good repeatability of the logic gates operation. These means values are clearly away from zero, which demonstrate that all LGPS maps realize the 1-bit full adder, albeit with a Boolean contrast close to 2% and that can reach 4-5% in the excitation conditions considered here for the DH device. Taken together, Figures 5d and 5e validate a high detection reliability of our interconnect-free concept of multiple output ALU.

The histograms in Figure 5e show an unusual skew that deserves some extra scrutiny. We have attempted to fit these distributions by a number of asymmetrical functions. The exponentially-modified Gauss (EMG) distribution clearly provides the best fits and is overlapped as a continuous line on the histograms. An EMG distribution describes phenomena that depends on a sum of two random variables that follows a normal Gaussian distribution, for one, and an exponentially decreasing distribution, for the other.[25] The fits provide, in particular, the value for the exponential decay which is about 2 ± 0.4 pixels, i.e. 140 ± 30 nm. In the context of our work, the ABC_{AP} is essentially a difference of NPL intensities. Several sources of normally distributed variations of the NPL signal can be envisioned during the map acquisition. On our optical bench, we consider that the main one is the stochastic mechanical fluctuations of the delay stage. However, the NPL intensity recorded in a given pixel should also depend on the distance between that pixel and the cavity edge, as considered in the phenomenological model used in Figure 2. Since the distributions of Figure 5e encompass all pixels in a broad region around the cavity perimeter, such a dependency would be embedded in the ABC_{AP} histograms. We can suppress the contribution of the pixel-to-edge distance by restricting the sampling area to the pixels located on the DH perimeter (See Supporting Information, Section S2). The corresponding ABC_{AP} histograms of both AND and XOR gates (Fig. S2) recover a symmetrical and Gaussian shape, thus confirming that the NPL intensity decays exponentially over a length scale of about 140 nm away from the edge. Strikingly, such a decay length coincides with the mean free path of hot electrons generated by a fs-pulsed laser.[26-28] This observation provides important insight in the plasmon-to-NPL conversion mechanism and justifies, in part, our phenomenological model used to qualitatively convert the plasmonic near-field into NPL intensity.

The thorough analysis of the 160 000 repeats allows to identify the maximized direct readout of the 2-output ALU performing the 1-bit full adder function as shown in Figure 5f for a double 300-nm diameter detection area. The AND, in I_{12}, and XOR, in I_0, realize the carry and the sum respectively. We demonstrate here that the DH response in these locations computes the algebraic addition of the two input bits without requiring any cascade of the two output gates and retains the same DH footprint that was initially used for all simple 1-output gates. The reconfigurability of the DH enables the implementation of both arithmetic (full-adder) and logic functions (AND, NOT, OR) in the same unit, therefore accomplishing the concept of ALU, whereby the selectors are the optical excitation parameters. Considering the size of the DH structure, more inputs can be accommodated[11] and suitable excitation/detection schemes may allow to implement more complex ALU, such as a 2-bit full adder which, following our concept, would require four inputs and three outputs to reach 3+3 = 6 (i.e. 11+11 = 110 in binary digits).

CONCLUSIONS

In this work, we have demonstrated one crucial milestone of the holistic concept of all-optical implementation of Arithmetic and Logic Units in single plasmonic cavities by performing the 2-input, 2-output operations required to add two 1-bit numbers. One key aspect is to realize the carry reversal, which is shown by mastering the coherent excitation of SP modes upon tuning the temporal sequence of the excitation and by preserving this coherence between the input and output ports thanks to the gold crystallinity. We have developed a systematic tool able to identify the existence of Boolean functions and quantify their robustness by analyzing the 2-dimensional response of the cavity. Interestingly, this tool could be generalized to other paradigms of 2D implementation of logic devices such as nanoelectromechanical[29-30] or single molecule ALU,[31] for which response maps would be available. We have found that the Boolean response of the plasmonic ALU is enhanced at the cavity edges with a spatial dependency that suggests a major role of the wall collisions of the ballistic hot electron in the plasmon-to-NPL momentum conversion. In the absence of a comprehensive theoretical of this non-linear phenomenon, this observation has allowed us to propose a qualitative phenomenological model that may be useful for further device engineering. In particular, our non-cascaded approach can be generalized to more complex Boolean functions. This prospect will require, first, to optimize the figure of merit (coined here as "Boolean contrast") of the ALU, which is out of the scope of the present study, and then to solve the inverse problem of designing a suitable cavity and defining its excitation/detection conditions to perform an arbitrary N-input ALU. The first challenge could advantageously exploit recent advances in evolutionary optimization[32] and machine learning,[33-36] as well as experimental methods such as wavefront design[37] and beam shaping.[38] The second challenge is probably more ambitious as no guideline is available to determine what cavity shape and excitation/detection configuration would be best suited for realizing a given ALU function with satisfactory Boolean contrast. However recent progress in optimizing meta-surfaces[39-40] and transmission characteristics[41] in holistic optical devices offer a timely opportunity to further explore the concepts proposed here.

ASSOCIATED CONTENT

Supporting Information. Phenomenological model of Plasmon-to-NPL conversion (S1). Origin of the skewness in the ABC_{AP} distribution (S2). This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

ED and ABo conceived the experiments, FDO and ED nanofabricated the devices and developed the LGPS tool. FDO and ABo conducted the experiments. GCF, YB and DS performed GDM simulations. NG, JB, Abe, ONL, CN developed new simulations codes. ED, ABo, AL, CGF and FDO analyzed the data. ED drafted the manuscript which was amended by all co-authors. All authors have given approval to the final version of the manuscript.

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SYNOPSIS TOC

Table of Contents artwork