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Compact implementation of an all-optical 1-bit full adder by coherent excitation of a single 3- μm^2 plasmonic cavity.

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Abstract. In contrast to the high performances of long-range, high-speed optical information transfer, optical information processing remains outperformed by electronic microprocessing. The two main reasons are the lack of gain medium that hampers the development of an optical analogue of the transistor and the lack of compactness of the approaches proposed so far. Here, we demonstrate a new concept of the design of all-optical elementary computing units based on the shaping of plasmonic modal landscape in micrometric on-chip 2D cavities to realize reconfigurable Arithmetic and Logic Units (ALU). Our interconnect-free devices perform multi-bit logic gate functions in a single cavity without ALU cascading, therefore obviating loss in vias and so the need for gain to restore the binary signal. Moreover, an astute cavity design allows to reconfigure a single cavity into multiple logic functions, including a first full adder. The main challenge on the way to increasing the functional Boolean complexity is the design of the cavity shape and of the excitation/detection parameters for which an approach based on artificial intelligence will be implemented.

1 Introduction

Processing information with conventional integrated circuits remains beset by the interconnect bottleneck: circuits made of smaller active devices need longer and narrower interconnects, which have become the prime source of power dissipation and clock rate saturation. Optical interchip communication provides a fast and energy-saving option that still misses a generic on-chip optical information processing by interconnect-free and reconfigurable Boolean arithmetic logic units (ALU). Considering metal plasmons as a platform with dual optical and electronic compatibilities, we forge interconnect-free, ultracompact plasmonic Boolean logic gates and reconfigure them, at will, into computing ALU without any redesign nor cascaded circuitry. As a starting point, we tailor the plasmon mode landscape of a single 2.6 μm^2 planar gold cavity and demonstrate the operation and facile reconfiguration of all 2-input logic gates. In particular, we show that the critical XOR gate is achieved by harnessing the coherent multibit excitation of the cavity, which opens the way to the first arithmetic function, the 1-bit full adder.

2 Reconfigurable modal plasmonic logic gates.

The general principle of plasmonic modal logic gate is illustrated in Figure 1. Surface plasmons (SPs) sustained by an ultrathin crystalline gold microplatelet are confined

in a two-dimensional cavity that creates resonant SP modes. The resulting near-field patterns are distributed over the entire structure as a set of strongly contrasted localized and enhanced spots. To promote an optimal input–output information transfer, we focus here on a continuous double hexagonal shape (Figs. 1A,B) with a size adjusted to show transmittance resonances in the visible (720 nm) to near-IR (810 nm) region. [1,2]

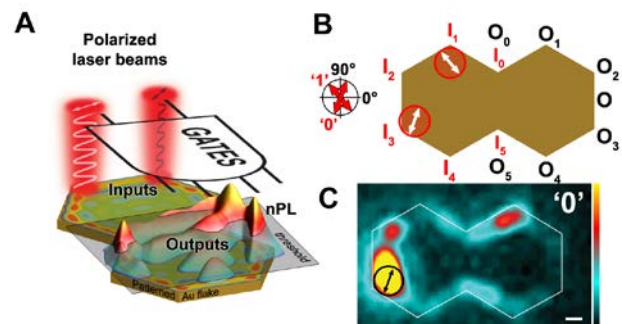


Fig. 1. (A) Schematic of a 2D crystalline gold cavity shaped into a double hexagon (DH) device (brown) that bears plasmonic eigenstates, which determines the optical near-field response. Two laser beams, with specific linear polarizations that encode the Boolean “0” and “1” inputs, excite the device that produces a remote nonlinear photoluminescence (nPL) signal with strong spatial variations in the output region. A nPL signal exceeding a threshold value corresponds to a Boolean “1” gate output. (B) Locations of the DH device inputs and outputs. A two-beam excitation is exemplified for inputs I_1 and I_3 with input polarizations 130° (Boolean “1”) and 70°

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(Boolean "0"), respectively. (C) Wide-field nPL image obtained by exciting the structure in position I_3 with linearly polarized light oriented at 70° from horizontal. The map is the response function of the device to a Boolean "0" in input I_3 . [2]

Our devices are fabricated by focused ion beam (FIB) milling single-crystalline gold microplatelets produced in solution and drop-casted onto ITO-coated glass coverslips. The FIB nanofabrication leads to a standalone double hexagon with sharp edges and preserved crystallinity. The footprint of the structure is $2.65 \mu\text{m}^2$ (extremal size of $2.5 \times 1.1 \mu\text{m}$).

When a femtosecond pulsed laser is focused on a near-field hotspot, it efficiently drives the plasmon resonance and generates nonlinear photoluminescence (nPL) not only at the excitation spot but also in the most remote regions of a specific near-field pattern (Fig. 1C). In this work, the nPL is used as an all-optical observable of the transfer function of the device.

Following the above principles and exploring the vast parametric space that includes the choice of input and output ports, the Boolean-encoding polarizations, the output threshold and the excitation wavelength, we demonstrate the implementation of all possible 2-input, 1-output logic gates and the agile reconfigurability of the DH device from one gate to another. Examples of experimentally demonstrated logic gate functions are shown in Fig. 2. We will further show that 3-input logic gates can also be realized in the same cavity without resorting to any gate cascading. [2]

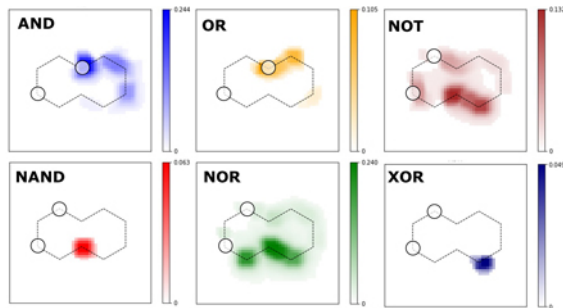


Fig. 2. Experimental Boolean contrast map for six different 2-input logic gates realized by reconfiguring the excitation conditions. The color scales indicate the intensity contrast between the Boolean "0" and "1" outputs. The input ports are marked with black circles. Adapted from [4].

3 Coherent excitation and full adder ALU

The non-additive XOR logic gate shown in Fig. 2 requires a specific attention. Indeed, the Boolean response of this gate cannot be reached by non-coherent excitation of the cavity. One way to obtain the appropriate table of truth is to exploit interferences by coherently exciting the surface plasmon modes. To achieve this regime, we have introduced the control of an extra degree of freedom, which is the temporal overlap between the femtosecond pulses exciting both inputs. [3] A delay stage is used to fine tune the coherent excitation and, in such condition, the XOR (and NXOR) gates are observed (Fig. 2). The XOR gate is a key element to ALU as it performs the binary addition of two bits. When combined with the

AND gate, that corresponds to the carry function, the first arithmetic Boolean function, the full adder, can be envisioned. We will show the first experimental demonstration that the same DH cavity can be robustly driven to perform the 2-input, 2-output 1-bit full-adder ALU (Fig. 3). This first proof-of-concept demonstrates that complex all-optical Boolean computing can be implemented in our compact interconnect-free plasmonic cavity without expanding its footprint. [4]

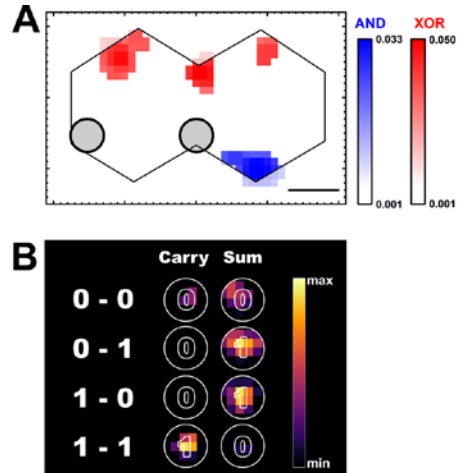


Fig. 3. Experimental simultaneous realization of the AND and XOR gates in the DH cavity. (A) Boolean contrast map showing the spatial distributions of both gates. Input ports are marked with grey circles. Input polarizations are 0° ("0") and 40° ("1"). Scale bar is 500 nm. (B) 1-bit full adder table of truth where the input intensity of the Sum and Carry signals are shown for all four input configurations corresponding to $0+0=0$, $0+1=1$ and $1+1=2$ ("10" in binary) additions.[4]

4 Conclusion and outlook

Further development towards more complex Boolean functions will require a better theoretical description of the near-field transduction into nPL and, more critically, a new paradigm for the design of the cavity shape and optimal excitation/detection configurations. A multi-objective evolutionary optimization approach does provide an efficient way of optimizing the driving parameters to operate the ALU. Yet the cavity shape remains the most challenging task in expanding the Boolean complexity of non-cascaded mono-block ALU as no rules are established that relates directly a chosen Boolean function to an optimal cavity shape.

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