



**HAL**  
open science

## **In situ and real-time investigation of the solidification of silicon by X-ray imaging**

Gabrielle Regula, Guillaume Reinhart, Isabelle Perichaud, Hadjer Ouaddah,  
Maike Becker, Thècle Riberi-Béridot, Maria Tsoutsouva, Nathalie  
Mangelinck-Noël

► **To cite this version:**

Gabrielle Regula, Guillaume Reinhart, Isabelle Perichaud, Hadjer Ouaddah, Maike Becker, et al.. In situ and real-time investigation of the solidification of silicon by X-ray imaging. 2022. hal-04287167

**HAL Id: hal-04287167**

**<https://hal.science/hal-04287167>**

Submitted on 15 Nov 2023

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# The 8<sup>th</sup> International Symposium on Advanced Science and Technology of Silicon Materials



Sponsored by The Japan Society of the Promotion of Science (JSPS)  
(The 145th Committee on Processing and Characterization of Crystals)



**November 7-9, 2022**

**Okayama Convention Center and Tenjin9, Okayama, Japan**

# The 8<sup>th</sup> International Symposium on Advanced Science and Technology of Silicon Materials

November 7-9, 2022

Okayama Convention Center and Tenjin9, Okayama, Japan

The Japan Society for the Promotion of Science (JSPS)  
The 145<sup>th</sup> Committee

## Committee

---

### General Chair

Koji Sueoka (Okayama Pref, Univ.)

### Program Chair

Shin-ichi Nishizawa (Kyushu Univ.)

### Vice Chairs

Toshinori Taishi (Shinshu Univ.)

Naoki Fukata (NIMS)

### Executive Advisory

Michio Tajima (Meiji Univ.)

Koichi Kakimoto (Tohoku Univ.)

Atsushi Ogura (Meiji Univ.)

Akira Sakai (Osaka Univ.)

### Program Committee Members

Shuichi Samata (SUMCO Corp.)

Hidekazu Tsuchida (Central Research Institute  
of Electric Power Industry)

Yukari Ishikawa (Japan Fine Ceramics Center)

Koji Izunome (GlobalWafers Japan Co.,Ltd.)

Osamu Ueda (Meiji Univ.)

Akira Uedono (Tsukuba Univ.)

Noritaka Usami (Nagoya Univ.)

Noboru Ohtani (Kwansei Gakuin Univ.)

Kazuhiko Omote (Rigaku Corp.)

Yasuhisa Sano (Osaka Univ.)

Takayoshi Shimura (Osaka Univ.)

Hidekazu Yamamoto (Chiba Inst. of Tech.)

Haruo Sudo (GlobalWafers Japan Co.,Ltd)

Yusuke Noda (Okayama Pref, Univ.)

### International advisory

John Borland (J.O.B. Technologies)

### Home Page

Satoshi Nakano (Kyushu Univ.)

### Published by

The Japan Society for the Promotion of Science (JSPS), The 145<sup>th</sup> Committee

## Preface

On behalf of the organizing committee, it is my great pleasure to welcome you to the Eighth International Symposium on Advanced Science and Technology of Silicon Materials held on November 7-9, 2022 at Okayama Convention Center and Tenjin9, Okayama, Japan. The symposium is organized by the 145th committee of the Japan Society for the Promotion of Science (JSPS). This seventh symposium follows the very successful previous symposia held in 1991, 1996, 2000, 2004, 2008, 2012 and 2016 at Kona in Hawaii and brings together internationally recognized experts in the science and technology of silicon and related materials.

The Symposium is held in hybrid due to the COVID-19 but arranged plenary and invited lectures without parallel sessions for more than 20 speakers and approximately 20 presenters with short and poster presentations, so scientific and engineering problems can be discussed at a high level.

Contributions from the sponsors, listed separately, were essential. The organizers wish to express their sincere gratitude to the corporate sponsors.

Finally, I am most grateful to all of the authors and participants for making the symposium successful. I would also like thank the members of the 145th committee for their valuable contribution and assistance. I greatly appreciate the valuable advice of Professor Akira Sakai, the previous general chair, in organizing the symposium, and the help of Professor Shin-ichi Nishizawa, program chair, in arranging these abstracts and proceedings.

October 14, 2022

Koji Sueoka  
General Chair  
Professor  
Okayama Pref, University

*Koji Sueoka*

# PROGRAM

November 7 (Monday) at Okayama Convention Center

12:00-13:00 Registration

13:15-13:30 Opening Remarks

---

## Session A

Chair: K. Sueoka (Okayama Pref. Univ.)

13:30 ~ 15:30 (Reception Hall)

- 
- 13:30 A-1 Large diameter SiC solution growth assisted by AI technology  
*Toru UJIHARA (Nagoya Univ., Japan)*
- 14:00 A-2 Standardization of Photoluminescence and Infrared Absorption Methods for Quantifying Low-Level Carbon in Si  
*Michio TAJIMA (JSNM, Japan)*
- 14:30 A-3 Gettering and Hydrogenation of Defects and Impurities in High Efficiency Silicon Solar Cells (Remote)  
*Daniel MACDONALD (The Australian National University, Australia)*
- 15:00 A-4 Ga<sub>2</sub>O<sub>3</sub> and beyond Ga<sub>2</sub>O<sub>3</sub> material of GeO<sub>2</sub> for power device  
*Kentaro KANEKO (Ritsumeikan Univ.)*
- 15:30 **Coffee Break** (Robby)

---

## Session P “Short Presentation for Posters”

Chair: S. Nishizawa (Kyushu Univ.)

15:50 ~ 17:00 (Reception Hall)

- 
- 15:50 P-1 Theoretical Study on Binding of Vacancy–Oxygen Complex (VOX) to Metals in RTP Wafers  
*H. Iwashiro (GlobalWafers Japan. Corp., Japan)*
- 15:53 P-2 Numerical Modeling and Evaluation of Constitutional Supercooling during Silicon Single Crystal Growth by Cz Method

Y. Mukaiyama (STR Japan, Japan)

- 15:56 P-3 First-principles Calculation on N-V Complex Formation in Si Crystal Growth  
A.Sada (Okayama Pref.Univ., Japan)
- 15:59 P-4 Theoretical verification of constitutional supercooling and growth conditions in heavily B-doped Si crystal growth by the Czochralski method  
Y. Fukui (Shinshu Univ., Japan)
- 16:02 P-5 A statical study of the effect of interface shape and growth time on dislocation density in multicrystalline Si  
H. Tanaka (Nagoya Univ.)
- 16:05 P-6 Formation of micro roughness during plasma chemical vaporization machining of silicon wafer and a way to reduce it  
D. Takeuchi (Osaka Univ., Japan)
- 16:08 P-7 The different Change of Dislocation Propagation in Si Wafer during High Thermal Budget Process of Impurity Doping with different Diffusion Temperatures  
J. Yuan (Kyushu Univ., Japan)
- 16:11 P-8 Evaluation of Crystal Quality by High-Speed, High-Resolution Hybrid X-ray Topography System  
K. Omote (RIGAKU Corp., Japan)
- 16:14 P-9 A TCAD Simulation Study for a New Technique to Calculate Carrier Recombination Lifetime Based on Open Circuit Voltage Decay Method  
S. Sasaki (SUMCO Corp., Japan)
- 16:17 P-10 Analysis of metal gettering in p–n junctions and effect of gettering sites inside Si wafers as starting materials for electronic device processing  
E. Kamiyama (GlobalWafers Japan, Japan)
- 16:20 P-11 Properties of a Nickel-related electronic level in multi-crystalline silicon for solar cells  
Y. Terada (Okayama Pref.Univ., Japan)
- 16:23 P-12 Effect of thermal treatment on bulk lifetime of CZ silicon wafer of solar cell

K. Tanahashi (AIST, Japan)

- 16:26 P-13 Fabrication of tensile-strained single-crystalline GeSn wires on amorphous quartz substrates by local liquid-phase crystallization  
T. Shimura (Osaka Univ., Japan)
- 16:29 P-14 Electron spin resonance study of Si dangling bond defects in stacks of LPCVD-SiN film on Si (100) substrate  
H. Miyagawa (Kagawa Univ., Japan)
- 16:32 P-15 Effect of Contact Angle between SiC and Metal Solvents on Growth Surface Morphology in Solution Growth of SiC  
T. Iwai (Shinshu Univ., Japan)
- 16:35 P-16 Evaluation of Thermal Conductivity Characteristics near Insulator/SOI Interface by Raman Spectroscopy  
K. Sahara (Meiji Univ., Japan)
- 16:38 P-17 PL spectra analyses of strain-free GeSn with high-Sn composition  
Y. Ito (Meiji Univ., Japan)
- 16:41 P-18 A linear-regression machine-learning model for predicting total energies of silicon crystal structures  
Y. Noda (Okayama Pref. Univ., Japan)
- 16:44 P-19 Development of ANN potential for Si(100) surface and validation of calculation accuracy  
M. Sato (Okayama Pref. Univ., Japan)
- 16:47 P-20 Artificial Neural Network potential analysis on self-interstitial atoms in Si  
K. Yamanaka (Okayama Pref. Univ., Japan)
- 16:50 P-22 Extension of Zeller's Silicon Power Device SEB Failure Rate Calculation method to Aviation Altitude  
S. Gollapudi (Kyushu Inst. Tech., Japan)
- 16:53 P-23 Evaluation of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystalline quality grown by crucible-free techniques  
I. Takahashi (C&A Co., Japan)
- 17:00 **Coffee Break** (Robby)

---

**Session P “Poster Session”**

Chair: S. Nishizawa (Kyushu Univ.)

17:20 ~ 19:50 (Robby)

---



---

**November 8 (Tuesday)** at Okayama Convention Center

---

**Session B**

Chair: T. Taishi (Shinshu Univ.)

9:30 ~ 10:30 (Reception Hall)

---

9:30 B-2  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal growth and device processing  
*Kohei SASAKI (Novel Crystal Technology Corp., Japan)*

10:00 B-3 Phonon properties of bulk silicon-germanium analyzed by inelastic X-ray scattering  
*Ryo YOKOGAWA (Meiji Univ., Japan)*

10:30 **Coffee Break** (Robby)

---

**Session C**

Chair: S. Nishizawa (Kyushu Univ.)

11:00 ~ 12:00 (Reception Hall)

---

11:00 C-1 Evolution of SiC material and device technologies (TBD)  
*Cengiz Balkas (Wolfspeed, USA)*

11:30 C-2 Contributions of Synchrotron X-ray Topography to the Understanding of Dislocation Configurations in SiC substrates and Epilayers  
*Michael DUDLEY (Stony Brook Univ. USA)*

12:00 Photo Session

12:15 Lunch Break

---

**Session D**

Chair: K. Kakimoto (Tohoku Univ.)

14:00 ~ 15:00 (Reception Hall)

---

14:00 D-2 Precipitation of suboxides in silicon and its impact on gettering and carrier recombination  
*Gudrun KISSINGER (IHP- Leibniz Institute for High Performance*

*Microelectronics, Germany)*

14:30 D-3 Formation Behavior of Oxygen Precipitates in Silicon Wafers Subjected to Ultra-High-Temperature Rapid Thermal Process  
*Haruo SUDO (GlobalWafers Japan, Japan)*

15:00 **Coffee Break** (Robby)

---

**Session E**

Chair: E.Kamiyama (GlobalWafers Japan)

15:30 ~ 17:00 (Reception Hall)

---

15:30 E-1 In situ and real-time investigation of the solidification of silicon by X-ray imaging (Remote)  
*Nathalie MANGELINCK-NOËL (Institute of Materials Microelectronics and Nanosciences of Provence, CNRS, France)*

16:00 E-2 Defect in cast-mono silicon (Remote)  
*Deren YANG (State Key Lab of Silicon Materials, Zhejiang University, China)*

16:30 E-3 III-N optical devices: physical processes limiting efficiency and reliability (Remote)  
*Matteo MENECHINI (University of Padova, Italy)*

17:00 E-4 Mitigation of bulk and surface recombination losses in silicon photovoltaic materials  
*John MURPHY (University of Warwick, UK)*

**18:00-20:00 Optional Dinner (ANA Hotel 19<sup>th</sup> floor “Sola”)**

---

**November 9 (Wednesday) at Tenjin9**

---

**Session F**

Chair: N. Fukata (NIMS)

9:30 ~ 11:30 (Noh Theater Hall “Tenjin9”)

---

9:30 F-1 Creation of Spin Defects in Silicon Carbide by Particle Irradiation for Quantum Applications

Takeshi OHSHIMA (QST, Japan)

10:00 F-2 Artificial-neural-network potential for accurately predicting atomic structure and physical properties of lattice defects in semiconductors

Tatsuya YOKOI (Nagoya Univ., Japan)

10:30 F-3 Characteristics and its control of white spot defects on Image Sensors

Nobuhiko SATO (Canon Inc., Japan)

11:00 F-4 Toward Silicon Quantum Computers: Challenges in Devices, Integration, and Circuits

Takahiro MORI (AIST, Japan)

11:30 **Lunch Break**

---

**Session G**

Chair: S. Nishizawa (Kyushu Univ.)

13:00 ~ 14:00 (Noh Theater Hall “Tenjin9”)

---

13:00 G-1 Silicon wafer cleaning technology

Yuji NAGASHIMA (Shibaura Mechatronics Corp., Japan)

13:30 G-2 Global electronics and semiconductor trend ~ Carbon neutral and DX change the trend~

Akira MINAMIKAWA (OMDIA, Japan)

**14:00-14:15 Closing Remarks**

# SPONSORS

The 8<sup>th</sup> International Symposium on Advanced Science and Technology of Silicon Materials will be held under the auspices of The 145<sup>th</sup> Committee of The Japan Society for the Promotion of Science (JSPS) and received financial assistance from Association for JSPS University-Industry Research Cooperation and the following companies.



<https://www.str-soft.co.jp/>

SP1



<https://www.nissin-giken.co.jp/>

SP2



GlobalWafers Japan

<http://www.sas-globalwafers.co.jp/>

SP3



<https://www.semilab-j.jp/>

SP4

*Kenix*

<http://www.kenix.jp/>

SP5



株式会社 フォトンデザイン

<http://www.photondesign.co.jp>

SP5



<https://www.sumcosi.com/english/>

SP6



<https://www.splead.jp/>

SP7

**PULSTEC**

パルステック工業株式会社

<https://www.pulstec.co.jp/en/>

SP8



<http://www.pascal-co-ltd.co.jp/index.html>

SP9



<https://www.rigaku.com/ja>

SP9



<https://www.jfe-tec.co.jp/>

SP10



<https://www.comtec.daikin.co.jp/SC/ms/>

SP10

# Invited lectures

**November 7 (Monday)**

at Okayama Convention Center Reception Hall

**13:30 ~ 15:30 Session A**

**November 8 (Tuesday)**

at Okayama Convention Center Reception Hall

**9:30 ~ 10:30 Session B**

**11:00 ~ 12:00 Session C**

**14:00 ~ 15:00 Session D**

**15:30 ~ 17:30 Session E**

**November 9 (Wednesday)**

at Tenjin9 Noh Theater Hall

**9:30 ~ 11:30 Session F**

**13:00 ~ 14:00 Session G**

**November 7 (Monday)**

# **Session A**

*Chair: K. Sueoka (Okayama Pref. Univ.)*

**13:30 ~ 15:30**  
(Reception Hall)

## Large diameter SiC solution growth assisted by AI technology

Toru Ujihara<sup>1\*</sup>

<sup>1</sup>*Institute of Materials and System for Sustainability, Nagoya University, Furo-cho, Chikusaku, Nagoya, 4648601, Japan*

e-mail: [ujihara@nagoya-u.jp](mailto:ujihara@nagoya-u.jp)

### Abstract

We use a technique called the solution method. In this method, the Si solvent is kept above 2,000 degrees Celsius, carbon is dissolved in it, and transported to the seed crystal for crystal growth. This method produces high quality crystals because there is no need to provide heat distribution. We have several key technologies for crystal growth.

### Introduction

SiC has been attracting attention as a power device material in recent years. Currently, commercially available SiC substrate crystals are grown by a sublimation method. In this method, the raw material is sublimated by heating it at high temperature and recrystallized on the seed crystal for crystal growth. This method still contains many dislocation crystals because a large temperature distribution is formed in the crystal during growth and cooling. In contrast, we develop a solution method. In this method, the Si solvent is kept above 2,000 degrees Celsius, carbon is dissolved in it, and transported to the seed crystal for crystal growth. This method produces high quality crystals because there is no need to provide large temperature distribution. In fact we have achieved high quality crystals compared to the usual common commercial crystals. With this method we have achieved crystal growth of 3 inches and now even 6 inches. We have also reached thicknesses of a few millimeters.

### Key technologies

Now, we have several key technologies for crystal growth. In the solution method, we use step bunching to reduce the dislocations present inside the crystal. We grow crystals with an off-angle on the crystal, thus making step bunching. Then, many of the threading dislocations are converted to other defects on the basal planes. By proceeding with crystal growth, these defects are swept out of the crystal. As a result, dislocation-free high-quality crystals are obtained. By the way, step bunching, while extremely important in reducing dislocations, also has a negative effect. Excessive bunching results in the formation of macro-trench defects. Such defects must be eliminated. In response, we are controlling the flow of the solution into the crystal.

When making large crystals, this flow control has a fundamental difficulty. Currently, we are growing crystals in an axisymmetric system. In that case, the solvent flow is also axisymmetric. However, the step structure is not axisymmetric. If we use a crystal with an off-angle to make step bunching, we will always get a proper flow somewhere on the crystal but a bad flow elsewhere. So we have developed a technique called switching flow. In this method, the flow from the center of the crystal to the edge and the flow from the edge to the center are realized alternately to apply the proper conditions throughout the crystal. By using this method, we have been able to obtain similar surface topography regardless of location.

Controlling the flow in a solvent is not easy. We cannot actually control the flow directly, nor can we directly observe it. Generally, the only way is to predict the flow by simulation. However, it is also extremely difficult to



control arbitrary flow by simulation. The reason for this is that there are many parameters that affect crystal growth. It is very difficult for humans to experimentally find the conditions that create multiple suitable flows. That is why we have developed the digital twin technique. With this technique, a copy of the experimental setup is first made in a computer. We then conduct the experiment, determine the optimal parameters, and perform the actual experiment. Because we can have thousands or tens of thousands of devices in the computer, we can try very large combinations of parameters and immediately derive the desired flow conditions. This is made as follows. Using these simulation data, a neural network that predicts internal temperature distribution and other parameters is constructed by machine learning. This shows that calculations that take about an hour in simulation can be completed in a fraction of a second in prediction.

Now, with such a digital twin, we can then define the objective function to find the experimental parameters that achieve the optimal flow and temperature distribution through optimization. In fact, we were able to achieve 3-inch crystals in about one year in this way. Furthermore, we can also immediately obtain experimental conditions for 6-inch crystals, and by realizing multiple flows in this way, we have succeeded in growing 6-inch crystals, and recently we are trying to grow 8-inch crystals as well.

## Standardization of Fourier-Transform IR Absorption and Photoluminescence Methods for Quantifying Low-Level Carbon in Si

Michio Tajima<sup>1,2,3,4\*</sup>

<sup>1</sup>*Japan Society of Newer Metals, Tokyo 105-0011, Japan*

<sup>2</sup>*Institute of Space and Astronautical Science/JAXA, Sagami-hara 252-5210, Japan*

<sup>3</sup>*NPERC-J, Tokyo 103-0024, Japan*

<sup>4</sup>*Meiji University, Kawasaki 214-8571, Japan*

e-mail: tajima@meiji.ac.jp, tajima@nperc-j.or.jp, tajima@isas.jaxa.jp

### Abstract

The Fourier-transform IR absorption (FT-IR) at room temperature and the photoluminescence (PL) spectroscopy at liquid He temperature after electron irradiation have been standardized based on their round-robin tests for quantifying residual C impurities in Si crystals in the concentration range of  $10^{14}$ - $10^{15}$  cm<sup>-3</sup>. Essential features of the standardized FT-IR method are the requirements of the baseline flatness less than 0.0005 and the sample thickness uniformity less than 0.001 mm to realize the detection limit of  $5 \times 10^{14}$  cm<sup>-3</sup>. For the PL method, the experimentally obtained relationship between the C concentration and the ratio of the G-line to the intrinsic emission agrees with the theoretical relationship, and can be used as a universal calibration curve for the quantification. The applicable lower level and relative root mean square deviation from secondary ion mass spectroscopy are  $5 \times 10^{14}$  cm<sup>-3</sup> and 26% for the FT-IR method and  $1 \times 10^{14}$  cm<sup>-3</sup> and 16% for the PL method.

### Introduction

Silicon power devices are attracting attention as key devices for realizing a low-carbon society. The state-of-the-art Si power device like an insulated gate bipolar transistor (IGBT) requires high quality Si wafers with long carrier lifetime [1,2]. Large-diameter magnetic-field applied Czochralski (MCZ) crystals are advantageous from the view point of productivity in comparison with floating-zone (FZ) crystals [3-5]. MCZ crystals contain more than an order of higher O impurities than FZ crystals. Small amount of residual C impurities behave as nucleation sites for O precipitates which act as recombination centers reducing the carrier lifetime [6,7]. In addition, in the IGBT device process, lifetime control by C-O complexes and formation of n-type buffer layers using high-energy particle irradiation are utilized. Therefore, strict control of C and O impurity concentrations together with the irradiation conditions are required [1-3,8]. Under these circumstances, the standardization is eagerly sought for quantifying low-level C impurities that stipulate material specifications, which serve as an interface between material suppliers and device manufacturers.

The most conventional technique for C quantification is infrared (IR) absorption method [9], which were standardized by JEITA [10] and SEMI [11]. Currently Fourier-transform IR absorption spectroscopy (FT-IR) is generally used. The detection limits stipulated by the JEITA and SEMI standards are  $2 \times 10^{15}$  cm<sup>-3</sup> and  $5 \times 10^{15}$  cm<sup>-3</sup>, respectively, at room temperature, which are an order of magnitude higher than the concentration requested for the wafers for recent devices. Although low-temperature measurements improves the detection limit [12], it is not necessarily easy for semiconductor manufacturers to implement them. Photoluminescence (PL) measurement at liquid He temperature after the introduction of C-related radiation damage has been proposed as a promising method

to detect C in the concentration range of  $10^{13}$ - $10^{15}$   $\text{cm}^{-3}$  [13-17]. In response to these situations, Working Group of the FT-IR and PL methods were organized in January 2017 in Material Standards Study Group for Semiconductor Supply-Chain (M4S), Japan Society of Newer Metals (JSNM) with an intention of standardizing the FT-IR and PL methods, where the Working Group consisted of wafer vendors, poly Si suppliers, device makers, analysis companies, equipment companies, academic experts, and administrative officers. The activity has been supported by the project “Acquisition and Promotion of International Standards for Energy Saving” planned by Ministry of Economy, Trade and Industry (METI) since June 2018. This paper describes the features of the newly developed FT-IR and PL methods and their standardization based on the round-robin tests (RRT). We discuss the accuracy and reliability of the methods.

## Room-temperature FT-IR method

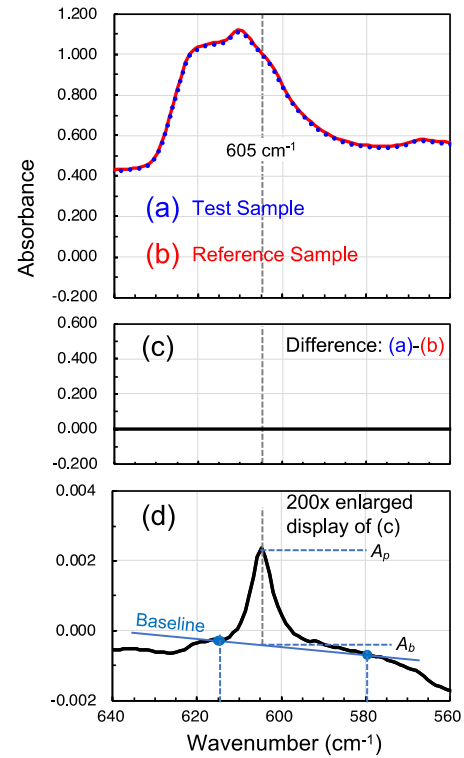
### Principle of the method

Carbon impurity atoms occupy substitutional sites in Si crystals and induce local vibrational mode (LVM) absorption at  $605 \text{ cm}^{-1}$  at room temperature [9]. This LVM absorption is used to quantify the C impurities on the basis of the established relationship between the absorption coefficient,  $\alpha$  and C concentration,  $N_C$  [10,11].

$$N_C = 8.2 \times 10^{16} \alpha \text{ (cm}^{-3}\text{)}$$

This absorption is overlapped by the strong and wide two-phonon (TO+TA) absorption with an absorption coefficient of approximately  $9 \text{ cm}^{-1}$  at room temperature [18]. From Eq. (1)  $\alpha$  for the target detection limit of  $N_C = 5 \times 10^{14} \text{ cm}^{-3}$  is calculated to be  $6.1 \times 10^{-3} \text{ cm}^{-1}$ , which is about 1/1500 of the two-phonon absorption. Because this strong two-phonon absorption reduces transmitted light, the detection limit cannot be improved by using a thick sample. The thickness of 2 mm is practically optimal and is specified in current standards [10,11].

Figure 1(a) shows the absorbance spectrum of a 2 mm thick Si test sample with  $N_C = 3.3 \times 10^{15} \text{ cm}^{-3}$ , where the spectrum is governed by the strong two-phonon absorption and the C absorption is unobservable. Differential absorption spectroscopy is commonly used to detect the weak C absorption: The absorbance spectrum of the test sample is subtracted by the spectrum of the reference sample with the negligible C concentration. The spectrum of the reference sample with very low C concentration ( $N_C = 1.2 \times 10^{14} \text{ cm}^{-3}$ ) is shown in Fig. 1(b), and little difference is discernible between the two spectra. Correspondingly, the subtracted (difference) spectrum shown in Fig. 1(c) is almost flat at zero in this scale. If the vertical scale is magnified 200 times, the C absorption peak appears as shown in Fig. 1(d). Note that the spectra shown here were taken properly following the procedure of the proposed method



**Fig. 1.** Detection of C absorption peak at  $605 \text{ cm}^{-1}$  buried in strong two-phonon absorption near  $610 \text{ cm}^{-1}$  by differential absorption spectroscopy. Absorbance spectra of (a) Si test sample with  $N_C = 3.3 \times 10^{15} \text{ cm}^{-3}$  and (b) C-lean reference sample. (c) Difference absorbance spectrum between test and reference samples. (d) 200 times enlarged display of difference absorbance spectrum in (c). C peak height ( $A_p - A_b$ ) is determined using baseline from  $615$  to  $580 \text{ cm}^{-1}$ . (1)

described in this paper. Otherwise, the magnified spectrum would generally contain unidentified large fluctuations.

Examples of the difference spectra for samples 5, 6 and 7 are shown in Fig. 2, where the specifications of the samples are summarized in Table 1. The C peak was clearly discernible for all the samples. To determine the absorption of the C peak,  $\alpha$ , the baseline from 615 to 580  $\text{cm}^{-1}$  is drawn on the absorbance spectrum following the JEITA standard [10]. The  $\alpha$  value is given by

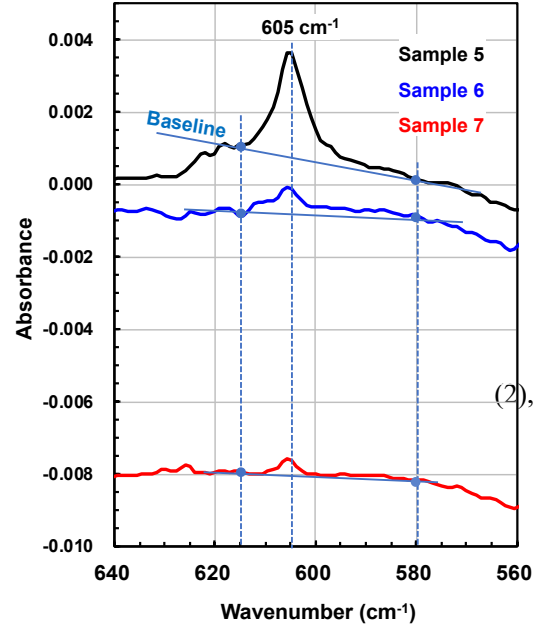
$$\alpha = \frac{23.03}{X} (A_p - A_b) \quad (2),$$

where  $X$  is thickness of a test sample in mm, and  $A_p$  and  $A_b$  are peak and baseline values of absorbance spectrum, respectively. Since the  $(A_p - A_b)$  value corresponding to the target detection limit of  $N_C = 5 \times 10^{14} \text{ cm}^{-3}$  for 2 mm thick test sample is calculated to be  $5.3 \times 10^{-4}$ , the baseline flatness should be less than 0.0005 in the baseline range from 615 to 580  $\text{cm}^{-1}$  [19]. Possible factors that deteriorate the baseline flatness are (1) instability of the FT-IR spectrometer including the replacements of test and reference samples, (2) thickness nonuniformity of test and reference samples, (3) free carrier absorption [20], (4) poor optical quality of sample surfaces. Factors (3) and (4) can be eliminated by using samples with resistivity higher than 10  $\Omega\text{-cm}$ , and by advanced mirror-polishing technique, respectively. In the following sections we discuss the factors (1) and (2).

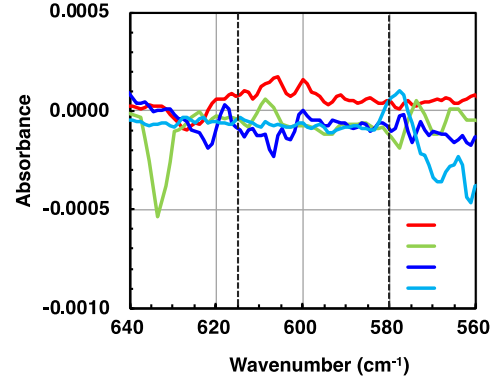
### Stability of the measurement system

The stability of the FT-IR spectrometer itself can be checked by a comparison of background single beam spectra taken twice at a regular interval with no sample mounted. The ratio of the two spectra and the common logarithm of the reciprocal of this ratio are generally termed 100% line and blank baseline, respectively. The blank baseline is used to examine the stability of the spectrometer alone.

We define a Si/Si baseline to check the stability of the FT-IR spectrometer including sample loading and unloading [19]. A sample with specifications similar to the test sample is prepared. The absorbance spectrum of the sample is obtained from the measurements of single beam spectrum of the background and the sample. Next, the sample is unloaded, and then the absorbance spectrum of the same sample is obtained from the measurements of the single beam spectrum of the background and the re-loaded sample in the same manner. The difference between these two absorbance spectra is defined as the Si/Si baseline. The Si/Si baseline is flat at zero, if the spectrometer is ideally stable, and the reproducibility of mounting the sample is perfect. If the spectrometer fluctuates and/or the



**Fig. 2.** Difference absorbance spectra for samples 5, 6 and 7 with C concentration of  $3.3 \times 10^{15}$ ,  $7.1 \times 10^{14}$  and  $5.7 \times 10^{14} \text{ cm}^{-3}$ , respectively.



**Fig. 3.** Si/Si baselines measured by four organizations (A - D). All the baselines satisfy the required flatness less than 0.0005 in the baseline range from 615 to 580  $\text{cm}^{-1}$ .

reproducibility of sample mounting is incomplete, a deviation from zero occurs and the flatness is disturbed.

As we described in the preceding section, the baseline flatness should be less than 0.0005 in the baseline range from 615 to 580  $\text{cm}^{-1}$  to realize the detection limit of  $N_C = 5 \times 10^{14} \text{ cm}^{-3}$  for 2 mm thick sample. We propose that the Si/Si baseline is a quite useful index for examining the stability of the measurement system during the measurements of the absorbance spectra of the test and reference samples in differential absorption spectroscopy. To our knowledge the concept of the Si/Si baseline has never been reported so far. The Si/Si baselines measured by four organizations (A - D) participated in the present RRT are shown in Fig. 3. It turned out that the required flatness was satisfied by the four organizations. Actually three more organizations participated in the RRT, but did not meet the requirement of the Si/Si baseline.

Here we point out the effect caused by the nonuniformity of the sample thickness in determining the C absorbance peak height [19]. The error induced by the nonuniformity  $\Delta$  in mm is estimated to be  $\alpha_B \Delta / 23.03$ , where  $\alpha_B$  is the absorption coefficients of the two-phonon absorption band. To realize the detection of the C peak for  $N_C = 5 \times 10^{14} \text{ cm}^{-3}$  the error must be smaller than 0.0005. Substituting  $\alpha_B = 9 \text{ cm}^{-1}$  gives  $\Delta < 0.0013 \text{ (mm)}$ , resulting in the requirement of “thickness uniformity of samples should be less than 0.001 mm.”

### Round-robin test

We performed RRT of the FT-IR measurement for samples listed in Table 1. They were divided into three groups, two MCZ wafers groups, **a** and **b**, and one FZ wafers group **c**, where the wafers in each group were sliced from the same ingot. A reference sample with the C concentration of  $1.2 \times 10^{14} \text{ cm}^{-3}$  was used for the differential absorption spectroscopy. All the samples were mirror-polished with the thickness of  $2.00 \pm 0.01 \text{ mm}$  and with the thickness uniformity of less than 0.001 mm. To make quantitative comparison with secondary ion mass spectroscopy (SIMS) and PL spectroscopy small chips of the samples were cut out from the adjacent part of the FT-IR samples.

The measurement conditions were basically in accordance with JEITA and SEMI standards [10,11] except for the conditions affecting the baseline flatness. Table 1 summarizes the absorption coefficients for samples 1-10 taken by organizations A-D, together with their average ( $\bar{\alpha}$ ), standard deviation ( $\sigma$ ) and relative standard deviation (RSD). The relative root mean square (RMS) deviation of the C concentration between the FT-IR and SIMS values was 26%. The reproducibility of the FT-IR measurement was examined by three organizations A-C for three times for sample 3. The RSD values of absorption coefficients ranges from 5 to 11% for the three organizations. These results indicate that C can practically be quantified down to  $5 \times 10^{14} \text{ atoms/cm}^3$ .

**Table 1.** Specifications of Si samples 1-10, their FT-IR RRT results by organizations A-D, and comparison of C concentration among FT-IR, SIMS and PL measurements.

No.	Vender	Method	Type	$\rho$ ( $\Omega\text{cm}$ )	[O] ( $\text{cm}^{-3}$ )	RRT of $\alpha$				Statics of $\alpha$			[C] ( $\text{cm}^{-3}$ )		
						A	B	C	D	$\bar{\alpha}$	$\sigma$	RSD (%)	FT-IR Ave	SIMS	PL
1	a	MCZ	n	12	2.9E+17	0.012	0.012	0.010	-	0.011	0.001	10	9.4E+14	1.1E+15	1.3E+15
2	a	MCZ	n	14	2.0E+17	0.007	0.008	0.004	-	0.006	0.002	33	5.1E+14	6.5E+14	7.8E+14
3	a	MCZ	n	16	1.5E+17	0.004	0.007	0.003	-	0.005	0.002	45	3.9E+14	4.2E+14	6.2E+14
4	a	MCZ	n	17	1.6E+17	0.002	0.005	0.003	-	0.003	0.002	46	2.7E+14	3.6E+14	4.7E+14
5	b	MCZ	n	>1000	1.1E+17	0.031	0.033	0.032	0.018	0.029	0.007	25	2.4E+15	3.3E+15	2.6E+15
6	b	MCZ	n	>1000	1.3E+17	0.006	0.007	0.005	0.005	0.006	0.001	17	4.7E+14	7.1E+14	5.9E+14
7	b	MCZ	n	>1000	1.7E+17	0.003	0.004	0.003	0.001	0.003	0.001	46	2.5E+14	5.7E+14	5.2E+14
8	c	FZ	n	41	<1.0E+16	-	0.019	0.015	0.013	0.016	0.003	20	1.3E+15	1.5E+15	(1.4E+15)
9	c	FZ	n	43	<1.0E+16	-	0.017	0.016	0.013	0.015	0.002	14	1.3E+15	1.4E+15	(1.2E+15)
10	c	FZ	n	45	<1.0E+16	-	0.013	0.010	0.007	0.010	0.003	30	8.1E+14	9.9E+14	(7.4E+14)

## PL method

### Principle of the method

The high-energy-particle irradiation produces the interstitial C and substitutional C complex ( $C_i-C_s$ ) and the  $C_i$  and interstitial O complex ( $C_i-O_i$ ), which are responsible for the strong PL emission of the G-line at 0.969 eV (1279 nm) and the C-line at 0.789 eV (1572 nm), respectively [21,22]. Quantitative analysis of the C impurities has been proposed based on the positive correlations between the C concentration and the G-line intensity.<sup>10-17)</sup> We used the intensity ratio between the G-line and band-edge emission line  $\{I_{TO}(FE)\}$  as an index of the C concentration to suppress the deviation caused by the differences in the surface condition of the samples and in the measurement conditions [23], following the standard procedure of the PL method for the quantification of donor and acceptor impurities [24,25].

### Round-robin test [26]

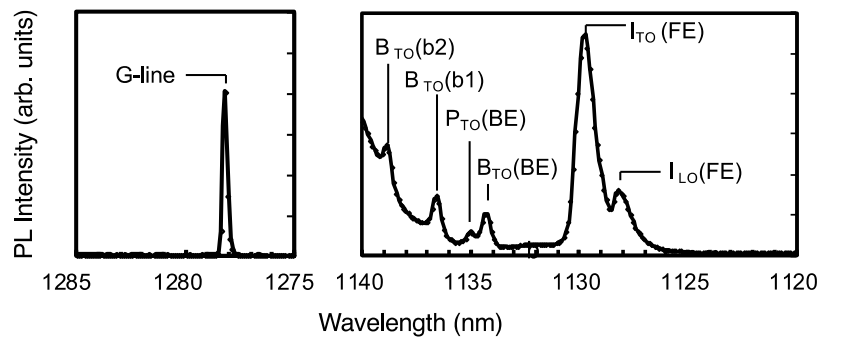
The first RRT was performed on MCZ wafers for IGBTs listed in Table 2, where the samples were irradiated with 1 MeV electrons with a fluence of  $1 \times 10^{15} \text{ cm}^{-2}$ . The samples contained O and C impurities in the range of  $1-2 \times 10^{17} \text{ cm}^{-3}$  and  $1 \times 10^{14}-3 \times 10^{15} \text{ cm}^{-3}$ , where the O concentration,  $N_O$ , were determined by FT-IR using the conversion factor IOC-88 [27,28] and  $N_C$  by SIMS, respectively. Ten organizations (#1 - #10) participated in PL RRT. The samples were immersed in liquid He and irradiated by the 532-nm-laser line with a beam diameter of 2.5 mm and a power of 50 mW on a sample surface.

Typical PL spectra of the G-line and  $I_{TO}(FE)$  line from sample G1 are shown in Fig. 4. The G-line intensity ratios ( $G/I_{TO}$ ) reported by all the organizations were plotted against the C concentration on a log-log scale for all the samples in Fig. 5(a). We found that a positive correlation holds for all the organizations and that the correlations look very similar among the organizations. To examine the similarity of the correlations we normalized the G-line intensity ratios of the respective samples by the ratio of the sample G1, denoted  $[G/I_{TO}]_N$ , and re-plotted against the C concentration in Fig.

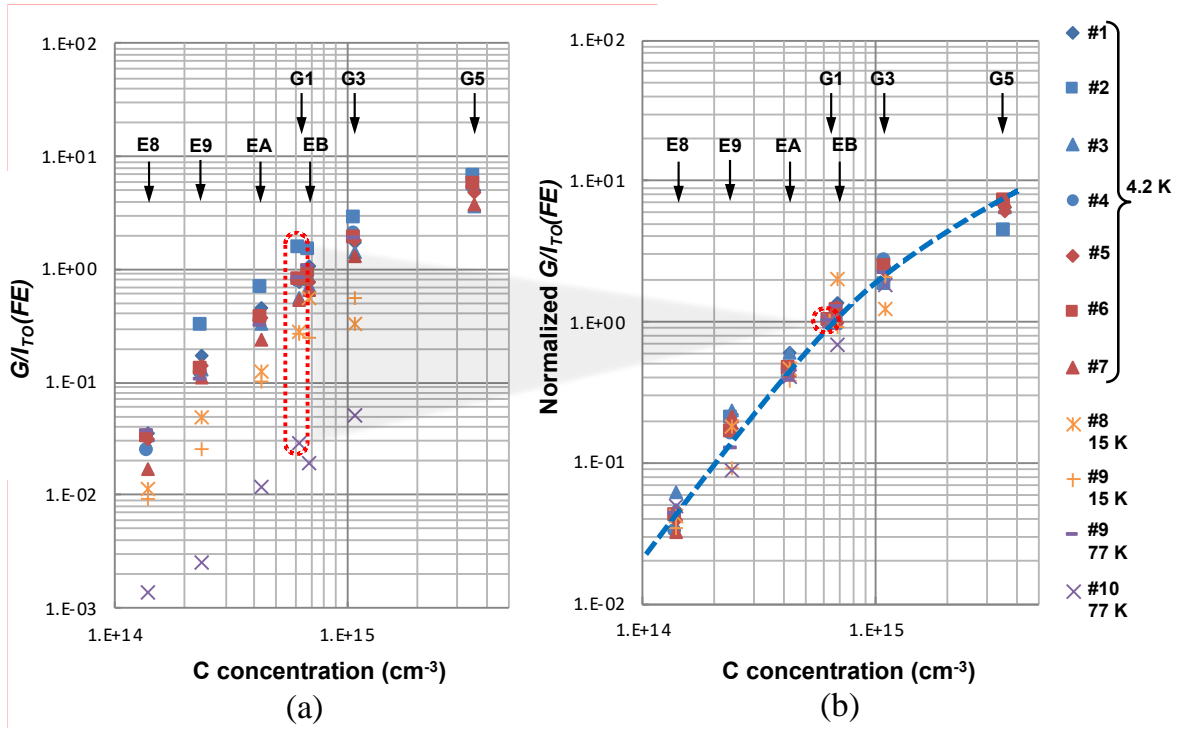
5(b). The reason why we chose the sample G1 as a reference sample was that its C concentration was around the middle value in the present samples. All the data points were on or very close to a single curve. This leads us to suggest that the correlation is universal and that the C concentration relative to the reference sample G1 can be

**Table 2.** Specifications of MCZ-Si samples for PL RRT.

No.	Cond. Type	$\rho$ ( $\Omega \cdot \text{cm}$ )	O conc. by FT-IR ( $\text{cm}^{-3}$ )	C conc. by SIMS ( $\text{cm}^{-3}$ )
E8	n	50~70	1.5E+17	1.4E+14
E9				2.4E+14
EA				4.3E+14
EB				6.9E+14
G1	p	5300	1.6E+17	6.3E+14
G3		5200	1.5E+17	1.1E+15
G5		1410	2.1E+17	3.6E+15



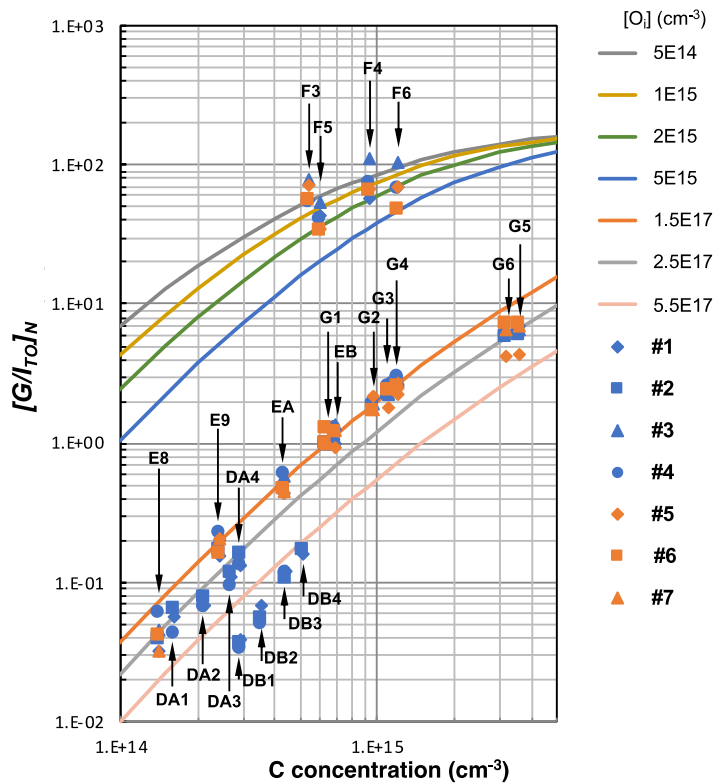
**Fig. 4.** PL spectra at 4.2 K of G-line and band-edge emission from sample G1 after 1 MeV electron irradiation. Notations of lines are given in Ref. 26.



**Fig. 5.** Correlation between C concentration and (a) G-line intensity ratio ( $G/I_{TO}(FE)$ ) for MCZ samples listed in Table 2, and (b)  $G/I_{TO}(FE)$  normalized by the ratio of reference sample G1 based on PL RRT by 10 organizations (#1 - #10).

determined using this correlation as a calibration curve.

Note that the PL measurement conditions were not strictly settled at the present RRT, although the standard procedures were recommended. Some organization used higher or lower spectral resolution. The calibration of spectral response of the measurement system was not requested, although the response differed greatly depending on detectors, gratings, filters and so on. Most organizations performed the measurement at 4.2 K (organization #1-#7) but some at 15 K and 77 K (organization #8-#10). In spite of the loose settlement of the conditions the universal correlation was obtained. It is surprising that the data taken at 15 K and 77 K were also located very close to the identical curve, as depicted in Fig. 5(b). This indicates the potential superiority of the present method.



**Fig. 6.** Theoretical relationships between  $N_C$  and  $[G/I_{TO}]_N$  for MCZ ( $N_O = 1.5 - 5.5 \times 10^{17} \text{ cm}^{-3}$ ) and FZ ( $N_O = 0.5 - 5 \times 10^{15} \text{ cm}^{-3}$ ) samples. PL RRT results by organizations #1-#7 are overlaid.

The detection limit of the method was estimated to be approximately  $4 \times 10^{13} \text{ cm}^{-3}$  [29].

### Calibration curve correction due to oxygen concentration variation [30]

The obtained calibration curve in Fig. 5(b) is applicable only for the samples with  $N_O = 1-2 \times 10^{17} \text{ cm}^{-3}$ . In order to verify the validity of the curve and expand its application range, a second RRT was performed on MCZ (group DA with  $N_O = 2.5 \times 10^{17} \text{ cm}^{-3}$  and group DB with  $N_O = 5.5 \times 10^{17} \text{ cm}^{-3}$ ) and FZ samples (group F with  $N_O \leq 5 \times 10^{15} \text{ cm}^{-3}$ ) by seven organizations (#1 - #7). The data points after the normalization with sample G1 are plotted in Fig. 6, where the results of the first RRT is also plotted.

The G-line intensity can be theoretically calculated using  $N_C$  and  $N_O$  and electron beam irradiation dose as parameters from the defect reaction during electron beam irradiation [14]. The solid lines in Fig. 6 indicate  $[G/I_{TO}]_N$  calculated for  $N_O = 1.5-5.5 \times 10^{17} \text{ cm}^{-3}$  for the MCZ sample and  $N_O = 0.5-5 \times 10^{15} \text{ cm}^{-3}$  for the FZ sample, where  $[G/I_{TO}]_N$  for  $N_C$  and  $N_O$  of sample G1 is set to one corresponding to the normalization process. The data points of the groups E, G, DA, and DB are located on or very close to the theoretical curves with  $N_O$  values of 1.5, 2.5, and  $3.5 \times 10^{17} \text{ cm}^{-3}$ , respectively. Those of the group F are also located near the theoretical curve of  $N_O = 0.5-5 \times 10^{15} \text{ cm}^{-3}$  expected for FZ crystals. The fact that all data points come close to the theoretical curves without adjusting the parameters for each groups demonstrates the validity of the theoretical formula, and is a noteworthy advantage. The theoretical calibration curves are given by

$$[G/I_{TO}]_N = 2.520 \times 10^{-30} \times N_C^2 \times (1.5 \times 10^{17} / N_O) \quad \text{for } [G/I_{TO}]_N \leq 1 \quad (3),$$

$$[G/I_{TO}]_N = \{-1.457 \times 10^{-32} \times N_C^2 + 2.825 \times 10^{-15} \times N_C - 7.7384 \times 10^{-1}\} \times (1.5 \times 10^{17} / N_O) \quad \text{for } [G/I_{TO}]_N > 1 \quad (4).$$

We applied the PL method to 16 MCZ samples independent of the present calibration procedure and found that the relative RMS deviation from SIMS values was 16%. This allows us to suggest that the PL method can be used as a standard technique for determining low-level C concentrations in MCZ Si crystals.

### Comparison of C quantification by FT-IR, PL and SIMS

For samples 1-10 in Table 2, the C concentrations by the FT-IR and PL methods are plotted against those by the SIMS analysis in Fig. 7, where the  $N_O$  of the FZ samples is assumed to be  $5 \times 10^{15} \text{ cm}^{-3}$  for the PL analysis. Almost all data points are within 30% deviation from the SIMS values. It can be said that the quantitative agreement of the C concentration in the range down to  $5 \times 10^{14} \text{ cm}^{-3}$  is a remarkable achievement. Table 3 summarizes sample requirements, applicable concentration ranges, and other characteristics for FT-IR and PL methods.

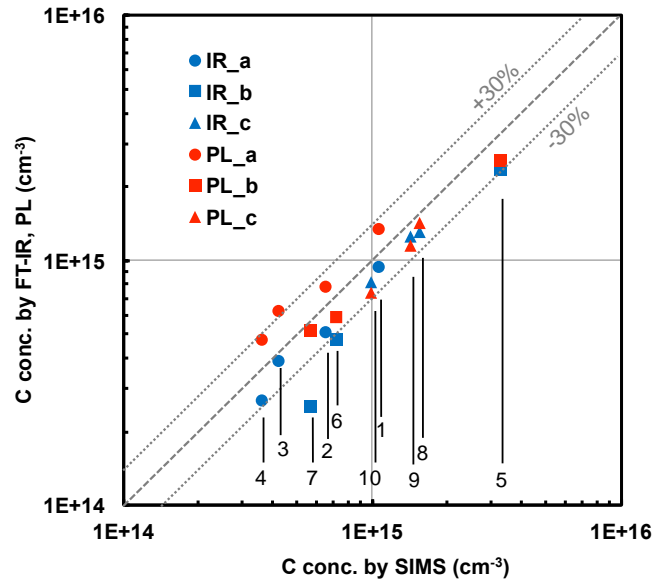


Fig. 7. C concentrations of samples 1-10 by FT-IR and PL methods are plotted against those by SIMS analysis. Blue and red symbols represent FT-IR and PL data, respectively.



## Conclusion

As a result of the present standardization process, it is shown that the C concentration can be determined down to  $5 \times 10^{14} \text{ cm}^{-3}$  with relative RMS error of 26% by the FT-IR method and down to  $1 \times 10^{14} \text{ cm}^{-3}$  with relative RMS error of 16% by the PL method. We believe that the FT-IR and PL methods are practically effective as reliable "measures" for characterizing wafer quality. Currently, we are making efforts toward the establishment of Japanese Industrial Standard (JIS) for the FT-IR and PL methods.

When the author first participated in this project, the FT-IR method focused on how to extract a minute C peak from a noisy absorbance spectrum, and concentrated on reducing noise by increasing the accumulation times. The author proposed a new definition of the Si/Si baseline as a measure of stability, since the stability of the instrument during a series of measurements is the key to the differential spectroscopy. As a result, the target detection limit was achieved. For the PL method, its high sensitivity was well known, but the bottleneck was the need to prepare several calibration curves depending on the specifications of the samples. Regarding this, it was demonstrated that the applicable range of the calibration curve is greatly expandable by faithfully following the theoretical equation based on the defect reaction. Through these processes, the author has realized the importance of returning to the basics and carefully accumulating data collection and analysis.

## Acknowledgements

The author would like to express sincere thanks to all the members of Working Groups in M4S in JSNM for cooperative works for the standardization including RRT since 2017. This work was partly supported financially by METI under the project "Acquisition and Promotion of International Standards for Energy Saving" since 2018. This paper describes the findings gained during the course of this project and lays the basis for the new standards for the FT-IR and PL methods.

## REFERENCES

- [1] T. Minato, K. Takano, and A. Kiyoi, Proc. Science and Technology of Silicon Materials 2018, S3-4 (2018).
- [2] J. Nishizawa, Proc. Science and Technology of Silicon Materials 2018, S3-3 (2018).
- [3] H.J. Schulze, H. Öfner, F.-J. Niedernostheide, J. G Laven, H.P. Felsl, S. Voss, A. Schwagmann, M. Jelinek, N. Ganagona, A. Susiti, T. Wübben, W. Schustereder, A. Breymesser, M. Stadtmüller, A. Schulz, T. Kurz, and F. Lükermann, Proc. 28th Int. Symp. Power Semicond. Devices & IC's (ISPSD) 2016, p. 355.
- [4] Y. Nagai, S. Nakagawa, and K. Kashima, J. Cryst. Growth, **401**, 737 (2014).
- [5] M. Higasa, Y. Nagai, S. Nakagawa, and K. Kashima, ECS Trans. **72** [4], 57 (2016).
- [6] S. Kishino, Jpn. J. Appl. Phys. **21**, 1 (1982).
- [7] B. O. Kolbesen and A. Mühlbauer, Solid-State Electron. **25**, 759 (1982).
- [8] K. Takano, A. Kiyoi, and T. Minato, Proc. 27th Int. Symp. Power Semicond. Devices & IC's (ISPSD) 2015, p. 129.
- [9] R.C. Newman and J.B. Willis, J. Phys. Chem. Solids **26**, 373 (1965).

**Table 3.** Characteristics of FT-IR and PL methods for C quantification.

		FT-IR	PL
Sample	Area (mm)	approx. 20x20	approx. 5x10
	Thickness (mm)	2.00±0.01 (Uniformity ≤0.001)	approx. 0.5-1
	Surface	Both sides mirror polished	Single side mirror polished or etched
Measurement	Preprocess	None	Electron irradiation
	Temperature	Room temp.	4.2 K
	Applicable range ( $\text{cm}^{-3}$ )	5E+14~5E+15	4E+13~3E+15

- [10] JEITA EM-3503 (2002). [http://www.jsnm.or.jp/jeita/jeita\\_standard/02/](http://www.jsnm.or.jp/jeita/jeita_standard/02/)
- [11] SEMI MF-1391-1107 (Reapproved 0912) (2012).
- [12] H. Ch. Alt, Y. Gomeniuk, B. Wiedemann, and H. Riemann, *J. Electrochem. Soc.* **150**, G498 (2003).
- [13] J. Weber and M. Singh, *Appl. Phys. Lett.* **49**, 1617 (1986).
- [14] M. Nakamura, E. Kitamura, Y. Misawa, T. Suzuki, S. Nagai, and H. Sunaga, *J. Electrochem. Soc.* **141**, 3576 (1994).
- [15] S. Nakagawa, K. Hirose, and M. Tajima, *Proc. Science and Technology of Silicon Materials 2007*, p. 227 (2007).
- [16] S. Nakagawa, *Oyo Buturi*, **84**, 976 (2015) [in Japanese].
- [17] M. Tajima, *Oyo Buturi*, **90**, 699 (2021) [in Japanese].
- [18] F. A. Johnson, *Proc. Phys. Soc.* **73**, 265 (1959).
- [19] M. Tajima, H Fujimori, R. Takeda, N. J. Kawai, and N. Ishihara, *Jpn. J. Appl. Phys.* **61**, 096502 (2022).
- [20] H. Saito and H. Shirai, *J. Electrochem. Soc.*, **147**, 1210 (2000).
- [21] G. Davies, *Phys. Rep.* **176**, 83 (1989).
- [22] G. Davies and R. C. Newman, *Handbook on Semiconductors*, Vol. 3, ed. S. Mahjan (Elsevier, Amsterdam, 1994) Chap. 21, p. 1557.
- [23] M. Tajima, *Appl. Phys. Lett.*, **32**, 719 (1978).
- [24] JIS H 0615 : 2021 [in Japanese] (2021).
- [25] SEMI MF1389-1115 (Reapproved 0222) (2022).
- [26] M. Tajima, S. Samata, S. Nakagawa, J. Oriyama, and N. Ishihara, *Jpn. J. Appl. Phys.* **59**, SGGK05 (2020).
- [27] A. Baghdadi, W. M. Bullis, M. C. Croarkin, Yue-zhen Li, R. I. Scace, R. W. Series, P. Stallhofer, and M. Watanabe, *J. Electrochem. Soc.* **136**, 2015 (1989).
- [28] SEMI MF 1188-1107 (Reapproved 0718) (2018).
- [29] Y. Satake, M. Tajima, S. Asahara, and A. Ogura, *Jpn. J. Appl. Phys.* **59**, 126501 (2020).
- [30] M. Tajima, S. Samata, S. Nakagawa, Y. Shinozuka, J. Oriyama, and N. Ishihara, *Jpn. J. Appl. Phys.* **60**, 026501 (2021).

**November 8 (Tuesday)**

# **Session B**

*Chair: T. Taishi (Shinshu Univ.)*

**9:30 ~ 10:30**  
(Reception Hall)

## $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal growth and device processing

Kohei Sasaki\* and Akito Kuramata

Novel Crystal Technology, Inc., 2-3-1 Hirose-dai, Sayama, Saitama, 350-1328, Japan

e-mail: sasaki@novelcrystal.co.jp

### Abstract

Development of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices has been accelerating over the past few years. In particular, 4-inch device-quality  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epi wafers have become commercially available, and low-loss trench MOS-type SBDs, few-kV finFETs, and normally-off MOSFETs have been demonstrated. In this paper, we will explain recent progress in crystal growth techniques for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and power devices based on this material.

### 1. Introduction

Ga<sub>2</sub>O<sub>3</sub> exists in five phases. The most stable is the  $\beta$ -phase. Figure 1 shows the crystal structure of this phase, which is monoclinic. The material properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and major semiconductors are summarized in Table 1 [1].  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has a huge bandgap of 4.5-4.9 eV. The critical electric field strength is expected to be 6-8 MV/cm. Its carrier concentration can be controlled in the range of 10<sup>15</sup>-10<sup>20</sup> /cm<sup>3</sup> by Si or Sn doping [2]. The electron mobility is around 200-300 cm<sup>2</sup>/Vs. From these material properties, Baliga's figure of merit for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> reaches a huge value, 3,444. This means that ultra-low-loss power devices can be fabricated by using  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Another important feature of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is that bulk crystals can be grown using the melt growth method at low cost. Accordingly,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is an attractive material for next-generation power devices.

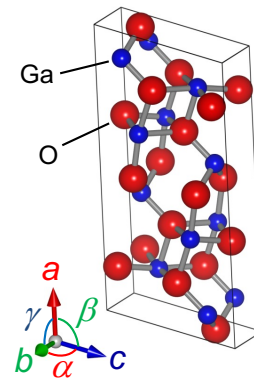


Fig. 1. Crystal structure of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

Table 1. Material properties

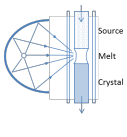
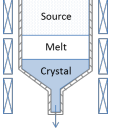
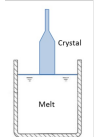
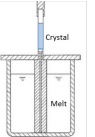
	Si	GaAs	4H-SiC	GaN	Diamond	$\beta$ -Ga <sub>2</sub> O <sub>3</sub>
Bandgap: $E_g$ (eV)	1.1	1.4	3.3	3.4	5.5	4.5-4.9
Electric field strength: $E_c$ (MV/cm)	0.3	0.4	2.5	3.3	10	8.0(est.)
Mobility: $\mu_e$ (cm <sup>2</sup> /Vs)	1,400	8,000	1,000	1,200	2,000	300(est.)
Dielectric constant: $\epsilon_s$	11.8	12.9	9.7	9	5.5	10
Baliga's FOM: $\epsilon\mu E_c^3$	1	15	340	870	24,661	3,444

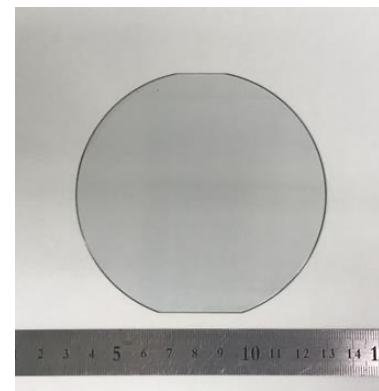
### 2. $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk crystal growth

The techniques for growing large  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk crystals include standard methods such as the Czochralski (CZ), floating zone (FZ), edge-defined film-fed growth (EFG), and vertical Bridgman (VB) method. Table 2 compares the bulk growth methods reported for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. In particular, the FZ method does not use a crucible, and it can grow

high-purity crystals. The development of the VB method has progressed rapidly in the last few years. 2-3-inch wafers have already been demonstrated. CZ is widely used for many materials to make large boules. However, in the case of  $\text{Ga}_2\text{O}_3$ , there is an issue regarding n-type doping, wherein the shape of n-doped crystals easily becomes like a coil. The development of the EFG method is the most advanced, and 100-mm wafers are commercially available (see Fig. 2). The dislocation density of 100-mm wafers is low enough, about  $10^3\text{-}10^4/\text{cm}^2$ . 150-mm wafers were demonstrated a few years ago [3]. Figures 3 (a), (b) show (a) a photograph of a 6-inch EFG system and (b) a schematic diagram of the crucible for EFG. An RF coil is used to heat the crucible, which is made of iridium. When the temperature exceeds the melting point of  $\beta\text{-Ga}_2\text{O}_3$ , the source powder starts melting. The melt goes up through a slit and reaches the top of the die. Growth is initiated by touching the seed crystal to the melt. The cross-sectional shape of the bulk crystal eventually becomes the same shape as the die.

**Table 2.** Comparison of  $\beta\text{-Ga}_2\text{O}_3$  bulk growth methods.

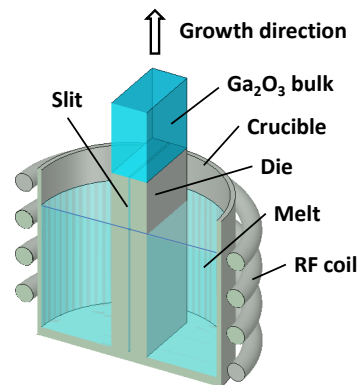
Method	FZ	VB	CZ	EFG
				
Bulk size reported	1 inch	2 inch	2 inch	6 inch
n-type doping	Possible	Possible	Difficult	Possible
Growth rate (mm/h)	5	0.5	2	15
Strong point	High purity	High quality	Large boule	Large n-type



**Fig. 2.** 4-inch  $\beta\text{-Ga}_2\text{O}_3$  single crystal substrate.



(a)



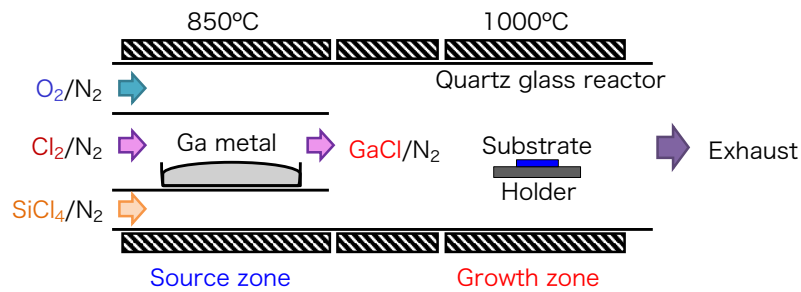
(b)

**Fig. 3.** (a) 6-inch EFG system and (b) schematic diagram of crucible of EFG.

### 3. $\beta\text{-Ga}_2\text{O}_3$ epitaxial growth

High-voltage  $\beta\text{-Ga}_2\text{O}_3$  power devices require high-quality and thick epitaxial films with a low donor concentration. The development of epitaxial growth techniques is underway using molecular beam epitaxy, halide vapor phase

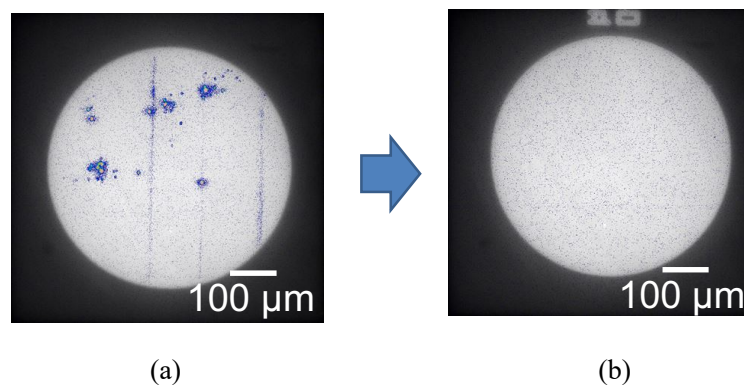
epitaxy (HVPE), metal organic chemical vapor deposition (CVD), mist CVD, etc. HVPE is the most suitable method for power-device applications because a high-purity and thick layer can be grown [4]. Figure 2 shows a schematic illustration of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> HVPE system, which was developed by Novel Crystal Technology, Inc. (NCT), the Tokyo University of Agriculture and Technology, and National Institute of Information and Communication Technology. The reactor is divided into two zones. In the source zone, GaCl is synthesized by the reaction between gallium metal and Cl<sub>2</sub> gas. In the growth zone, Ga<sub>2</sub>O<sub>3</sub> is grown by the reaction between GaCl and O<sub>2</sub>. The standard growth temperature is 1000 °C. SiCl<sub>4</sub> is used as a dopant source.



**Fig. 4.** Schematic illustration of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> HVPE system.

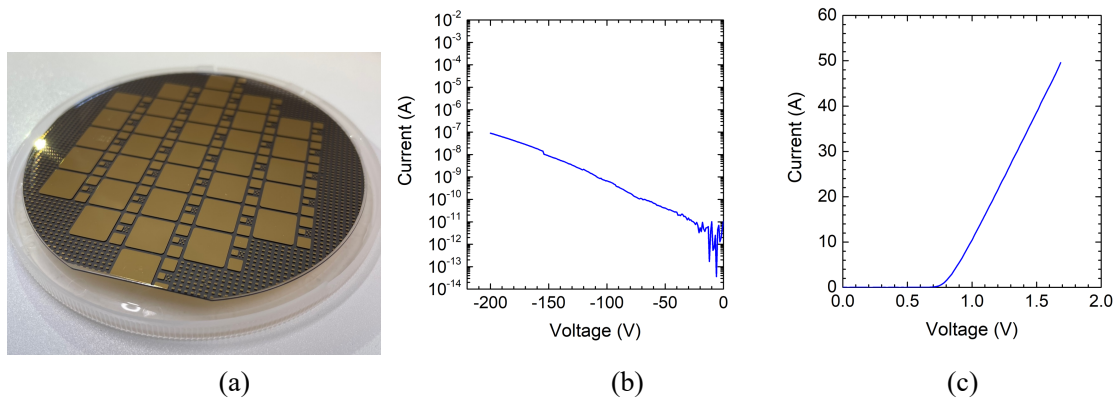
In 2017, NCT fabricated 2-inch HVPE system. However, the HVPE epi had many killer defects around 200 /cm<sup>2</sup>. The density of defects should be less than 1 /cm<sup>2</sup> in order to make a large current (over 10 A) device. One of the origins of these killer defects is polycrystalline particles of Ga<sub>2</sub>O<sub>3</sub> generated during HVPE epi-growth. Subsequent improvements to the growth conditions successfully decreased these defects.

Figure 5 shows the results of emission microscopy. Emission microscopy is an observation method for identifying leakage points, in other words the locations of killer defects. In this case, the back side of the anode electrode was observed through the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epi wafer. Figure 5 (a) and (b) show emission microscopic images of SBDs fabricated with the conventional epitaxial method (epi) and with the improved method. The size of the anode was 500  $\mu$ m, and the anode bias was set at -200 V. As can be seen, the conventionally made SBD had many emission points and line-like emissions. On the other hand, the SBD made with the improved method showed no such emissions.



**Fig. 5.** Emission microscopy images of  $\phi$ 500- $\mu$ m anode Ga<sub>2</sub>O<sub>3</sub> SBDs made by (a) conventional epi and (b) improved epi.

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs with a large 10-mm-square anode were fabricated to evaluate the killer defect density. Figure 6 (a) shows a photograph of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs fabricated on a 100-mm  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epi wafer. The epi thickness and donor concentration were about 10  $\mu$ m and  $1 \times 10^{16}$  /cm<sup>3</sup>, respectively. Figure 6 shows (b) the reverse and (c) the forward characteristics. Clear forward and reverse characteristics were obtained. Maximum applied reverse voltage was fixed at -200 V, because these SBDs have no edge termination. About 52% of the devices (16/31 devices) had characteristics matching the theoretical prediction. From the yield and anode diameter, the killer defect density was estimated to be 0.7 /cm<sup>2</sup>.



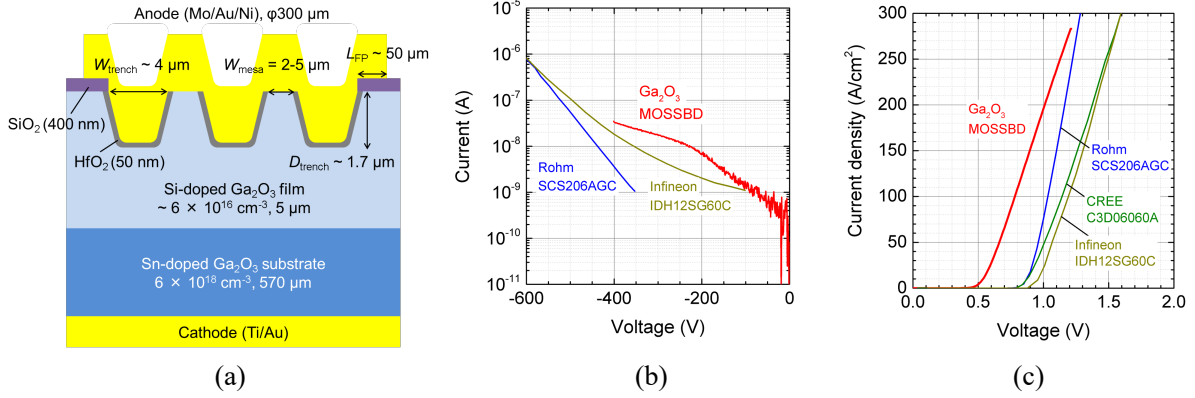
**Fig. 6.** (a) Photograph, (b) reverse and (c) forward characteristics of large 10-mm-square anode SBDs on a 100-mm  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epi wafer.

#### 4. $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs

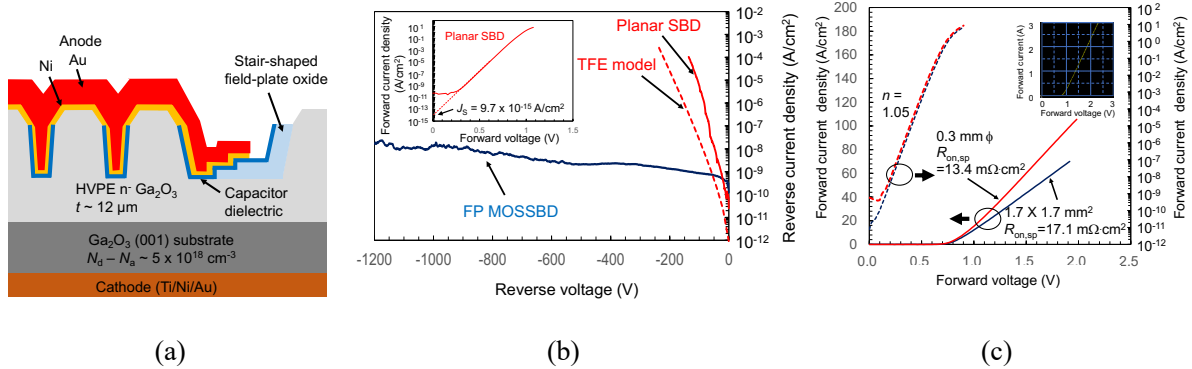
In 2017, NCT fabricated Ga<sub>2</sub>O<sub>3</sub> trench MOSSBDs [5]. By incorporating a trench structure in the SBDs, the electric field at the Schottky junction can be decreased; consequently, the leakage current can be decreased. Figure 7(a) shows a schematic illustration of a device. The anode metal is molybdenum, and the cathode metal is titanium. This device has a simple field-plate structure. The hafnium dioxide was used for the MOS junction.

Figures 7 (b), (c) shows the (b) reverse and (c) forward characteristics of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD and commercially available 600-V class SiC SBDs. The red line shows the characteristics of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD, and the other lines are those of the SiC SBDs. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD had a similar reverse leakage level to that of the SiC SBDs (Fig. 7(b)). The forward threshold voltage was almost 50% smaller than that of the SiC SBDs, and the on-resistance was of similar order. The forward voltage was 30-40% smaller than that of the SiC SBDs. These results demonstrate that the performance of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices can exceed that of SiC devices.

In 2022, NCT reported the characteristics of 1.7-mm square 1.2 kV  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBDs [6]. A stair-shaped field plate and a high-quality 2-inch Ga<sub>2</sub>O<sub>3</sub> epi wafer were used, as shown in Fig. 8(a). Figures 8 (b) and (c) show the reverse and forward characteristics. The blue line indicates the characteristics of 1.7-mm square SBDs with a trench MOS structure and red line those of SBDs without the trench structure. The MOSSBD showed a high breakdown voltage of over 1.2 kV with sufficiently low leakage current. The ideality factor was about 1.05, and the specific on-resistance was about 13-17 m $\Omega$ cm<sup>2</sup>.



**Fig. 7.** (a) Schematic illustration of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD, (b) reverse and (c) forward characteristics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD and commercially available SiC SBDs.



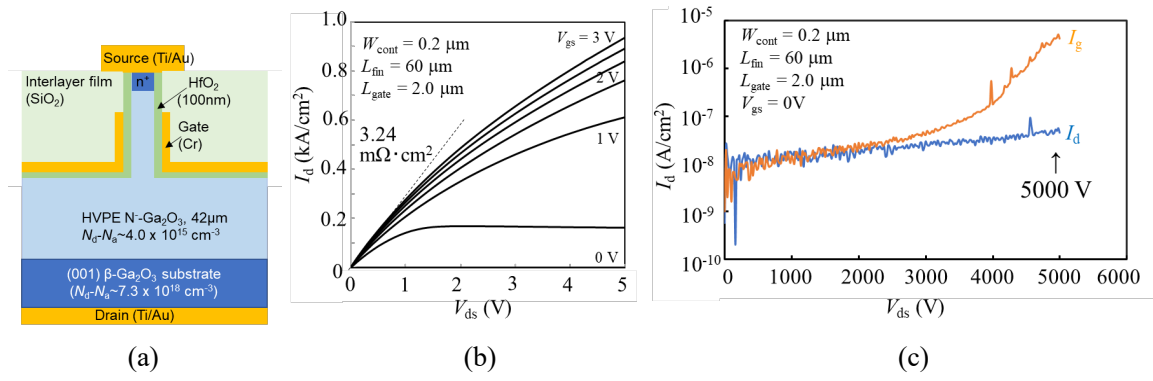
**Fig. 8.** (a) Schematic illustration of 1.2 kV  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD, (b) reverse and (c) forward characteristics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSSBD (red line) and planer SBDs (blue line).

## 5. $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs

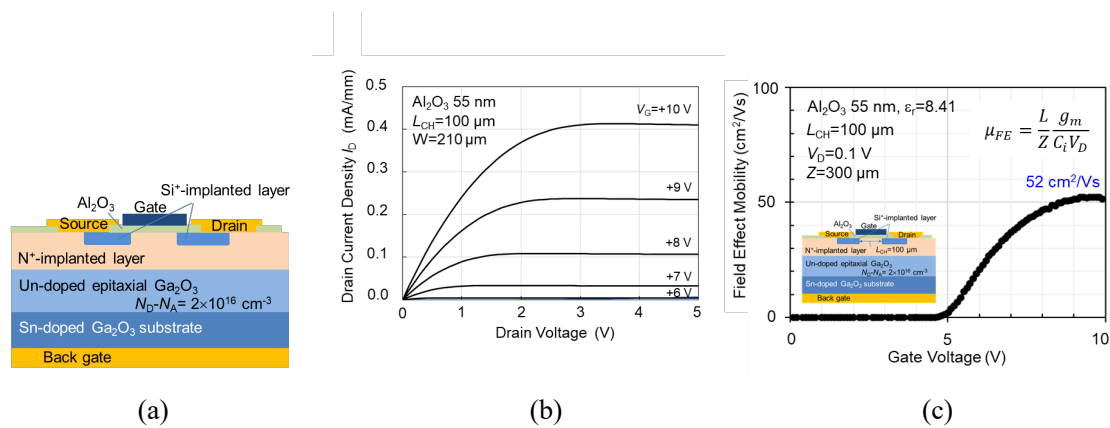
In 2021, NCT developed 5 kV  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> single FinFETs. Figure 9 (a) shows a schematic illustration of the device. The donor concentration and epi thickness were about  $4 \times 10^{15} / \text{cm}^3$  and 42  $\mu\text{m}$ , respectively. Figure 9 (b) shows the drain current-voltage characteristics. This device showed clear normally-off characteristics. However, the threshold voltage was small, only about 0.09 V. The current density was calculated from the mesa width. Specific on-resistance was about 3  $\text{m}\Omega\text{cm}^2$ . Figure 9 (c) shows a three-terminal off-state voltage waveform. The device achieved the world's highest breakdown voltage, 5.0 kV.

In 2022, NCT developed normally-off  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> DMOSFETs. Figure 10 shows a schematic illustration. The ion implantation technique was used to make a nitrogen-doped well layer and Si-doped contact layer. This device had a large enough threshold voltage, 6.2 V. Of particular note is the large field effect mobility of 52  $\text{cm}^2/\text{Vs}$ . However, the blocking voltage was small due to the large leakage current through the nitrogen-doped layer. It was thought that ion implantation damage remained in the device. In the future, the activation annealing technique should be improved in order to increase the breakdown voltage.





**Fig. 9.** (a) Schematic illustration, (b) current-voltage, and (c) three-terminal off-state characteristics of  $\beta$ - $\text{Ga}_2\text{O}_3$  single FinFET.



**Fig. 10.** (a) Schematic illustration, (b) current-voltage, and (c) field-effect-mobility characteristics of  $\beta$ - $\text{Ga}_2\text{O}_3$  MOSFET.

## 5. Conclusions

The article reviewed recent progress in  $\beta$ - $\text{Ga}_2\text{O}_3$  crystal growth for power devices. Improvements to the crystal quality of 100-150 mm  $\beta$ - $\text{Ga}_2\text{O}_3$  wafers are underway. The development of  $\beta$ - $\text{Ga}_2\text{O}_3$  SBDs and FETs is accelerating. We hope to further development toward early commercialization of  $\beta$ - $\text{Ga}_2\text{O}_3$  power devices.

## Acknowledgements

Part of this work was supported by the New Energy and Industrial Technology Development Organization (NEDO) and Innovative Science and Technology Initiative for Security, Grant Number JPJ004596, ATLA, Japan.

## REFERENCES

- [1] M. Higashiwaki et al., Appl. Phys. Lett. **100** (2012) 013504.
- [2] N. Ueda et al., Appl. Phys. Lett. **70** (1997) 3561.
- [3] A. Kuramata et al., Jpn. J. Appl. Phys. **55** (2016) 1202A2.
- [4] H. Murakami et al., Appl. Phys. Express **8** (2015) 015503.
- [5] K. Sasaki et al., IEEE Electron Device Lett. **38** (2017) 6, 783-785.
- [6] F. Otsuka et al., Appl. Phys. Express **15** (2022) 016501.

## Phonon properties of bulk silicon-germanium analyzed by inelastic X-ray scattering

Ryo Yokogawa<sup>1,2\*</sup>

<sup>1</sup> School of Science and Technology, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa 214-8571, Japan

<sup>2</sup> Meiji Renewable Energy Laboratory, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa 214-8571, Japan

e-mail: r\_yokogawa@meiji.ac.jp

### Abstract

I report on the phonon properties of bulk single-crystalline silicon-germanium (SiGe) analyzed by inelastic X-ray scattering (IXS) with synchrotron radiation. The phonon dispersion curves of bulk SiGe were investigated and an anomalous mode at low-energy region was observed directly. The phonon dispersion curves of the anomalous mode indicate that there was no momentum and Ge fraction dependence from  $\Gamma$  to X points in the Brillouin zone, indicating that the mode originated from the Ge localized vibration without propagation properties. Broadening of the acoustic phonon spectral linewidth was also observed. This behavior suggests that a change in the acoustic phonon spectral linewidth indicates a reduction in the acoustic phonon lifetime caused by the appearance of the anomalous low energy phonon dispersion, leading to suppression of the thermal transport in the SiGe alloy.

### Introduction

Silicon-germanium (SiGe) is one of the most promising semiconductor candidate materials used for next-generation thermoelectric devices [1] and electric devices [2] thanks to its much lower thermal conductivity and high hole mobility compared to bulk Si crystals, respectively. It is important for a SiGe thermoelectric devices to reveal the correlation between the phonon scattering and the thermal transport mechanism as device miniaturization proceeds to the nanometer scale. Moreover, it is indispensable for SiGe electric devices to reveal the disturb of the carrier transport by phonon scattering at high temperatures, which can be done using a mobility model [3] composed of three dispersion factors (coulomb, surface roughness, and phonon scattering).

There are several reports on the phonon scattering mechanism in the SiGe alloy explained by several simulations [4, 5]. However, the origin of the low thermal conductivity of SiGe has not been experimentally investigated in yet. In addition, the phonon properties of SiGe such as phonon dispersion curve and phonon lifetime remain mostly unclear.

Raman spectroscopy (RS) is a powerful technique for measuring phonon energy through Raman spectrum, and there are many reports on the behavior of optical phonon modes for SiGe, i.e., Ge-Ge, Si-Ge, and Si-Si modes and local vibration modes (LVMS) [6]. It is well known that the energies of these optical modes depend on the strain and Ge fraction, and the change in the position and spectral intensity are often utilized to determine the strain and Ge fraction of the alloy [7]. However, RS can only observe optical phonon modes at the Brillouin zone center and cannot bring information on acoustic phonon modes. Inelastic neutron scattering (INS) is another technique to address the phonon dispersion curves, but it generally requires large size samples from the viewpoint of the relatively weak neutron beam flux and small neutron cross sections.

Inelastic X-ray scattering (IXS) with synchrotron radiation is a powerful technique that reveals phonon energy, phonon dispersion curves, and phonon spectral linewidth, but not applied to SiGe alloys until now. In this paper, I introduce the investigation of the phonon properties such as the dispersion curves, the phonon spectral linewidth for acoustic modes to explore the origin of the low thermal conductivity of bulk SiGe alloys by IXS.

## Experiments

The single-crystalline SiGe samples for IXS were prepared by two different growth methods: the Czochralski (Cz) [8] and traveling liquidus zone (TLZ) methods [9]. I confirmed in advance by X-ray diffraction (XRD) that the samples were strain-free states. The sample information is summarized in Table 1.

The IXS measurements were performed at the BL35XU [10] and the BL43LXU [11] beamline of the SPring-8 synchrotron facility. The measurements were conducted at room temperature using reflection geometry. The incident x-ray energy was set to 17.8 and 21.7 keV, which corresponds to Si (9 9 9) reflection and Si (11 11 11) reflection, and the overall energy resolution was around 3.0 and 1.5 meV, respectively. The incident X-ray beam size was approximately  $60 \times 75 \text{ cm}^2$ .

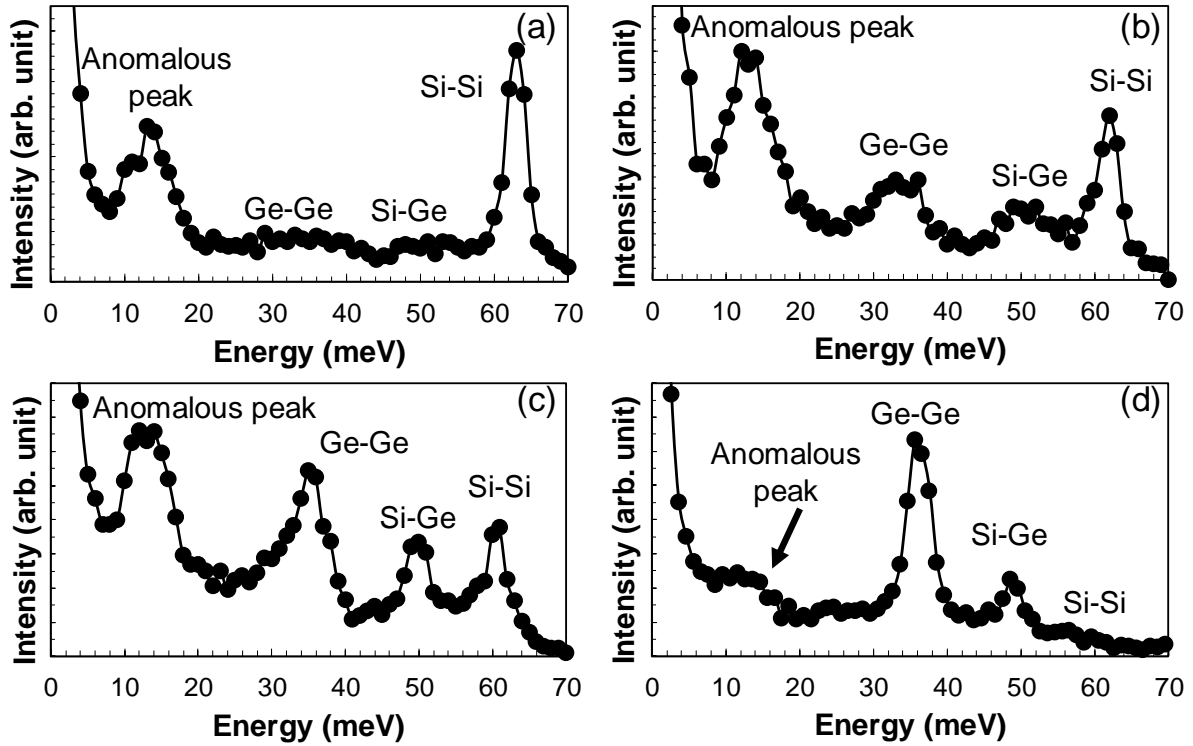
The molecular dynamics (MD) simulations were also performed to reproduce the phonon properties of bulk SiGe using the MD LAMMPS [12] simulation code. The initial lattice constant  $a_i$  of  $\text{Si}_{1-x}\text{Ge}_x$  was defined as  $a_i = 5.658 - 0.227x$ . The cell size of a bulk  $\text{Si}_{1-x}\text{Ge}_x$  was set to cuboidal structures consisting of 3,840 atoms with a width of  $4a_i \times 4a_i \text{ \AA}$  and a length of  $30a_i \text{ \AA}$ . The following Stillinger-Weber (SW) potential function [13] was applied. The average strain state in the model crystal of SiGe for MD simulations was set to 0. The atomic arrangements in the  $\text{Si}_{1-x}\text{Ge}_x$  alloy model were shuffled using random numbers.

**Table 1.** Specifications of bulk  $\text{Si}_{1-x}\text{Ge}_x$  samples.

Ge fraction $x$	Crystal orientation	Sample fabrication method
0.16	(001)	Cz
0.32	(001)	TLZ
0.45	(001)	TLZ
0.72	(111)	Cz

## Results and discussion

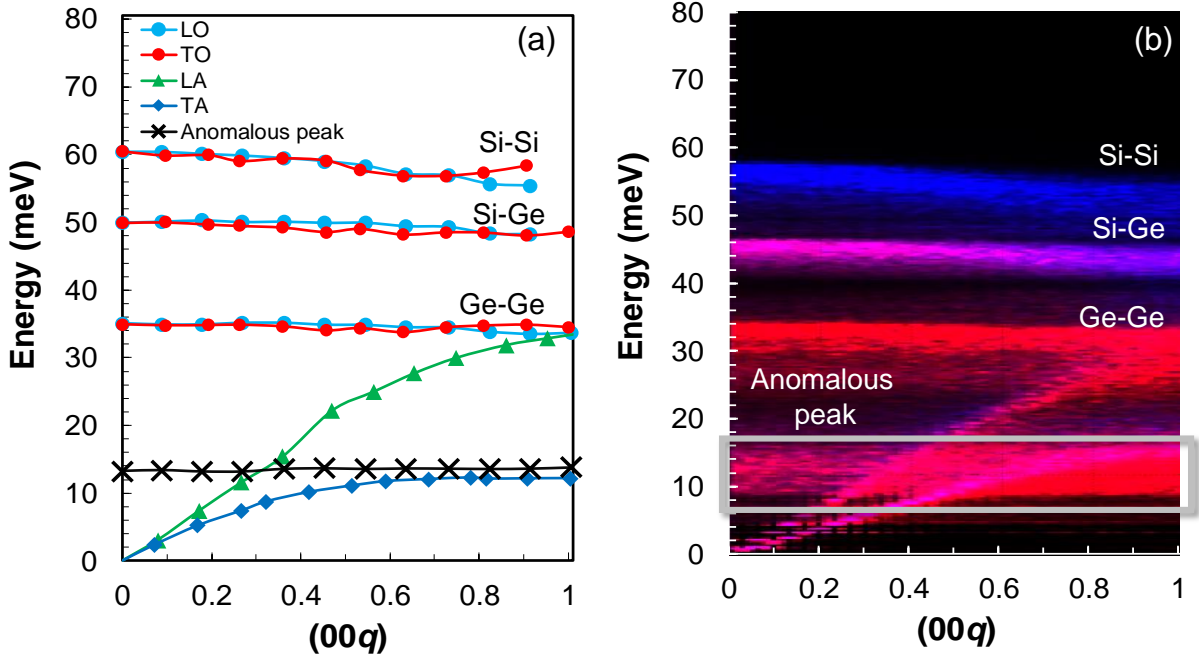
Figure 1 shows the IXS spectra (optical modes) at  $\Gamma$  point for bulk SiGe with Si (9 9 9) reflection (BL35XU). In all samples, three optical phonon modes (Ge-Ge, Si-Ge, and Si-Si modes) were observed, similar to the RS measurements. As seen in the profiles of the RS measurements, asymmetrical broadenings on the low-energy side of the first-order optical phonon of the Ge-Ge, Si-Ge, and Si-Si modes were also observed. In the Raman scattering, these broadenings are often explained using the so-called spatial correlation model, which reproduces the relaxation of momentum conservation due to random atom positions [14], and a similar mechanism is supposed to dominate the asymmetrical profiles in IXS. Moreover, anomalous peaks appear on the low-energy side (around 13 meV) in addition to the optical modes above [15]. These peaks have not been detected either for the pure Si and Ge phonon spectra in the INS and RS study. Therefore, these peaks are expected to show a unique vibrational mode in the SiGe alloy.



**Fig. 1.** IXS spectra at  $\Gamma$  point for bulk  $\text{Si}_{1-x}\text{Ge}_x$  with  $x$  of (a) 0.16, (b) 0.32, (c) 0.45, and (d) 0.72 with Si (9 9 9) reflection (BL35XU) [15].

As an example of phonon dispersion of bulk  $\text{Si}_{1-x}\text{Ge}_x$ , Fig. 2(a) shows the phonon dispersion curves of bulk  $\text{Si}_{1-x}\text{Ge}_x$  with  $x$  of 0.45 along  $\Gamma$ -X obtained by peak fitting the IXS spectra with (symmetrical) Voigt function, so the asymmetric features described above are not considered. The SiGe alloy has a diamond structure over the whole Ge fraction range ( $0 \leq x \leq 1$ ). Therefore, the phonon dispersion relations are expected to consist of four phonons along  $\Gamma$ -X (similar to pure Si and Ge): longitudinal optical (LO), transverse optical (TO), longitudinal acoustic (LA), and transverse acoustic (TA) phonon modes. As shown in Fig. 2(a), the acoustic modes reflect this scenario, and single LA and TA modes are observed. In contrast to the acoustic modes, the LO and TO modes are split into three modes (Ge-Ge, Si-Ge, and Si-Si modes). The TO and LO modes are degenerated at the  $\Gamma$  point, and the obtained phonon dispersions agree well with the results at the  $\Gamma$  point (see Fig. 1) and RS measurements. Figure 2(b) shows the phonon dispersion curves obtained by the MD simulation for  $x = 0.45$ . The intensities of blue, magenta, and red colors indicate the density of states (DOS) of the Si-Si, Si-Ge, and Ge-Ge vibration modes, respectively, in Fig. 2(b). The results of the optical and acoustic phonon modes in the simulation are in good agreement with the experimental results.

In addition, the anomalous mode has no momentum dependence along  $\Gamma$ -X as shown in Fig. 2 and no Ge fraction dependence was also confirmed (not shown), suggesting that this mode is something localized and there is no propagation derived from alloy structure. This supports the idea that the obtained phonon mode is a low-energy LVM that occurs when, for example, Ge-Ge pairs or Ge atom clusters are surrounded by Si atoms. The effect of Ge cluster size [16] and atomic mass [17] were observed by MD simulation and the idea is almost consistent with the local mode of the Ge cluster.



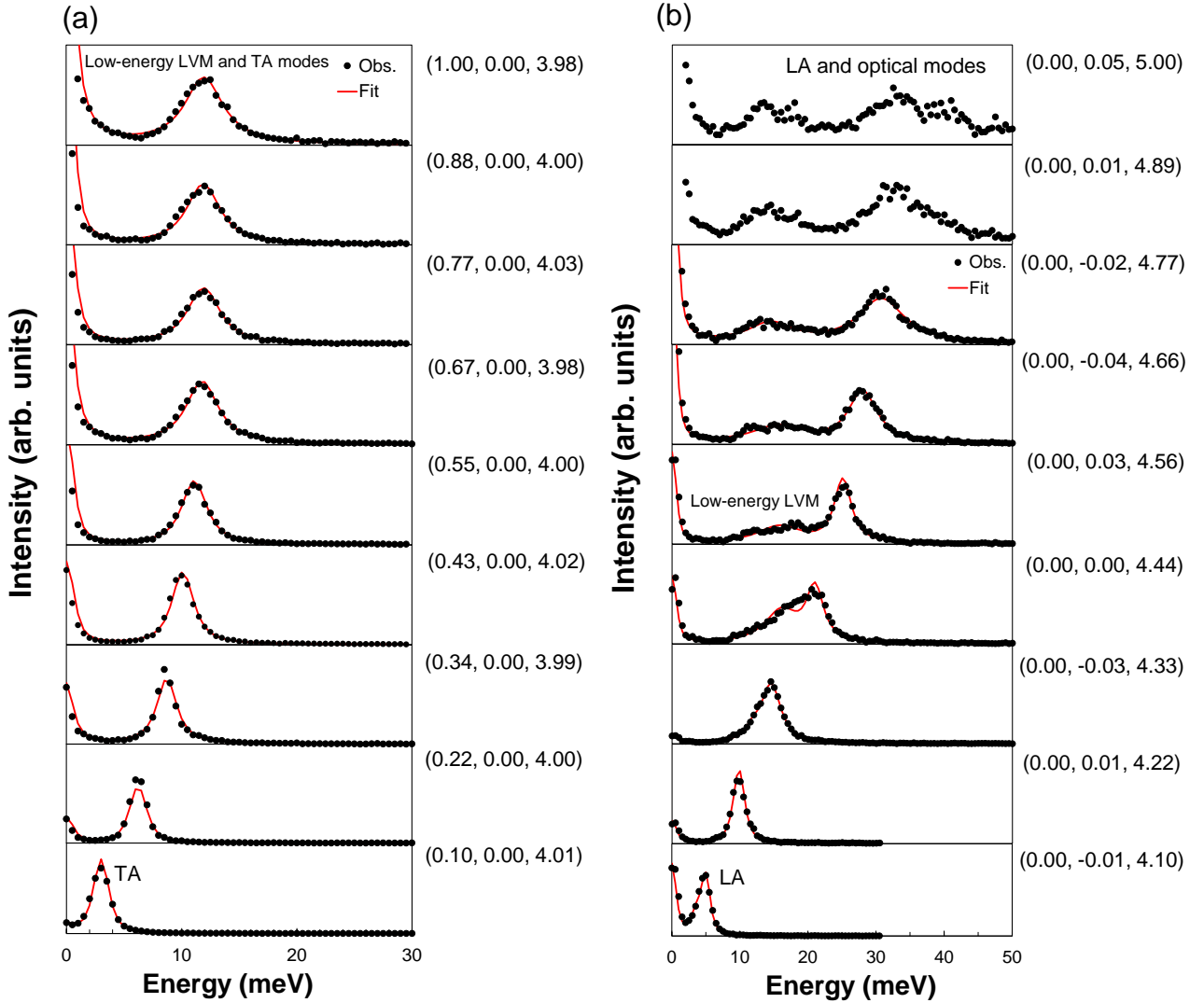
**Fig. 2.** Phonon dispersion relations of bulk  $\text{Si}_{1-x}\text{Ge}_x$  with  $x$  of 0.45 along  $\Gamma$ -X with Si (9 9 9) reflection (BL35XU) [15]. (a) Phonon dispersion curves including the anomalous peaks obtained by peak positions of IXS spectra. Note that there are three types of first-order optical modes (Ge-Ge, Si-Ge, and Si-Si modes). (b) Corresponding phonon dispersion curves simulated by the MD calculations. The blue, magenta, and red colors indicate the Si-Si, Si-Ge, and Ge-Ge vibration modes, respectively. The phonon dispersion of the anomalous peak is marked with a gray rectangle.

Figure 3(a) and (b) shows the IXS spectral linewidth of the TA and LA modes of bulk  $\text{Si}_{1-x}\text{Ge}_x$  with  $x$  of 0.45. The IXS spectral linewidth of both modes became dramatically broader around the X point. This broadening was commonly observed in the other bulk  $\text{Si}_{1-x}\text{Ge}_x$  samples. In addition, relative symmetrical broadenings of the acoustic phonon modes along  $\Gamma$ -X were confirmed, in contrast to the first-order optical phonon of the Ge-Ge, Si-Ge, and Si-Si vibration modes with asymmetrical broadenings on the low-energy side at  $\Gamma$  point. From the above, the acoustic modes along  $\Gamma$ -X for the SiGe alloy do not relax the momentum conservation [14] (in other words, asymmetrical broadenings) any differently from the first-order optical phonon modes even if the atomic positions are random.

As momentum ( $q$ ) changes from 0 to 1 (from  $\Gamma$  to X points), the TA phonon energy is close to that of the low-energy LVM (anomalous mode) at  $0.5 \leq q \leq 1$  (see Fig. 3(a)), presumably due to phonon mixing (overlapping) between the TA mode and anomalous mode. On the other hand, as the LA mode has a different energy position from the anomalous peak on the low energy side at  $0.5 \leq q \leq 1$  as shown in Fig. 3(b), I consider that broadening of the LA mode itself has occurred (note that it is difficult to determine the line-width near the X point since the LA and optical modes such as Ge-Ge vibration mode are completely mixed).

Although I also found that the TA phonon spectral linewidth has Ge fraction dependence (not shown), further investigation and analysis are required to extract the TA phonon spectral line-width because the TA phonon energy is overlapping to that of the LVM at a low energy position around the X point. In contrast, the LA phonon spectral linewidth having no Ge fraction dependence (not shown) indicates that there is no change of the LA phonon

lifetime.



**Fig. 3.** Momentum ( $q$ ) dependence of IXS spectra of acoustic modes (TA and LA modes) for  $\text{Si}_{1-x}\text{Ge}_x$  ( $x = 0.45$ ) with Si (11 11 11) reflection (BL35XU). (a)  $Q \sim (q, 0, 4)$  (TA mode mainly appears) and (b)  $Q \sim (0, 0, 4 + q)$  (LA mode mainly appears) [18].

### Conclusions

In this study, the phonon properties of bulk SiGe alloys are investigated for acoustic modes to explore the origin of the low thermal conductivity by IXS with synchrotron radiation. The anomalous phonon mode on the low-energy side in bulk SiGe has been observed through measurement of phonon dispersion curves for bulk SiGe. The anomalous mode had no momentum and Ge fraction dependence and this behavior was consistent with the MD calculations, indicating that the mode originated from the Ge localized vibration (low-energy LVM) without propagation property. Moreover, both TA and LA phonon spectra were broadened as momentum increased (from  $\Gamma$  to X points). The acoustic phonon spectral-width broadening may contribute to the suppression of the thermal conductivity by interfering with the low-energy LVM.

## Acknowledgements

The part of this work was supported by the CREST Project No. JPMJCR19Q5 of the Japan Science and Technology Corporation (JST). The IXS measurements were performed at SPring-8 with the approval of JASRI (Proposal Nos. 2016A1496, 2017B1630, 2019A1678, 2019B1750, 2020A0662, 2020A1463, 2021A1363, and 2022A1470). I thank Dr. Hiroshi Uchiyama (JASRI), Dr. Daisuke Ishikawa (JASRI), Dr. Alfred Q. R. Baron (RIKEN/JASRI), Dr. Satoshi Tsutsui (JASRI), Dr. Hiroshi Fukui (JASRI), and Dr. Ichiro Hirosawa (SAGA-LS) for their support with IXS measurements. I also thank Prof. Ichiro Yonenaga (Tohoku University) and Dr. Yasutomo Arai (JAXA) for preparation of bulk SiGe samples. Analyzing the IXS results were supported by Prof. Takanobu Watanabe (Waseda University), Prof. Motohiro Tomita (Seikei University), Dr. Sylvia Yuk Yee Chung, Dr. Takuto Kojima (Nagoya University), Dr. Koji Usuda (KIOXIA Corp.), Mr. Haruki Takeuchi, and Mr. Yutaka Hara throughout the work.

## REFERENCES

- [1] J. P. Dismukes, L. Ekstrom, E. F. Steigmeier, I. Kudman, and D. S. Beers, *J. Appl. Phys.* **35**, 2899 (1964).
- [2] K. Ismail, J. O. Chu, and B. S. Meyerson, *Appl. Phys. Lett.* **64**, 3124 (1994).
- [3] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, *IEEE Trans. Electron Devices* **41**, 2357 (1994).
- [4] J. Garg, N. Bonini, B. Kozinsky, and N. Marzari, *Phys. Rev. Lett.* **106**, 045901 (2011).
- [5] T. Hori, T. Shiga, and J. Shiomi, *J. Appl. Phys.* **113**, 203514 (2013).
- [6] O. Pagès, J. Souhabi, V. J. B. Torres, A. V. Postnikov, and K. C. Rustagi, *Phys. Rev. B* **86**, 045201 (2012).
- [7] F. Pezzoli, L. Martinelli, E. Grilli, M. Guzzi, S. Sanguinetti, M. Bollani, H. D. Christina, G. Isella, H. von Känel, E. Wintersberger, J. Stangl, and G. Bauer, *Mater. Sci. Eng. B* 124-125, **127** (2005).
- [8] I. Yonenaga, *J. Cryst. Growth* **275**, 91 (2005).
- [9] K. Kinoshita, Y. Arai, O. Nakatsuka, K. Taguchi, H. Tomioka, R. Tanaka, and S. Yoda, *Jpn. J. Appl. Phys.* **54**, 04DH03 (2015).
- [10] A. Q. R. Baron, Y. Tanaka, S. Goto, K. Takeshita, T. Matsushita, and T. Ishikawa, *J. Phys. Chem. Solids* **61**, 461 (2000).
- [11] A. Q. R. Baron, *SPring-8 Information Newsletter* **15**, 14 (2010).
- [12] S. Plimptom, *J. Comput. Phys.* **117**, 1 (1995).
- [13] F. Stillinger and T. Weber, *Phys. Rev. B* **31**, 5262 (1985).
- [14] P. Parayanthal and F. H. Pollak, *Phys. Rev. Lett.* **52**, 1822 (1984).
- [15] R. Yokogawa, H. Takeuchi, Y. Arai, I. Yonenaga, M. Tomita, H. Uchiyama, T. Watanabe and A. Ogura, *Appl. Phys. Lett.* **116**, 242104 (2020).
- [16] S. Y. Y. Chung, M. Tomita, J. Takizawa, R. Yokogawa, A. Ogura, H. Wang, and T. Watanabe, *AIP Advances*, **11**, 075017 (2021).
- [17] S. Y. Y. Chung, M. Tomita, R. Yokogawa, A. Ogura, and T. Watanabe, *AIP Advances*, **11**, 115225 (2021).
- [18] R. Yokogawa, Y. Arai, I. Yonenaga, M. Tomita, S. Y. Y. Chung, H. Uchiyama, T. Watanabe, and A. Ogura, *Appl. Phys. Lett.* **121**, 082105 (2022).

**November 8 (Tuesday)**

# **Session C**

Chair: *S. Nishizawa (Kyushu Univ.)*

**11:00 ~ 12:00**  
(Reception Hall)



**November 8 (Tuesday)**

# **Session D**

Chair: *K. Kakimoto (Tohoku Univ.)*

**14:00 ~ 15:00**  
(Reception Hall)

## **Precipitation of suboxides in silicon and its impact on gettering and carrier recombination**

G. Kissinger<sup>1\*</sup>, D. Kot<sup>1</sup>, T. Müller<sup>2</sup>, and A. Sattler<sup>2</sup>

<sup>1</sup>*IHP – Leibniz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*

<sup>2</sup>*Siltronic AG, Einsteinstraße 172 Tower B / Blue Tower, 81677 Munich, Germany*

e-mail: gkissinger@ihp-microelectronics.com

### **Abstract**

The phase composition of oxide precipitates and the corresponding emission of self-interstitials at the minimum of the free energy and their evolution with increasing number of oxygen atoms in the precipitates are investigated theoretically. The results can explain the compositional evolution of oxide precipitates and the role of self-interstitials therein. The formation of suboxides around the edges of SiO<sub>2</sub> precipitates after reaching a critical size can explain phenomena like gettering of Cu by segregation to the suboxide region and lifetime reduction by recombination of minority carriers in the suboxide. It provides an alternative explanation, based on minimized free energy, to the theory of strained and unstrained plates. A second emphasis was paid to the evolution of the morphology of oxide precipitates. Based on the comparison with results from scanning transmission electron microscopy the sequence of morphology evolution of oxide precipitates was deduced. It turned out that it is opposite to the sequence assumed until now.

### **Introduction**

Investigations of the precipitation of interstitial oxygen in Czochralski (CZ) silicon have been carried out since decades. The issue is very complex involving other species like intrinsic point defects, dopants and impurities. In addition to this, the initial stages of oxygen precipitation take place on the atomic level and cannot be observed directly until now. However, advances in diagnostic methods always provide new insights into the precipitation process. Nevertheless, there are still open issues which need to be clarified. Such issues are the getter efficiency of oxide precipitates for metallic impurities and the recombination activity of oxide precipitates in relation to their composition. First, recent hypotheses and findings are summarized here.

Starting from TEM investigations of the size of oxide precipitates and comparing it with their density determined by preferential etching and the loss of interstitial oxygen (O<sub>i</sub>) measured by FTIR, Falster et al. found a discrepancy between the total loss of O<sub>i</sub> and the visible loss of O<sub>i</sub> in the form of precipitates observed by transmission electron microscopy (TEM) [1]. They developed a theory which distinguishes between strained oxide precipitates, which are able to getter metallic impurities, and unstrained oxide precipitates so-called “ninja” precipitates, being not able to getter metallic impurities [1]. There are several arguments speaking against this theory [2]. Until now, several phenomena are explained by the conversion from so-called unstrained to strained oxide precipitates, as e.g. during recombination of minority carriers [3-6].

The stoichiometry of oxide precipitates was investigated using electron energy loss spectrometry (EELS) carried out by scanning transmission electron microscopy (STEM) [7]. It was shown that the center of oxide precipitates consists of oxygen-rich SiO<sub>x</sub> being in most cases SiO<sub>2</sub> surrounded by suboxide with decreasing x towards the edges. These suboxides surrounding oxide precipitates act as gettering sinks for Cu impurities [8]. Murphy et al. reported

that iron impurities segregate to oxide precipitates and thus form additional recombination centers in addition to dangling bonds [9, 10]. It is of interest if in any case oxide precipitates are surrounded by suboxide because it could become a criterion for efficient gettering.

Here, we describe a theoretical investigation of the phase composition of oxide precipitates and the corresponding emission of self-interstitials at the minimum of the free energy and their evolution with increasing number of oxygen atoms in the precipitates. The comparison with experimental results from ourselves and from the literature allowed us to understand the important role of suboxides for internal gettering of metallic impurities and for carrier recombination at oxide precipitates being important for lifetime control.

## Modelling and Experimental

The models for minimizing the free energy  $G$  are extensively described in Ref. [2]. Two cases were modeled spherical and spheroidal precipitates whereby the former represent the octahedral precipitates and the latter represent plate-like precipitates both being the main types of oxide precipitates found experimentally in silicon. The models are valid for a closed system which basically represents the situation in the bulk of a silicon wafer. The free energy in the spheroidal model is a three-dimensional function which can determine for each number of precipitated oxygen atoms  $n$  the minimum of  $G$  with respect to the corresponding aspect ratio  $\gamma$ , the stoichiometry  $x$ , and the interstitials to be emitted per precipitated oxygen atom  $\beta$ . The minimization was achieved by solving:

$$\frac{\partial G(n,x,\beta,\gamma)}{\partial \gamma} = 0, \quad \frac{\partial G(n,x,\beta,\gamma)}{\partial x} = 0 \quad \text{and} \quad \frac{\partial G(n,x,\beta,\gamma)}{\partial \beta} = 0$$

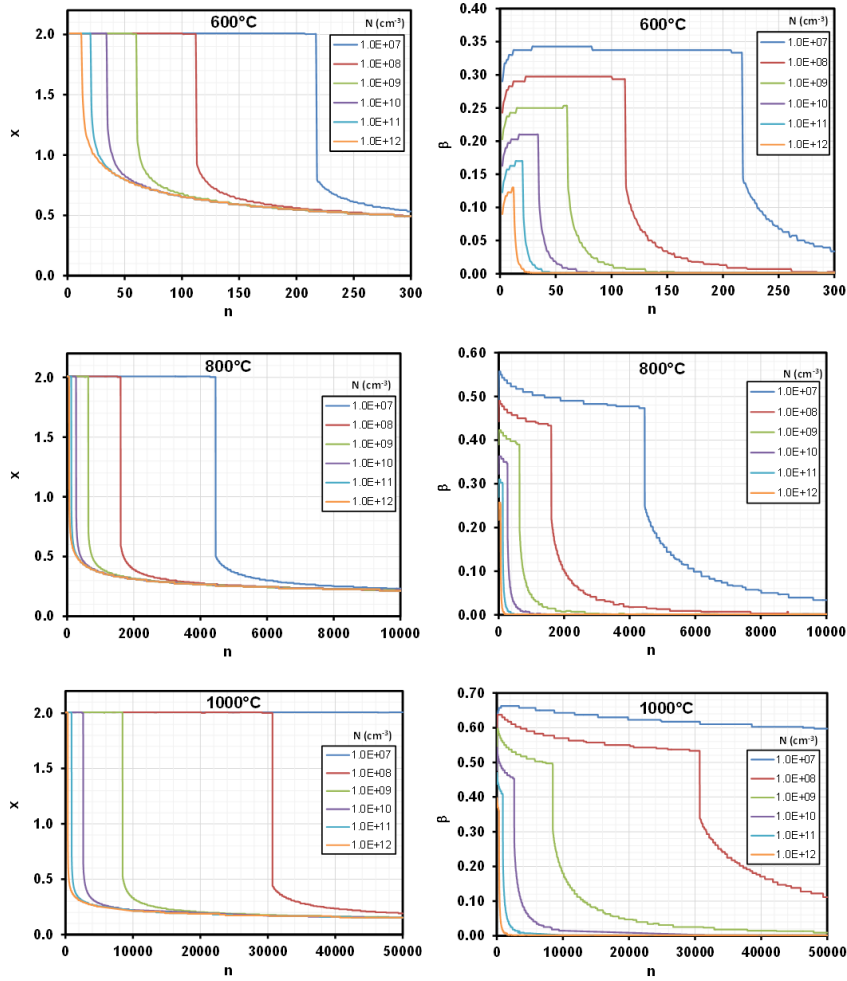
under the constraints  $0 < \gamma < 1$ ,  $0 \leq x \leq 2$ , and  $0 \leq \beta \leq 0.7$ . The range of  $\beta$  covers all possibilities from zero to full strain relief by self-interstitial emission. For the spherical model,  $G$  is just a two-dimensional function because  $\gamma = 1 = \text{const}$ .

Experimental data were generated for comparison with the results of modeling. The details about getter test experiments and scanning transmission electron microscopy (STEM) investigations of the precipitate morphology can be found in Ref. [2].

## Results

Results of the spherical model are shown in Fig. 1. It can be seen that for low numbers of precipitating oxygen atoms the composition is  $\text{SiO}_2$  and the self-interstitial emission relieving the strain is very high. With increasing  $n$ , the emission of self-interstitials slightly decreases up to a critical number of precipitated oxygen atoms  $n_{crit}$ . Then, the minimum free energy suddenly jumps to low values of  $x$ , changing the stoichiometry into a suboxide, accompanied by very low emission of self-interstitials. The critical number of precipitated oxygen atoms decreases with increasing density of oxide precipitates and it increases with increasing temperature.

Results of the spheroidal model can be found in Fig. 2. As in the model for spherical precipitates for low numbers of precipitating oxygen atoms the composition is  $\text{SiO}_2$  and the self-interstitial emission relieving the strain is very high. For low numbers of precipitating oxygen atoms, the morphology is

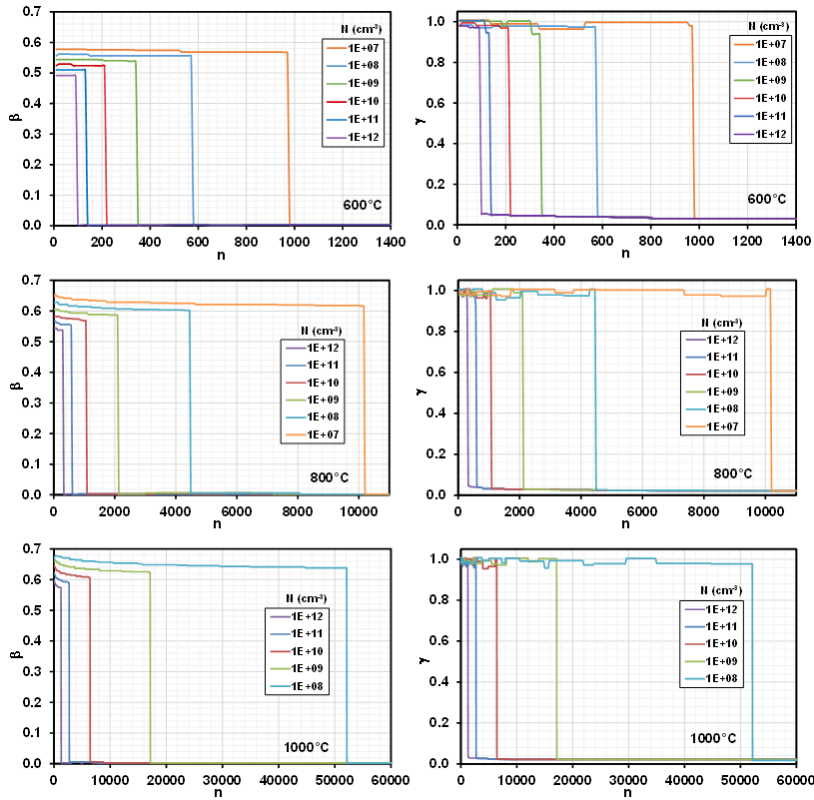


**Fig. 1.** Stoichiometry of oxide precipitates  $x$  (left) and self-interstitials emitted per precipitated oxygen atom  $\beta$  (right) both plotted as function of the number of oxygen atoms in the precipitate  $n$  shown for different densities of oxide precipitates  $N$  and different temperature. Modelling for  $C_{O_i}^0 = 6 \times 10^{17} \text{ cm}^{-3}$  [2]. Copyright 2020 with permission from the authors.

samples of silicon wafers annealed at 1000 °C for times up to 30 h by STEM with a density of oxide precipitates of about  $1 \times 10^{10} \text{ cm}^{-3}$ . Octahedral oxide precipitates could be observed only below the surface of the silicon wafers up to a depth of 100 $\mu\text{m}$  or less depending on the annealing time. With further increasing depth we first detected transition forms between octahedral and platelets and then only platelets. With increasing annealing time the depth up to which octahedral precipitates were observed decreased. This is well in agreement with the results of modeling oblate spheroidal oxide precipitates. Below the surface, part of the emitted self-interstitials can diffuse out and the increased  $n_{\text{crit}}$  makes the octahedral morphology more stable for higher  $n$ . When the octahedral morphology becomes unstable, what happens first in the bulk, the precipitates start changing their morphology as demonstrated in Fig. 3. Figure 3a shows an octahedral precipitate below the surface before the morphological transition starts. It can be seen in Fig. 3b that growth in [111] direction is retarded and growth in [110] directions around the edges of the octahedron is enhanced. In Fig. 3c, the transformation progressed and a platelet evolving from the octahedron becomes visible. Figure 3d shows a large platelet with the original octahedron and in Fig. 3e only the platelet is

also spherical. However, when  $n_{\text{crit}}$  is reached the precipitate changes its shape from sphere to platelet and stops the emission of self-interstitials maintaining the composition of SiO<sub>2</sub>. The optimum aspect ratio of the platelets lies between 0.02 and 0.03. Such values were also found experimentally by Sueoka et al. [12].

The modeling results refer to homogeneous oxide precipitates under quasi-equilibrium conditions. In reality, the kinetics of morphology change is much more slowly than a change of stoichiometry, which just happens during the attachment of new atoms. Therefore, when the octahedral morphology gets unstable suboxides can be expected to form as well. We investigated the evolution of the morphology of oxide precipitates experimentally using



**Fig. 2.** Self-interstitials emitted per precipitated oxygen atom  $\beta$  (left) and aspect ratio  $\gamma$  (right) both plotted as function of the number of oxygen atoms in the precipitate  $n$  shown for different densities of oxide precipitates  $N$  and different temperature. Modelling  $C_{O_i}^0 = 6.5 \times 10^{17} \text{ cm}^{-3}$  [2]. Copyright 2020 with permission from the authors.

existing finally. Via surface reconstruction the atoms of the original octahedron distribute on the (100) surface of the platelet. The evolution of the morphology of growing oxide precipitates is well in agreement with results of modeling. However, it is exactly the opposite to the evolution model of Bergholz et al. [13].

A possible criterion for efficient gettering of Cu should be based on the spherical model because changes of morphology are very slow and suboxides can be expected to be formed. Three different states of oxide precipitates being relevant for gettering can be distinguished. If their size is subcritical they are unable to getter impurities. They consist of  $\text{SiO}_2$  at this stage. When the number of precipitated oxygen atoms exceeds the critical number for suboxide formation gettering

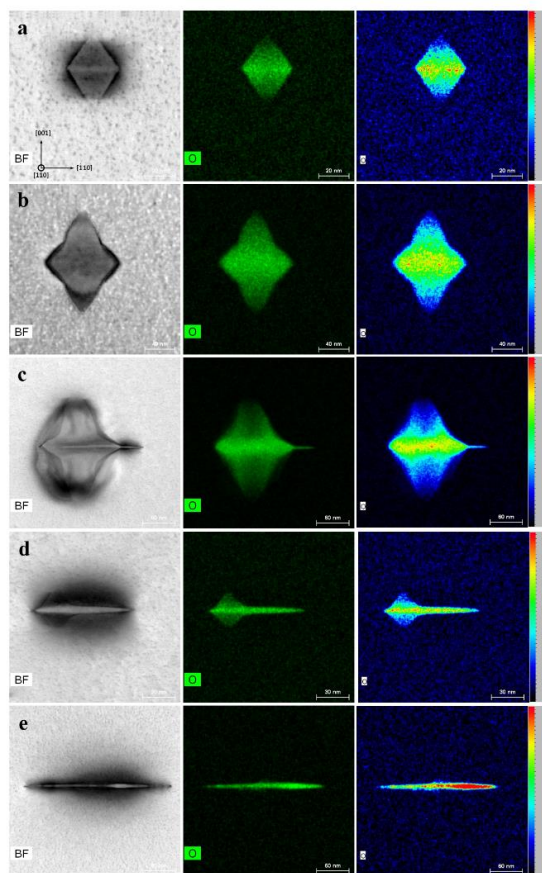
becomes possible but the efficiency is not high enough to getter all of the Cu atoms. If the number of oxygen atoms in the suboxide exceeds a further critical value the precipitates can efficiently getter the copper impurities. Based on the results of modeling, the time to reach efficient gettering strongly depends on the density of oxide precipitates. This is well in agreement with Ref. 1 but based on an alternative explanation for the effects described there.

In Fig. 4, experimental and modeled getter efficiencies for Cu are compared. The results are in good agreement. Further comparisons of experimental and modelling results for gettering and also for lifetime reduction by recombination of minority carriers in the suboxide can be found in Ref. [2]. In all these cases, a good agreement between modeling and experimental results was found.

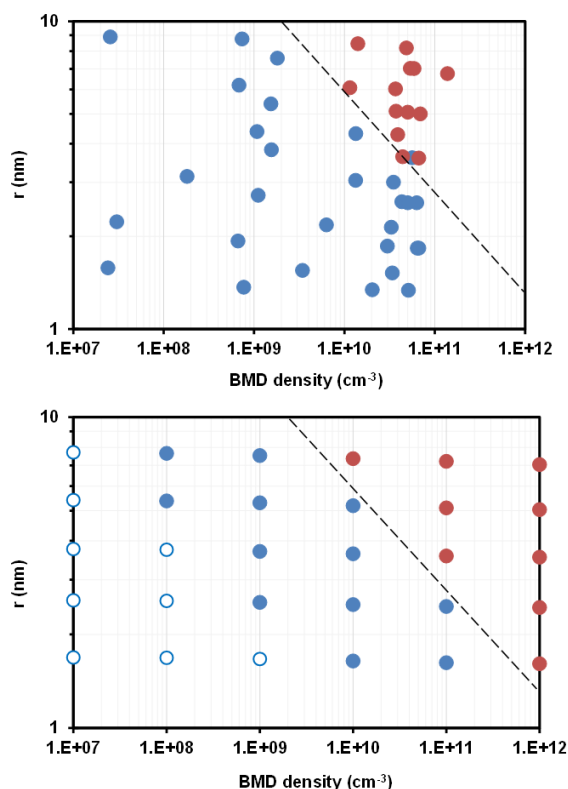
## Conclusions

The aim of this work was to find out the optimum path of growing oxide precipitates with respect to their stoichiometry, emission of self-interstitials and morphology. Applying the model for spherical oxide precipitates, it was found that for low numbers of precipitating oxygen atoms the composition is  $\text{SiO}_2$  and the self-interstitial emission relieving the strain is very high. With increasing  $n$ , the emission of self-interstitials slightly decreases up to a critical number of precipitated oxygen atoms

$n_{crit}$ . Then, the minimum free energy suddenly jumps to low values of  $x$ , changing the stoichiometry into a suboxide, accompanied by very low emission of self-interstitials. The critical number of precipitated oxygen atoms decreases with increasing density of oxide precipitates and it increases with increasing temperature. This means that the availability of suboxides for getting of Cu impurities depends on both the annealing temperature and the density of oxide precipitates. For very high densities of oxide precipitates the time to achieve efficient getting of oxide precipitates is extremely short. It increases markedly with decreasing density of oxide precipitates. Applying the model for oblate spheroidal precipitates similarly to the model for spherical precipitates for low numbers of precipitating oxygen atoms the composition is  $\text{SiO}_2$  and the self-interstitial emission relieving the strain is very high. For low numbers of precipitating oxygen atoms, the



**Fig. 3.** TEM images of oxide precipitates annealed at 1000 °C reflecting the evolution of precipitate morphology from top to bottom. Left: STEM bright field images (dark contrasts are caused by strain fields), middle: EDX maps of oxygen, and right: mapping of oxygen counts in arbitrary units increasing from blue to red [2]. Copyright 2020 with permission from the authors.



**Fig. 4.** Getter efficiency of samples annealed for different times at 800 °C plotted as function of radius and density of oxide precipitates, above: experimental values from Cu getter tests, below: theoretical values. Full red circles represent high getter efficiencies  $\geq 90\%$ , full blue circles represent inefficient getting, and empty blue circles represent precipitates theoretically being unable to getter at all [2]. Copyright 2020 with permission from the authors.

morphology is also spherical. However, when  $n_{crit}$  is reached the precipitate changes its shape from sphere to platelet and stops the emission of self-interstitials maintaining a composition of SiO<sub>2</sub>. The optimum aspect ratio of the platelets lies between 0.02 and 0.03.

The modeling results refer to homogeneous oxide precipitates under quasi-equilibrium conditions. In reality, the kinetics of morphology change is much more slowly than a change of stoichiometry, which just happens during the attachment of new atoms. Therefore, when the octahedral morphology gets unstable suboxides can be expected to form as well. The stages of morphology change start at octahedral morphology. Then the growth into  $\langle 110 \rangle$  directions starting at the edges of the octahedron is enhanced until a platelet evolves from the octahedron and the original octahedron remains as fins on the platelet before it vanishes completely. The rate of morphology change depends on the possibility of out-diffusion of the generated self-interstitials and thus on the depth from the wafer surface.

The formation of suboxides at the edges of oxide precipitates after reaching a critical size is reached can explain several phenomena like gettering of Cu by segregation to the suboxide region and lifetime reduction by recombination of minority carriers in the suboxide. It thus provides an alternative explanation, based on minimized free energy, to the theory of strained and unstrained plates.

## REFERENCES

- [1] R. Falster, V. V. Voronkov, V. Y. Resnik, and M. G. Milvidskii, Proc. Electrochem. Soc., High Purity Silicon VIII (2004), Electrochem. Soc., Pennington, NJ, USA, Vol. **2004-05**, p.188.
- [2] G. Kissinger, D. Kot, A. Huber, R. Kretschmer, T. Müller, and A. Sattler, ECS J. Solid State Sci. Technol. **9**, 064002 (2020).
- [3] K. Bothe, R. J. Falster and J. D. Murphy, Appl. Phys. Lett. **101**, 032107 (2012).
- [4] J. D. Murphy, K. Bothe, M. Olmo, V. V. Voronkov, and R. J. Falster, J. Appl. Phys. **110**, 053713 (2011).
- [5] G. Kissinger, J. Vanhellefont, E. Simoen, C. Claeys, and H. Richter, Mat. Sci. Eng. B **36**, 225 (1996).
- [6] J. D. Murphy, M. Al-Amin, K. Bothe, M. Olmo, V. V. Voronkov, and J. R. Falster, J. Appl. Phys. **118**, 215706 (2015).
- [7] G. Kissinger, M. A. Schubert, D. Kot, and T. Grabolla, ECS J. Solid State Sci. Technol. **6**, N54 (2017).
- [8] G. Kissinger, D. Kot, M. Klingsporn, M. A. Schubert, A. Sattler, and T. Müller, ECS J. Solid State Sci. Technol. **4**, N124 (2015).
- [9] J. D. Murphy, K. Bothe, V. V. Voronkov, and R. Falster, Appl. Phys. Lett. **102**, 042105 (2013).
- [10] V. Lang, J. D. Murphy, R. J. Falster, and J. J. L. Morton, J. Appl. Phys. **111**, 013710 (2012).
- [11] Secco d'Aragona, J. Electrochem. Soc. **199**, 948 (1972).
- [12] K. Sueoka, M. Akatsuka, M. Yonemura, T. Ono, E. Asayama, and H. Katahama, J. Electrochem. Soc. **147**, 756 (2000).
- [13] W. Bergholz, M. J. Binns, G. R. Booker, J. C. Hutchison, S. H. Kinder, S. Messoloras, R. C. Newman, R. J. Stewart, and J. G. Wilkes, Phil. Mag. B, **59**, 499 (1989).

## Formation Behavior of Oxygen Precipitates in Silicon Wafers Subjected to Ultra-High-Temperature Rapid Thermal Process

Haruo Sudo<sup>1\*</sup>, Kozo Nakamura<sup>2</sup>, Hideyuki Okamura<sup>1</sup>, Susumu Maeda<sup>1</sup>, and Koji Sueoka<sup>3</sup>

<sup>1</sup>Base Technology Group, Technology Department, GlobalWafers Japan Co., Ltd., 6-861-5, Seiro-machi Higashiko, Kitakanbara-gun, Niigata, 957-0197 Japan,

<sup>2</sup>Center for Regional Innovation and Strategy, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan,

<sup>3</sup>Faculty of Computer Science and System Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

Haruo\_Sudo@sas-globalwafers.co.jp

### Abstract

In this study, the formation behavior of oxygen precipitates in Si wafers during a two-step heat treatment was investigated using both experiments and simulations. Si wafers were subjected to a rapid thermal process (RTP) at 1350 °C in an oxygen atmosphere. The first-step temperature was varied from 750 to 950 °C, and the duration of this step was 0.5–16 h. Meanwhile, in the second step, the temperature was maintained at 1000 °C for 16 h. The results suggested that the highest oxygen precipitate density was achieved when the first-step temperature was set at 850 °C. Considering the results obtained using the constructed simulation model, we concluded that the resulting oxygen precipitate density was determined by the nucleation rate, growth size, and timing of the terminal point of the nucleation.

### 1. Introduction

The oxygen precipitates in Si wafers serve as excellent gettering sites for metal impurities. The gettering technology for Si wafers is necessary for maintaining high purity in the active layers while manufacturing image sensors and logic devices. Falster *et al.* first reported that a rapid thermal process (RTP) in the temperature range of 1100–1250 °C with rapid cooling in a non-oxidation atmosphere produced excess vacancies (*Vs*) in Czochralski (CZ)–Si wafers [1]. During the cooling process, *V* concentration in the sub-surface layer decreased due to out-diffusion. However, in the bulk region, where the influence of out-diffusion is weak, more *Vs* than interstitial Si atoms (*Is*) remain after pair annihilation [1-3]. This may be attributed to the higher thermal equilibrium concentration of *Vs* than that of *Is*. Thereby, high-density oxygen precipitates are formed only in the bulk region. Pagani *et al.* reported that a nitrogen atmosphere effectively enhanced oxygen precipitation during RTP, compared to that in an argon atmosphere, because the nitriding wafer surface induces excess *Vs* [4]. In contrast, Akatsuka *et al.* reported the suppressed oxygen precipitation in an oxygen atmosphere. They explained that *Vs* do not remain in the wafers with the dominance of *Is* through oxidation [2].

Our previous study was focused on the effects of ultra-high temperatures ( $\geq 1300$  °C) on CZ–Si wafers [5-10]. At RTP temperatures higher than 1300 °C, we simultaneously achieved effective annihilation of void defects in *V*-rich type CZ–Si wafers and controlled the generation of excess *Vs* even in an oxygen atmosphere. In particular, the oxygen precipitates in these RTP wafers were formed in the bulk region after heat treatments. Maeda *et al.* qualitatively explained that void defects are effectively annihilated, and vacancies remain simultaneously at RTP temperatures  $> 1300$  °C in oxygen atmosphere, based on the concentration balance of point defects, as shown in



Fig. 1 [8]. The solid lines represent the thermal equilibrium concentration of  $V$  ( $C_V^{eq}$ ) and  $I$  ( $C_I^{eq}$ ).  $C_V^{eq}$  is greater than  $C_I^{eq}$  at any temperature. The dotted lines represent the estimated concentration of  $V$  ( $C_V$ ) and  $I$  ( $C_I$ ) in oxygen atmosphere at the end point of the maximum temperature. At temperatures  $< 1300$  °C,  $C_I$  is more significant than  $C_V$ . Thereby, no oxygen precipitates are formed during heat treatments after RTP. However,  $C_I$  decreases and  $C_V$  increases with increasing RTP temperature.  $C_I$  and  $C_V$  become comparable around 1300 °C. Furthermore, above 1300 °C, although  $I_s$  are supersaturated ( $C_I > C_I^{eq}$ ),  $C_V$  is greater than  $C_I$ . In this case, void defects are effectively annihilated, and oxygen precipitates are formed due to residual  $V_s$  during heat treatments after RTP. Therefore, the ultra-high temperature RTP technology produces  $V$ -rich-type CZ–Si wafers with a well-designed structure comprising denuded and intrinsic gettering zones, which can impact semiconductor manufacturing.

Further, we clarified that the oxygen precipitate density quantitatively depends on the residual  $V$  concentration in wafers owing to RTP [9]. However, the formation behavior of oxygen precipitates in RTP wafers by heat treatment over a wide temperature range has not been completely clarified. In this study, the effects of heat treatment with various temperatures and durations following RTP on the oxygen precipitates were systematically investigated to clarify the formation behaviors of oxygen precipitates owing to residual  $V_s$ . In addition, we attempted to estimate the formation behavior of oxygen precipitates through our simulation model.

## 2. Experimental Procedure

The CZ–Si wafers listed in Table 1 were used in the RTP experiment. These Si (001)-oriented CZ–Si wafers with a diameter of 300 mm were doped with boron to have a resistivity of 14–27  $\Omega \cdot \text{cm}$  and were mirror-polished. The concentration of interstitial oxygen [Oi] was measured using a Fourier-transform infrared spectroscope (QS-1200, Onto Innovation), following ASTM F121-79. Meanwhile, the concentration of [N] was estimated using nitrogen's segregation coefficient, the Si crystals' solidification ratio, and the amount of doped  $\text{Si}_3\text{N}_4$ . The [Oi] of wafers A, B, and C were set at similar levels. Further, considering the significant effect of nitrogen on the oxygen precipitate density formed by increasing the  $V$  concentrations in the wafers by forming  $V$ -N complexes during RTP [11], [N] was experimentally selected.

For the RTP, the wafers were held at 1350 °C for 30 s in an oxygen atmosphere. The cooling rate was set at 120  $\text{K s}^{-1}$  to retain the excess  $V_s$  generated in the bulk region. A two-step heat treatment was then carried out in a vertical batch furnace after RTP to induce oxygen precipitate nucleation and growth. The temperature of the first step was varied from 750 to 950 °C, and the duration of this step was 0.5–16 h. Meanwhile, the second step was performed at a temperature of 1000 °C for 16 h. The CZ–Si wafers were placed in a vertical batch furnace at 600 °C. The temperature ramp rate in the first step from 600 °C was fixed at 10  $\text{K min}^{-1}$ . In contrast, in the second step, it was fixed at 5  $\text{K min}^{-1}$ .

The depth profiles of oxygen precipitate densities were evaluated by measuring the bulk micro-defects (BMDs), which mainly represent the oxygen precipitates, using an infrared (IR) tomography apparatus (MO-441, Raytex). IR tomography could not accurately evaluate the saturating densities above  $8 \times 10^9 \text{ cm}^{-3}$  because of the overlap of the scattered light of the individual BMDs. However, the actual BMD densities were higher. To determine the differences in BMD densities for each experimental condition, we focused and compared the depth from the wafer surface with BMD densities of up to  $1 \times 10^9 \text{ cm}^{-3}$ , defined as the "precipitate depth". Comparing the precipitate depths for each wafer is equivalent to comparing the BMD densities in the bulk region.

### 3. Experimental Results

The typical depth profiles of the BMD densities and cross-sectional IR tomography images of wafer B ( $[N] = 7.80 \times 10^{14} \text{ cm}^{-3}$ ) are shown in Fig. 2. A high density of BMDs was formed in the bulk region under all heat treatment conditions; in contrast, no BMDs were formed in the surface layers because of the sufficient reduction of the residual  $V$  concentrations due to the out-diffusion of  $V$ s during the cooling process in the RTP. When the first-step temperature was set at 750 and 800 °C, the depth profiles from the wafer surfaces were affected by the heat treatment duration. The profiles at which the BMDs were detectable are shown in Fig. 2(a) and (b). Meanwhile, when the first-step temperature was set at 900 °C, the depths were not affected by the duration, as shown in Fig. 2(c).

To clarify the difference in BMD formation in the first step of the heat treatment under different conditions, we compared the precipitate depths of the BMD densities reaching  $1 \times 10^9 \text{ cm}^{-3}$ . As  $[N]$  increased, the precipitate depth decreased, suggesting that nitrogen effectively enhanced oxygen precipitation owing to the increasing residual  $V$  concentrations. For various  $[N]$ , the lowest precipitate depth was obtained when the first-step temperature was set at 850 °C. A low precipitate depth indicates a high BMD density in the bulk region. In addition, the precipitate depth depended on the heat treatment duration at temperatures below 850 °C, whereas they were weakly affected by the heat treatment duration at temperatures above 850 °C. These results are shown in Fig. 4, including our simulation results.

### 4. Simulation Results and Comparison with the Experimental Results

The simulation process in this study consisted of two steps: calculation of the depth profiles of the residual  $V$  concentrations after RTP and calculation of the oxygen precipitation, including the  $V$  effect during the two-step heat treatment following RTP. The nucleation rate of the oxygen precipitates ( $\text{SiO}_2$ ) was assumed to be proportional to the fourth power of the residual vacancy concentration, and the growth of  $\text{SiO}_2$  was assumed to be diffusion-limited for oxygen atoms. In addition, we assumed that  $I_s$ , which were generated by the growth of the  $\text{SiO}_2$ , the emission ratio of  $I_s$  is 1.2 per  $\text{SiO}_2$  molecule and 0.6 per oxygen atom under a complete strain relaxation condition. The residual  $V$ s are consumed by pair annihilation with  $I_s$ , thus stopping oxygen precipitation owing to the depletion of the residual  $V$ s. For more details, please refer to our past reports [9,10].

A comparison between the BMD depth profiles obtained by the experiments and simulations for wafer B ( $[N] = 7.80 \times 10^{14} \text{ cm}^{-3}$ ) is shown in Fig. 3. The markers and solid lines represent the experimental and simulation results, respectively. The simulations effectively reproduced the profiles of BMDs below the saturation level of the measured density. When the first-step temperature was set at 800 and 900 °C with durations of 2–16 and 0.5–2 h, respectively, the calculated depth profiles were not affected by the duration of the heat treatment, indicating that nucleation was completed even with short durations at 800 and 900 °C. Further, the simulation reproduced the variations in the precipitation depths at  $1 \times 10^9 \text{ cm}^{-3}$  with the  $[N]$  content in the wafers, temperature, and duration of the first step of the heat treatment, as shown in Fig. 4. Specifically, the simulation predicted that the precipitate depths would be shallowest when the first-step temperature was set at 850 °C. In addition, it showed that the precipitate depths would depend on the heat treatment duration at first-step temperatures below 850 °C, whereas they would be largely unaffected by the duration above 850 °C.

The resulting behaviors are explained in Fig. 5 via our simulation. When the first-step temperature was set at 750 °C for 1 h, the BMD density did not increase effectively, which can be ascribed to two reasons. First, the BMDs smaller than the critical radius dissolved during the temperature increase in the second step, as shown in Fig. 5(a). Second, the BMD density does not effectively increase even with a duration of 16 h at 750 °C owing to its low nucleation rate. When the first-step temperature was set at 900 °C for the fast growth of the BMDs in Fig. 5(c), the BMDs did not dissolve during the temperature rise to the second heat treatment step. However, the nucleation stopped earlier because of the consumption of residual  $V_s$  due to the pair annihilation with  $I_s$  generated by the BMD growth. Consequently, the first-step temperature of 850 °C in Fig. 5(b) effectively increased the BMD density.

## 5. Conclusion

This study was aimed at clarifying the formation behavior of oxygen precipitates in RTP wafers treated at 1350 °C in oxygen atmosphere. Regardless of nitrogen concentration, the highest oxygen precipitate density was obtained when the first-step temperature of the two-step heat treatment was set at 850 °C. In addition, the density was affected by the duration of the first heat treatment step at temperatures below 850 °C. In contrast, the density was weakly affected by the duration at temperatures above 850 °C. Based on our simulation, at temperatures below 850 °C, some oxygen precipitates dissolved during the temperature rise owing to their slow growth. In addition, because the nucleation rate was lower, the density did not increase effectively, even at longer durations. The nucleation stopped earlier when the temperature was set at 850 °C or more, even with the high nucleation rate. This was due to the accelerated consumption of the residual  $V_s$  due to  $I_s$  generated by the growth. Consequently, setting the temperature at 850 °C effectively increased the density. Therefore, we concluded that the resulting BMD density was determined based on the nucleation rate, growth size, and timing of the terminal point of nucleation.

## References

- [1] R. Falster, V. V. Voronkov, and F. Quast, *phys. stat. sol. (b)* **222**/1, 219–244 (2000).
- [2] M. Akatsuka, M. Okui, N. Morimoto, K. Sueoka, *Jpn. J. Appl. Phys.* **40**/1, 3055–3062 (2001).
- [3] G. Kissinger, J. Dabrowski, A. Sattler, C. Seuring, T. Müller, H. Richter, and W. von Ammon, *J. Electrochem. Soc.* **154**/6, H454 (2007).
- [4] M. Pagani, R. J. Falster, G. R. Fisher, G. C. Ferrero, and M. Olmo, *Appl. Phys. Lett.* **70**/12, 1572–1574 (1997).
- [5] K. Araki, S. Maeda, T. Senda, H. Sudo, H. Saito, and K. Izunome, *E.C.S. J. Solid State Sci. Technol.* **2**/3, P66–P70 (2013).
- [6] K. Araki, S. Maeda, H. Sudo, T. Aoki, H. Saito, and K. Izunome, *E.C.S. Solid State Lett.* **3**, 114 (2014).
- [7] K. Araki, H. Sudo, and S. Maeda, *E.C.S. Solid State Lett.* **4**/9, P63–P65 (2015).
- [8] S. Maeda, H. Sudo, H. Okamura, K. Nakamura, K. Sueoka, and K. Izunome, *J. Appl. Phys.* **123**, 161591 (2018).
- [9] H. Sudo, K. Nakamura, S. Maeda, H. Okamura, K. Izunome, and K. Sueoka, *E.C.S. J. Solid State Sci. Technol.* **8**/1, P35–P40 (2019).
- [10] H. Sudo, K. Nakamura, H. Okamura, S. Maeda, and K. Sueoka, *J. Appl. Phys.* **131**, 055704 (2022).
- [11] V. V. Voronkov and R. Falster, *J. Electrochem. Soc.* **149**/3, G167 (2002).

Table 1. Interstitial oxygen concentrations [Oi] (ASTM F121-79) and nitrogen concentrations [N] in the CZ-Si wafers.

Wafers	[Oi] ( $10^{18} \text{ cm}^{-3}$ )	[N] ( $10^{14} \text{ cm}^{-3}$ )
A	1.15	2.66
B	1.17	7.80
C	1.26	12.9

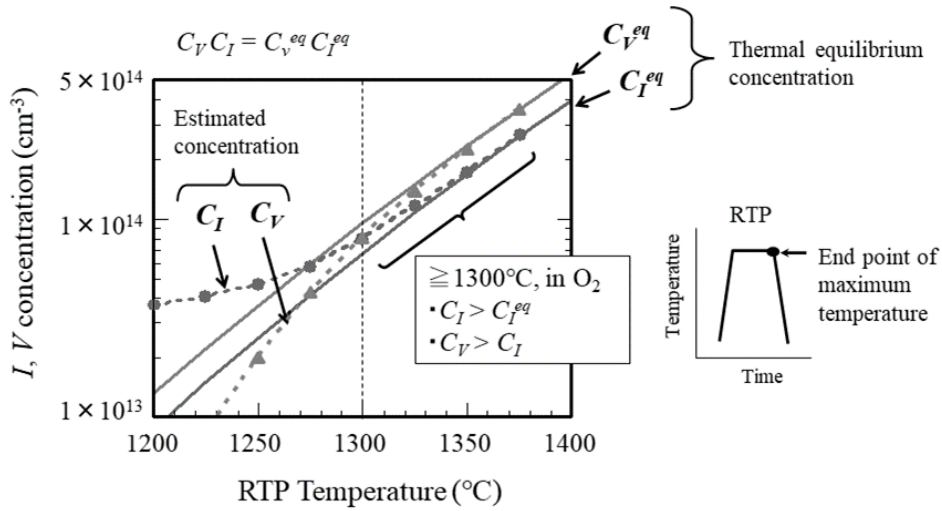


FIG. 1. Relationship between point defect concentration and RTP temperature [8].

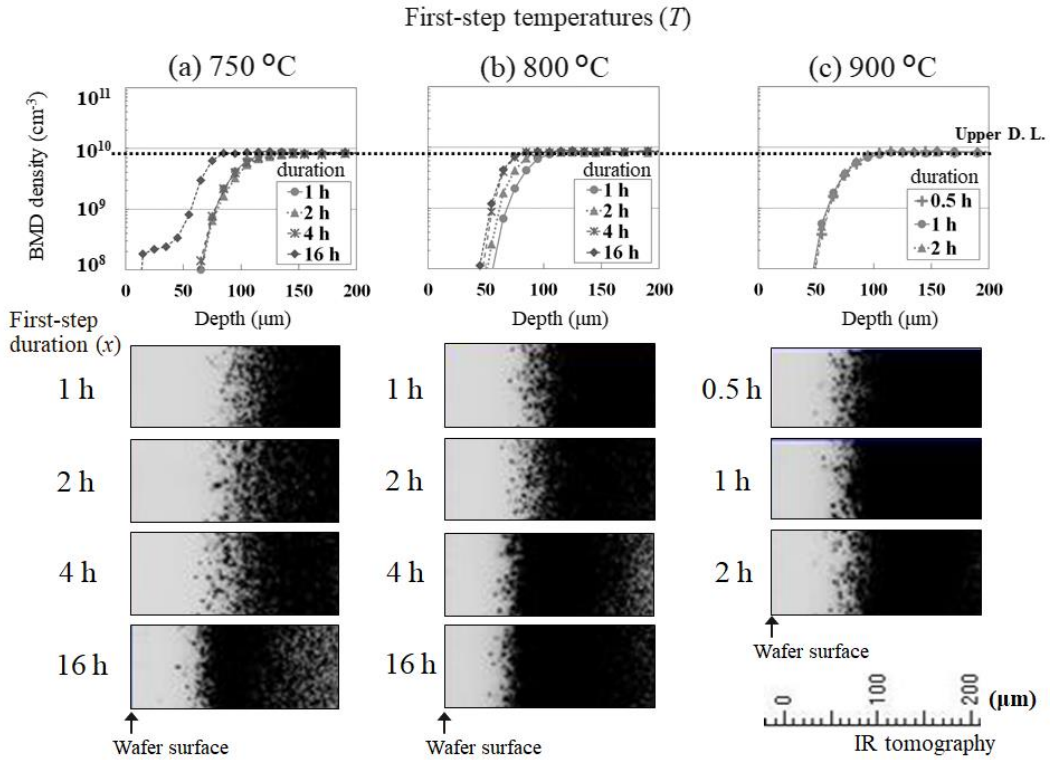


FIG. 2. Depth profiles of BMD densities and cross-sectional IR tomography images of wafer B ( $[N] = 7.80 \times 10^{14} \text{ cm}^{-3}$ ) after the two-step heat treatment ( $T \text{ (}^\circ\text{C)} \times x \text{ (h)} + 1000 \text{ }^\circ\text{C} \times 16 \text{ h}$ ) following RTP. The first-step temperatures ( $T$ ) are (a)  $750 \text{ }^\circ\text{C}$ , (b)  $800 \text{ }^\circ\text{C}$ , and (c)  $900 \text{ }^\circ\text{C}$ . The black dots in the IR tomography images indicate light scattering by the BMDs [10].

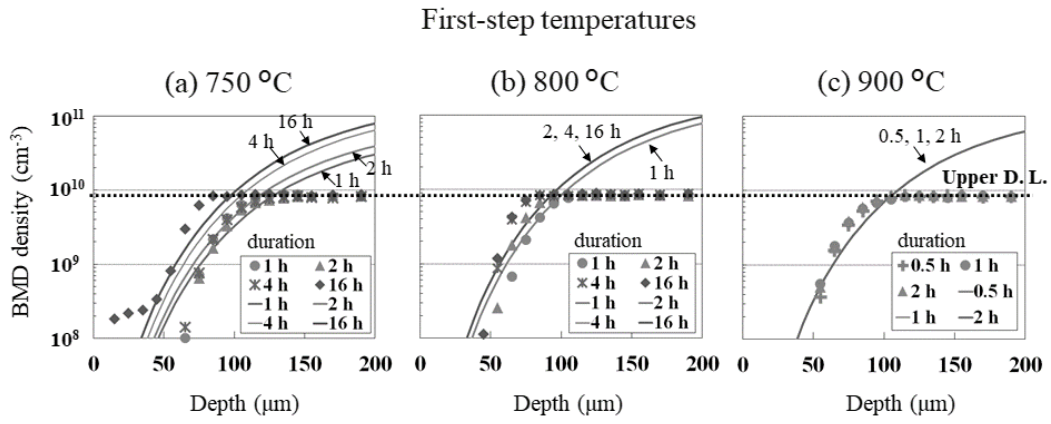


FIG. 3. Comparison of BMD depth profiles obtained by experiments (markers) and simulations (solid lines) for wafer B ( $[N] = 7.80 \times 10^{14} \text{ cm}^{-3}$ ) with first-step heat treatment temperatures of (a) 750 °C, (b) 800 °C, and (c) 900 °C [10].

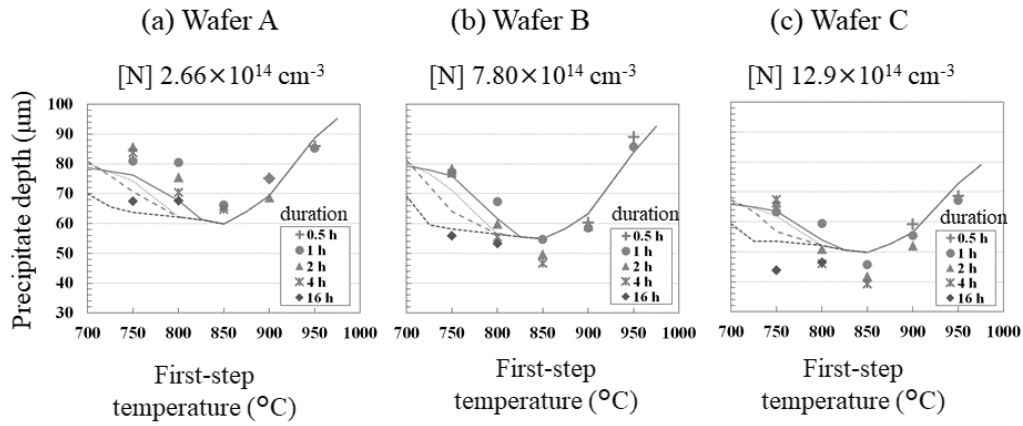


FIG. 4. Experimentally measured (markers) and simulated (solid lines) precipitate depths of CZ-Si wafers (a) A, (b) B, and (c) C [10].

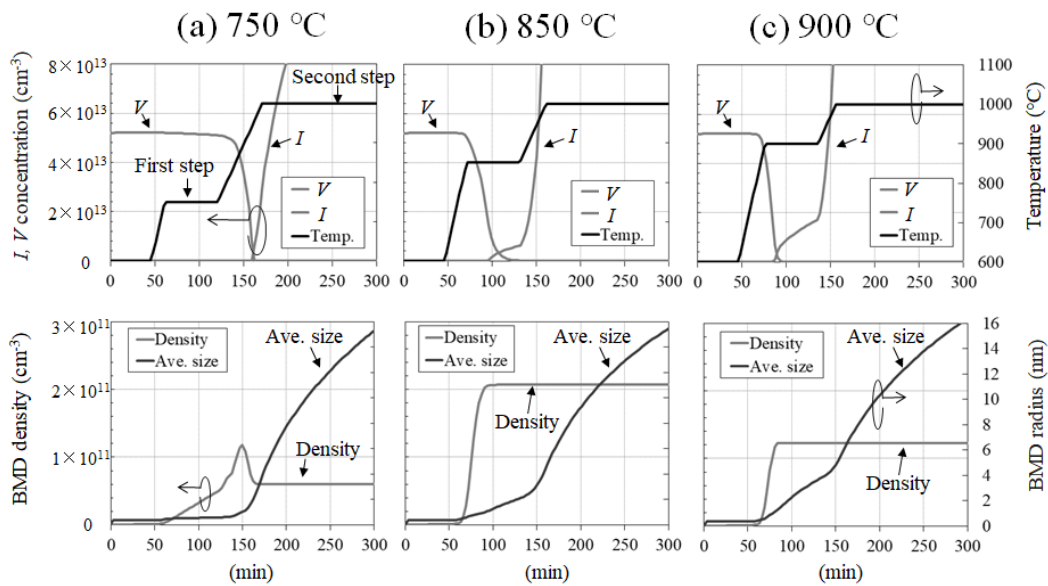


FIG. 5. Comparison of formation behaviors of BMDs in wafer B ( $[N] = 7.80 \times 10^{14} \text{ cm}^{-3}$ ) during first-step heat treatment at (a) 750 °C, (b) 850 °C, and (c) 950 °C for 1 h [10].

**November 8 (Tuesday)**

# **Session E**

Chair: *E. Kamiyama (GlobalWafers Japan)*

**15:30 ~ 17:30**  
(Reception Hall)

## ***In situ* and real-time investigation of the solidification of silicon by X-ray imaging**

Gabrielle Regula<sup>1</sup>, Guillaume Reinhart<sup>1</sup>, Isabelle Périchaud<sup>1</sup>, Hadjer Ouaddah<sup>1</sup>, Maike Becker<sup>1</sup>, Thècle Riberi-Béridot<sup>1</sup>, Maria Tsoustouva<sup>1</sup>, Nathalie Mangelinck-Noël<sup>1\*</sup>

<sup>1</sup>Aix Marseille Univ, Université de Toulon, CNRS, IM2NP, 13397 Marseille, France

\*e-mail: nathalie.mangelinck@im2np.fr

### **Abstract**

Aiming to the production of low cost and high efficiency solar cells based on silicon material, all processes either innovative or conventional face challenges linked to formation and development of the grain structure, distortion of the crystal and crystalline defects during the solidification step. Our contribution consists in studying these key and fundamental solidification mechanisms by conducting *in situ* and time-resolved investigations. Two imaging techniques based on X-ray synchrotron radiation are combined during solidification: X-ray radiography and Bragg diffraction (topography). X-ray radiography brings information on the morphology and kinetics of the solid/liquid (S/L) interface. X-ray Bragg diffraction (topography) gives complementary information about misorientations, structural defect formation and the global and local level of distortion of the crystal. The dynamics of twinning, grain competition, sub-grain formation and of the related crystal distortions have been studied in silicon with this method as well as the effect of the impurities on grain nucleation and defect formation.

### **Introduction**

The development of solar photovoltaic (PV) electricity requires significant advances in research and development to answer to the constantly renewed societal demand for higher conversion efficiency, lower costs and efficient recycling. Silicon is a well-established technology still representing about 90% of the world photovoltaic market. The final grain structure, associated defects (grain boundaries, sub-grains and dislocations) and crystal distortion issued from the solidification step are responsible for PV properties for a large part [1, 2]. Additionally, impurities, from furnace environment, crucibles, doping and feedstock, play a major role as they not only modify grain nucleation and competition during solidification [3, 4] but interact as well with structural defects [5]. As a consequence, for all Si ingot fabrication processes, producing either mono-crystalline or multi-crystalline ingots [6, 7], the control of the grain structure, defect, impurity concentration and segregation during the solidification step remains a major challenge to improve the material properties. This objective can only be attained with a thorough understanding of the crystallisation mechanisms [8-10] and of the complex interaction between growth defects and impurities. Deep understanding of the mechanisms and of their temporality are limited by the difficulty of accessing, from the *ex situ* study of the solidified ingots, to the origin of defective areas. Mechanisms involved during the solidification process can only be fully understood by advanced *in situ* methods based on optical or X-ray techniques [9, 11-23]. In particular, X-ray diffraction imaging using white beam (topography) is used in the field of material sciences to study crystal defects. Any deviation from the perfect plane orientation of the crystal structure, caused for example by dislocations, grain boundaries, or precipitates, results in a contrast [24, 25]. *In situ* studies monitoring the heating, melting and/or solidification stages of silicon crystals have shown to give unique insights into the evolution of dislocations [25, 26], cracks [27, 28], grain nucleation competition and distortion of the crystal structure [9, 20, 29]. Ultimately, this knowledge could be used to optimize the directional

solidification processes to reduce the dislocation density, the residual stress field and impurity inhomogeneity that have an impact on both electrical and mechanical properties of the Si wafers.

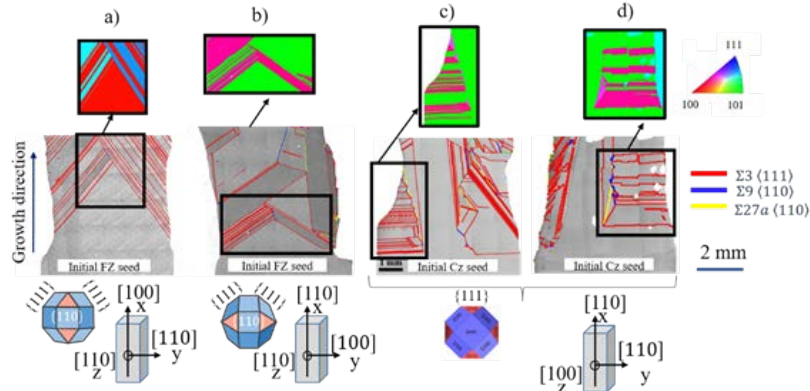
### Experimental techniques

The directional solidification experiments are carried out in a unique IM2NP device named GaTSBI (Growth at high Temperature observed by Synchrotron Beam Imaging), installed at beamline ID19 at the European Synchrotron Radiation Facility (ESRF). GaTSBI is composed of a high temperature directional solidification furnace employed in conjunction with synchrotron radiation X-ray imaging techniques (radiography and Bragg diffraction imaging). Information on the solid–liquid interface dynamics, on the single grain dynamic evolution during growth, the crystalline orientation / misorientation, the qualitative level of crystal distortion as well as the nature and interaction of structural defects in general are obtained. Recently, the experimental setup has been improved to be able to use fully synchronized camera systems to record both topographs (images of the diffraction spots of a particular {hkl} family planes) and radiographs at the same time [22]. The enhancement of the recording frequency now provides the opportunity to study the propagation, multiplication and rearrangement of dislocations by interaction with themselves, grain boundaries and the solid-liquid interface, during the entire experiment [16]. A detailed description of the equipment and of the imaging techniques can be found elsewhere [18, 22]. *Ex situ* electron backscatter diffraction (EBSD) measurement are also performed after solidification and cooling down to room temperature using a FEG-SEM JEOL JSM 7001F equipped with a HKL Nordlys camera. Apart from the inverse pole figure (IPF) orientation maps, the coincidence site lattice map (CSL) is reconstructed to evidence the grain boundaries with a special character.

### Results and discussion

#### 1. Twinning during the solidification:

**Fig 1.** Grain structure and twin boundaries after growth from monocrystalline seeds. Applied temperature gradient  $G$ : 30 K/cm and cooling rate in K/min: (a) FZ<100>-IS, -1 K/min, (b) FZ<110>-IS, -1 K/min, (c) CZ<110>-IS-1, -0.2 K/min and (d) CZ<110>-IS-2,  $G$ : 20 K/cm and  $K$ : -0.2 K/min. Top: Inverse Pole Figure (IPF) map along the growth direction. Middle: CSL (Coincidence Site Lattice) map. Bottom: Seed orientation [18].

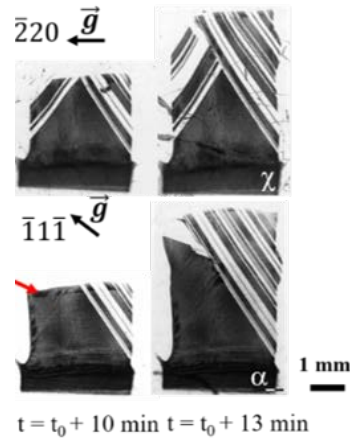
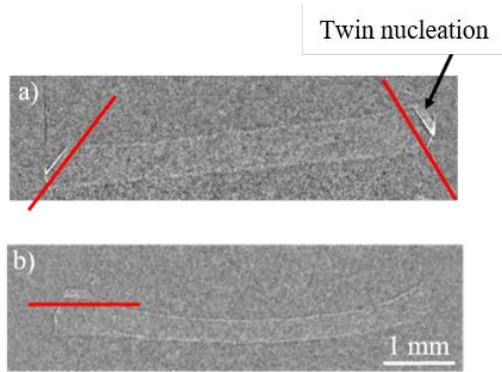


Four typical final grain structures of samples solidified in the GaTSBI furnace are shown in Fig. 1. These samples are solidified from float-zone (FZ) monocrystalline seeds (Fig. 1.a and 1.b) and from Czochralski (Cz) seeds (Fig. 1.c and d) after partial melting of the seed. Cz seeds are used for the cast-mono industry [30]; they contain oxygen (typically:  $0.5-1 \times 10^{18}$  at/cm<sup>3</sup> in Cz ingots compared to  $< 10^{15}$  at/cm<sup>3</sup> in FZ ingots). The coincidence site lattice maps (middle line in Fig. 1) are shown in order to reveal the grain boundary character and in particular the twin boundaries. The samples are solidified from seeds with crystallographic orientations shown Fig.1 (bottom line). A



majority of  $\Sigma 3$  twins (red colour) are observed in all samples which are representative of experiments with FZ and Cz seeds. The  $\Sigma 3$  twins are aligned along  $\{111\}$  facet orientation imposed by the seed crystallographic orientation, as it was also observed by Trempa *et al.* [13]. The fact that the behaviour of FZ and Cz seeds is comparable suggests that the presence of oxygen (O) is not a predominant factor for twin nucleation. Fig. 2.a and 2.b correspond to a snapshot at one instant during solidification showing the solid-liquid interface of samples in Fig. 1.a and 1.c, respectively. These *in situ* X-ray radiography images (Fig. 2) reveal that the solid-liquid interface is smooth during growth under these conditions for both FZ (Fig. 1.a) and Cz (Fig. 1.c) seeds. No destabilization of the interface can be observed in all cases when growing from Cz or FZ seeds.

**Fig. 2.** X-ray radiography images of the solid-liquid interface: (a) FZ<100>-IS, (b) CZ<110>-IS-1 [18].

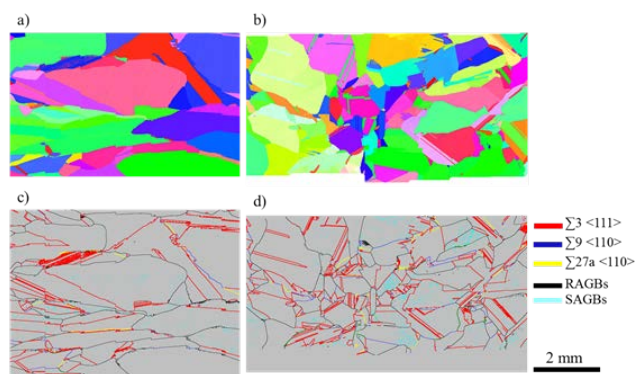
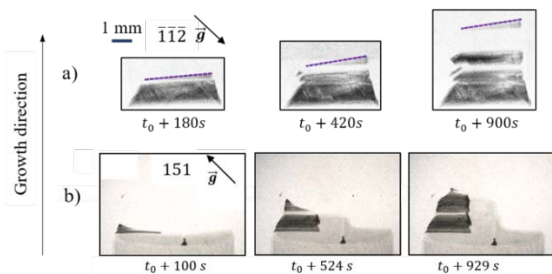


**Fig. 3.** Topographs recorded during solidification of FZ<100>-IS [20].

Despite the global smooth interface,  $\{111\}$  facets can be clearly seen on the X-ray radiography images at the edges of the sample (Fig. 2). It was verified that they correspond to the projection of  $\{111\}$  facets (red lines on Fig. 2). Twin nucleation takes place regularly on these  $\{111\}$  facets as can be seen for example on Fig. 2.a (right) and Fig. 2.b (left). The *in situ* topographs (Fig. 3) corresponding to the case of Fig. 2.a show that side  $\Sigma 3$  twins develop at the edges from  $\{111\}$  facets and compete with the main central grain issued from the seed [10, 20].

## 2. Successive Twinning and growth of the twins

**Fig 4.** Topographs corresponding to twinning zones, a) CZ<110>-IS-2, b) CZ<110>-IS-1 [18].



**Fig. 5.** IPF and CSL maps (bottom line) obtained by EBSD a) and c) MX1-AG sample; b) and d) MX2-AG sample.

Successive twinning is evidenced (alternation of two crystallographic orientations/colours in Fig.1 and stripped/hatched aspect of the topographs in Fig. 3 and 4) during solidification in all solidified samples. It is also classically observed in industrial size ingots [17,18]. The hatched aspect on the topographs during solidification (Fig. 3 and 4) corresponds to an orientation contrast due to the nature of twinning [14,15]. Topographs collected at

different times during the solidification of samples CZ<110>-IS-1 and CZ<110>-IS-2 (corresponding to the experiments in Fig. 1.c and Fig. 1.d, respectively) are shown in Fig. 4. The purple dotted line is added in Fig. 4.a to indicate the corresponding solid-liquid interface shape as observed in the radiographs. The observation of the upper part of the diffraction spots shows that the twin nucleation occurs at the edges of the samples at the solid-liquid-vacuum-crucible phase line as also seen in the radiographs (Fig. 2) where the highest undercooling is measured. The twin growth rate at the nucleation instant (about 15  $\mu\text{m/s}$ ) exceeds the one of the global solid-liquid interface (2  $\mu\text{m/s}$ ). The consequence is that the twin grains that nucleate on the edges grow vertically very fast and in advance compared to the global solid-liquid interface inducing the triangular shape recorded on the topographs during solidification. As a subsequent step, a growth rate plateau is measured, after which the next twin nucleation can take place [8]. The nucleation of the twin and growth upwards in the directional solidification direction go along with the propagation of the twin grains towards the centre as revealed by the topographs (Fig. 4). A main result of these investigations, that can only be obtained *in situ* and real-time, is that only  $\Sigma 3\langle 111 \rangle$  type twinned grains nucleate during growth of FZ or Cz seeded samples.

### 3. Grain competition and crystal distortion

Crystal distortion is observed at the location of  $\Sigma 3$  twin nucleation as can be seen on the topographs (e.g. Fig. 3). It is revealed by the enhanced black contrast observed at the location of twin nucleation. Higher order twin boundaries such as  $\Sigma 9\langle 110 \rangle$  and  $\Sigma 27a\langle 110 \rangle$  do not nucleate during solidification and are only the result of grain encounter and competition in all experiments based on FZ or Cz seeds [8,10,15]. A statistical analysis of the percentage of the different types of twin boundaries was obtained from EBSD measurements on several samples from FZ seeding only to exclude the influence of impurities. The majority of twin boundaries are of  $\Sigma 3$  type (typically more than 90 %). As the samples grow, more and more  $\Sigma 3$  twin grains nucleate so that encounters are more likely to occur increasing the amount of higher order twin boundaries as the solidification length increases which produces more and more complex grain structure as e.g. in the case of industrial processes. The competition and formation of higher order twin boundaries go along with distortions and the accumulation of dislocations. The dislocation behaviour when meeting grain boundaries varies according to the grain boundary type. Lower or no dislocation accumulation and distortion are observed at the level of  $\Sigma 3$  twin boundaries. Indeed, there is a higher probability that dislocations can move along  $\Sigma 3$  twin boundaries due to the  $\{111\}$  common glide planes that exists at the level of  $\Sigma 3$  twin boundaries compared to the case of higher order twin boundaries [20]. On the contrary, strain (black contrast on the topographs) is observed in all cases at the level of higher order twin boundaries either because cross-slip of dislocations is not possible and/or because they are responsible for the emission of dislocations as observed in particular for  $\Sigma 27a\langle 110 \rangle$  grain boundaries [9].

### 4. Grain structure in silicon samples containing light impurities

Fig. 6 shows the IPF and CSL maps in samples MX1-AG and MX2-AG both cut in as-grown ingots after the cold crucible continuous casting process [31]. The same processing conditions were applied but the concentrations in carbon (C) and oxygen (O) differ:  $[\text{O}_i] = 3.7 \times 10^{16}$  and  $6.7 \times 10^{16}$   $\text{at/cm}^3$ ,  $[\text{C}_s] = 7.6 \times 10^{16}$  and  $2.2 \times 10^{17}$   $\text{at/cm}^3$  for MX1-AG and MX2-AG, respectively. The first qualitative visual assessment indicates that there is no preferential growth crystallographic orientation in both samples. Besides, the number of grains is very different, about twice more grains are present inside sample MX2-AG compared with sample MX1-AG for the same surface. The corresponding percentages of  $\Sigma 3$  (70 and 61 %),  $\Sigma 9$  (7 and 8 %),  $\Sigma 27a$  and  $b$  (3 and 2 %) twin boundaries and of random angle grain boundaries (RAGB: 17 and 27 %) are given for MX1-AG and MX2-AG, respectively. These

results are representative of other parts of the same wafers, of other samples of the same type as-grown from the industrial process and of samples processed in the GaTSBI furnace. The amount of  $\Sigma 3$  twin boundaries is significantly lower for samples of type MX2 compared to MX1. At the same time, the amount of high order twin boundaries and of random angle grain boundaries increases. The presence of a higher concentration in light impurities, mostly C and O here, seems to be at the origin of the formation of additional grains during growth. Indeed, it was proven that the presence of precipitates reduces the nucleation undercooling of the first Si crystals [38]. Additionally, it is expected that impurities or precipitates accumulate in grain boundary grooves as proposed by Fujiwara *et al.* [13] and as discussed as well by Autruffe *et al.* [8]. Inside grain boundary grooves the undercooling is higher as measured in our previous work [9] so that there is a higher probability of grain nucleation especially if some impurities/precipitates are present. As nucleation takes place on precipitates or impurities, the new grain does not have to be necessarily in twin relationship at the level of the {111} facets that can exist in the grain boundary groove.

##### 5. Grain structure formation in the presence of Cu

The effect of Cu during solidification was also studied [21]. First, even for concentrations in Cu as low as  $10^{15}$ - $10^{17}$  at/cm<sup>3</sup>, the dendritic destabilisation of the solid-liquid interface is observed by *in situ* X-ray radiography whereas it has not been observed for samples contaminated with light impurities [21]. Impurities accumulate above the solid-liquid interface during solidification when they have an equilibrium partition ratio greater than one which is the case of both C and Cu. In the case of Cu, Cu accumulates above the solid-liquid interface which ultimately leads to interface destabilisation whereas impurities like C regularly precipitate. Second, no significant effect of Cu on the grain structure establishment has been characterised. Third, a higher Cu concentration is measured at the grain boundaries even of the highest quality type ( $\Sigma 3$  twin boundaries) compared to areas where no structural defects are evidenced and it degrades the electrical properties [21]. It is striking that the effect on the electrical properties is significant even for initial concentrations of Cu of the order of  $10^{15}$  at/cm<sup>3</sup>.

### Conclusion and prospects

Time-resolved phenomena that occur during Si crystal growth such as grain and twin nucleation, grain competition, defect generation and their evolution and cross-interaction are investigated *in situ* by X-ray radiography and topography imaging. Twinning observed with the studied processing conditions is a growth rather than a distortion phenomenon. Moreover, only  $\Sigma 3$  twins nucleate during growth in samples from Cz and FZ origin, higher order grain boundaries being solely the result of grain competition. In the presence of light impurities (O and C in this work), the resulting grain structure is constituted by a higher proportion of high-order twin and of RAGBs compared with the case of low contaminated samples in both model and as-grown industrial samples. Cu, which was studied as a model of a fast diffusing metallic impurity, segregates during solidification and induces a dendritic destabilization of the interface. However, there is no significant modification of the grain structure, indicating that Cu does not seem to be significantly involved in grain nucleation. In the future, the correlation between grain structure, defect formation, local chemical segregation and electrical properties will be further investigated and extended to samples with other types of defects and impurities. The simultaneous and time-resolved recording of radiographs and topographs now provides the opportunity to study the propagation and dynamics of dislocations, their interaction with grain boundaries and the solid-liquid interface, and the development of crystal distortion during the whole process.

## REFERENCES

- [1] G. Stokkan, Y. Hu, Ø. Mjøs, M. Juel, *Sol Energ Mat Sol C* **130**, 679 (2014).
- [2] J. Huang, S. Yuan, X. Yu, D. Yang, *physica status solidi (a)* (2022) 2200448.
- [3] B. Heilbronn, F. De Moro, E. Jolivet, E. Tupin, B. Chau, R. Varrot, B. Drevet, S. Bailly, D. Rey, H. Lignier, Y. Xi, T. Riberi-Béridot, N. Mangelinck-Noël, G. Reinhart, G. Regula, *Crystal Research and Technology* **50**, 1 (2014).
- [4] M. Beaudhuin, G. Chichignoud, P. Bertho, T. Duffar, M. Lemiti, K. Zaïdat, *Materials Chemistry & Physics* **133**, 284 (2012).
- [5] I. Périchaud, *Solar Energy Materials & Solar Cells* **72**, 315 (2002).
- [6] C.W. Lan, A. Lan, C.F. Yang, H.P. Hsu, M. Yang, A. Yu, B. Hsu, W.C. Hsu, A. Yang, *Journal of Crystal Growth* **468**, 17 (2017).
- [7] A. Jouini, D. Ponthenier, H. Lignier, N. Enjalbert, B. Marie, B. Drevet, E. Pihan, C. Cayron, T. Lafford, D. Camel, *Progress in Photovoltaics: Research and Applications* **20**, 735 (2012).
- [8] A. Autruffe, L. Vines, L. Arnberg, M. Di Sabatino, *Journal of Crystal Growth* **372(0)**, 180 (2013).
- [9] M.G. Tsoutsouva, T. Riberi – Béridot, G. Regula, G. Reinhart, J. Baruchel, F. Guittonneau, L. Barrallier, N. Mangelinck-Noël, *Acta Materialia* **115**, 210 (2016).
- [10] M. Trempa, C. Reimann, J. Friedrich, G. Müller, D. Oriwol, *Journal of Crystal Growth* **351**, 131 (2012).
- [11] K. Fujiwara, L.-C. Chuang, K. Maeda, *High Temperature Materials and Processes* **41(1)**, 31 (2022).
- [12] L.-C. Chuang, K. Maeda, H. Morito, K. Shiga, W. Miller, K. Fujiwara, *Materialia* **7**, 100357 (2019).
- [13] K. Fujiwara, M. Ishii, K. Maeda, H. Koizumi, J. Nozawa, S. Uda, *Scripta Materialia* **69(3)**, 266 (2013).
- [14] K. Fujiwara, K. Maeda, N. Usami, G. Sazaki, Y. Nose, K. Nakajima, *Scripta Materialia* **57**, 81 (2007).
- [15] K. Fujiwara, W. Pan, K. Sawada, M. Tokairin, N. Usami, Y. Nose, A. Nomura, T. Shishido, K. Nakajima, *Journal of Crystal Growth* **292(2)**, 282 (2006).
- [16] S.W. Neves Dias, M. Becker, H. Ouaddah, I. Périchaud, G. Reinhart, N. Mangelinck-Noël, G. Regula, *physica status solidi (b)* **2100594**, 1 (2022).
- [17] M.G. Tsoutsouva, G. Regula, B. Rynningen, P.E. Vullum, N. Mangelinck-Noël, G. Stokkan, *Acta Materialia* **210**, 116819 (2021).
- [18] H. Ouaddah, M. Becker, T. Riberi – Béridot, M.G. Tsoutsouva, V. Stamelou, G. Regula, G. Reinhart, I. Périchaud, F. Guittonneau, L. Barrallier, J.-P. Valade, A. Rack, E. Boller, J. Baruchel, N. Mangelinck-Noël, *Crystals* **10**, 555 (2020).
- [19] M. Becker, E. Pihan, F. Guittonneau, L. Barrallier, G. Regula, H. Ouaddah, G. Reinhart, N. Mangelinck-Noël, *Sol Energ Mat Sol C* **218**, 110817 (2020).
- [20] T. Riberi – Béridot, M.G. Tsoutsouva, G. Regula, G. Reinhart, F. Guittonneau, L. Barrallier, N. Mangelinck-Noël, *Acta Materialia* **177**, 141 (2019).
- [21] H. Ouaddah, I. Périchaud, D. Barakel, O. Palais, M. Di Sabatino, G. Reinhart, G. Regula, N. Mangelinck-Noël, *physica status solidi (a)* **1900298**, 1 (2019).
- [22] M. Becker, G. Regula, G. Reinhart, E. Boller, J.-P. Valade, A. Rack, P. Tafforeau, N. Mangelinck-Noel, *Journal of Applied Crystallography* **52(6)**, 1312 (2019).
- [23] J.-I. Chikawa, *Journal of Crystal Growth* **24-25**, 61 (1974).
- [24] J. Baruchel, M. Di Michiel, T. Lafford, P. Lhuissier, J. Meyssonier, H. Nguyen-Thi, A. Philip, P. Pernot, L.

Salvo, M. Scheel, *Comptes Rendus Physique* **14(2)**, 208 (2013).

[25] A.N. Danilewsky, J. Wittge, A. Croell, D. Allen, P. McNally, P. Vagovič, T. dos Santos Rolo, Z. Li, T. Baumbach, E. Gorostegui-Colinas, J. Garagorri, M.R. Elizalde, M.C. Fossati, D.K. Bowen, B.K. Tanner, *Journal of Crystal Growth* **318(1)**, 1157 (2011).

[26] F. Vallino, J.-P. Château, A. Jacques, A. George, *Materials Science and Engineering: A* **319–321(0)**, 152 (2001).

[27] A. Danilewsky, J. Wittge, K. Kiefl, D. Allen, P. McNally, J. Garagorri, M.R. Elizalde, T. Baumbach, B.K. Tanner, *Journal of Applied Crystallography* **46(4)**, 849 (2013).

[28] A. Rack, M. Scheel, A.N. Danilewsky, *IUCrJ* **3(2)**, 108 (2016).

[29] T. Riberi-Béridot, N. Mangelinck-Noël, A. Tandjaoui, G. Reinhart, B. Billia, T. Lafford, J. Baruchel, L. Barrallier, *Journal of Crystal Growth* **418**, 38 (2015).

[30] A. Jouini, D. Ponthenier, H. Lignier, N. Enjalbert, B. Marie, B. Drevet, E. Pihan, C. Cayron, T. Lafford, D. Camel, *Progress in Photovoltaics: Research and Applications* **20(6)**, 735 (2012).

[31] B. Gallien, T. Duffar, S. Lay, F. Robaut, *Journal of Crystal Growth* **318**, 208 (2011).

## Defects in cast-mono silicon

Deren Yang<sup>1, 2\*</sup>

<sup>1</sup> *State Key Lab of Silicon Materials and School of Materials Science and Engineering, Zhejiang University, 28 Zheda Road., Hangzhou, 310027, China*

<sup>2</sup> *School of Materials Science and Engineering, NingboTech University, 1 Qianhu South Road, Ningbo, 315199, China*

e-mail: [mseyang@zju.edu.cn](mailto:mseyang@zju.edu.cn)

### Abstract

Photovoltaic (PV) has developed rapidly in the world in last 20 years. It is clear that crystalline silicon including Czochralski silicon (Cz-Si) and multicrystalline silicon (mc-Si) is the main material and occupies more 97% market share in 2021. In current, the main challenge for Si PV is to lower cost and to increase the efficiency of solar cells. Cast-mono crystalline silicon (CM-Si) combining the advantages of both Cz-Si and mc-Si has attracted much attention. CM-Si is mostly single crystalline and could be texturized by sodium hydroxide to lower reflectivity. Therefore, CM-Si should be lower cost and higher efficiency.

In this presentation, we give a review on our recent work about the defects of CM-Si during the growth and solar cell fabrication. It is considered that dislocations in CM-Si, especially when the dislocation density is higher than  $1 \times 10^6 / \text{cm}^2$ , have seriously influence on the quality of crystalline silicon and cut down the efficiency of solar cells. Moreover, the dislocation density of CM-Si must be controlled within an acceptable range in the crystal growth process. By designing the orientation of seeds, grain boundaries originated from the junction of seeds can be controlled, and then the density of random dislocations could be suppressed. The experiments could help better understand the pros and cons of current CM-Si and boost its application in industry.

### REFERENCES

- [1] X. Gu, X. Yu, K. Guo, L. Chen, D. Wang, D. Yang, *Solar Energy Materials & Solar Cells* **101**, 95(2012).
- [2] D. Hu, S. Yuan, L. He, H. Chen, Y. Wan, X. Yu, D. Yang, *Solar Energy Materials & Solar Cells* **140**, 121(2015).
- [3] X. Mao, X. Yu, S. Yuan, and D. Yang, *Applied Physics Express* **12**, 051012.(2019) .
- [4] F. Zhang, X. Yu, D. Hu, S. Yuan, L. He, R. Hu, and D. Yang, *Solar Energy Materials and Solar Cells* **193**, 214 (2019).
- [5] J. Huang S. Yuan, H. Chen, D. Hu, L. Wang, D. Yang, X. Yu, *Journal of Crystal Growth* **596**, 126820(2022)

### III-N optical devices: physical processes limiting efficiency and reliability

M. Meneghini<sup>1,6</sup>, C. De Santi<sup>1</sup>, M. Buffolo<sup>1</sup>, A. Caria<sup>1</sup>, F. Piva<sup>1</sup>, C. Casu<sup>1</sup>, N. Roccatò<sup>1</sup>, J. F. Carlin<sup>2</sup>, N. Grandjean<sup>2</sup>, A. Tibaldi<sup>3</sup>, F. Bertazzi<sup>3</sup>, M. Goano<sup>3</sup>, G. Verzellesi<sup>4</sup>, N. Trivellini<sup>1,5</sup>, G. Meneghesso<sup>1</sup>, E. Zanoni<sup>1</sup>

1. Department of Information Engineering, University of Padova, via Gradenigo 6/B, 35131 Padova, Italy

2. Institute of Physics, Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland

3. Politecnico di Torino, Corso Duca degli Abruzzi, 24, 10129 Torino, Italy

4. Università di Modena e Reggio Emilia, via Amendola 2, Pad. Morselli, 42122 Reggio Emilia, Italy

5. Department of Industrial Engineering, University of Padova, via Gradenigo 6/B, 35131 Padova, Italy

6. Department of Physics and Astronomy, University of Padova, via Gradenigo 6/B, 35131 Padova, Italy

E-mail: [matteo.meneghini@unipd.it](mailto:matteo.meneghini@unipd.it)

III-N materials (including gallium nitride and its alloys) have excellent properties for the fabrication of high-efficiency light-emitters. Thanks to the use of InGaN and AlGaIn ternary semiconductors, it is possible to cover a wide range of emission wavelengths, from the deep-ultraviolet (UV) to the visible spectrum. This makes III-N devices ideal for a large number of application fields, from automotive to lighting, from sensing to disinfection.

III-N materials are typically grown heteroepitaxially on foreign substrates, as sapphire, silicon carbide or silicon. This may result in a relatively large density of both point and extended defects, that may impact on the electrical and optical performance of the devices, as well as on their reliability. Fig. 1 reports the simplified structure and the band diagram of an InGaN-based light-emitting diode.

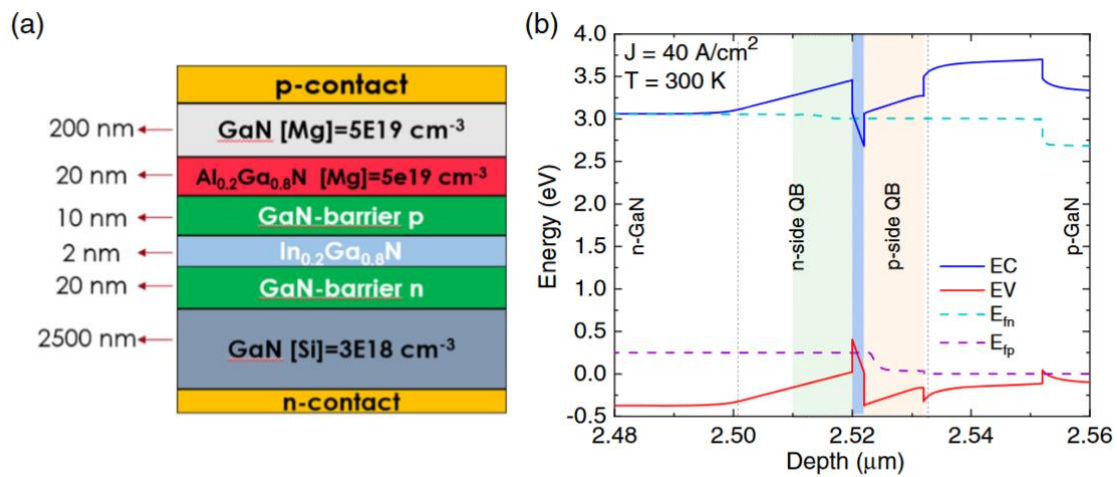


Fig. 1: (a) schematic structure of an InGaN-based light-emitting diode and (b) related band diagram (reproduced from [1], licensed under CC BY 4.0, <https://creativecommons.org/licenses/by/4.0/>)

This presentation will review the most relevant processes that limit the performance and reliability of III-N light-emitting diodes, by presenting a set of case studies recently analyzed within our research group.

The attention will be focused on: a) the methodologies for identifying the presence of defects in GaN, with specific reference to deep-level transient spectroscopy (DLTS) and deep-level optical spectroscopy (DLOS); b) the properties of common defects in GaN, with reference to the energy position in the bandgap (Fig. 2), and the capture cross section and the resulting non-radiative lifetime (Fig. 3); c) the impact of defects on the sub turn-on

voltage electrical characteristics, and the role of trap-assisted tunneling (TAT); d) the dependence of defect density on the indium concentration in the quantum wells; e) the most common ageing processes and indicators for InGaN light-emitting diodes, and related discussion.

The presentation will include an introductory part, for members of the audience who are not familiar with the topic, and a more specific section which is focused on research-oriented results. This will allow members of the audience to get an update in this relevant field of research.

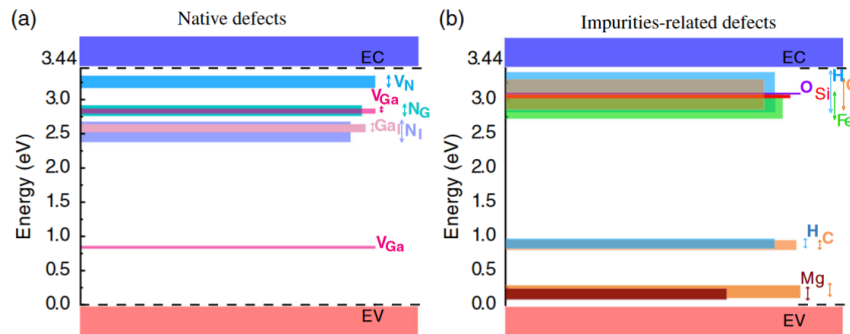


Fig. 2: Position of the most common a) native and b) impurity-related defects within the bandgap of GaN.

Extended defects have been omitted for clarity (reproduced from [1], licensed under CC BY 4.0,

<https://creativecommons.org/licenses/by/4.0/>)

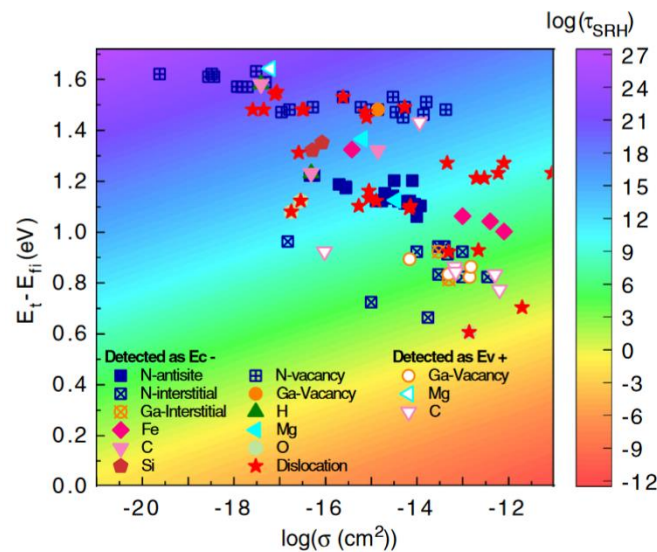


Fig. 3: plot of trap level in function of capture cross section, expressed in log scale, of experimentally characterized deep levels commonly found in GaN (only trap levels with associated physical origin have been included). The underlying heatmap represents the logarithm of the SRH lifetime at 300 K normalized for a trap concentration equal to  $N_t=10^{15} \text{ cm}^{-3}$  (reproduced from [1], licensed under CC BY 4.0,

<https://creativecommons.org/licenses/by/4.0/>)

## REFERENCES

[1] Buffolo, M., Caria, A., Piva, F., Roccatò, N., Casu, C., De Santi, C., Trivellini, N., Meneghesso, G., Zanoni, E. and Meneghini, M. (2022), Defects and Reliability of GaN-Based LEDs: Review and Perspectives. *Phys. Status Solidi A*, 219: 2100727. <https://doi.org/10.1002/pssa.202100727>



**November 9 (Wednesday)**

# **Session F**

*Chair: N. Fukata (NIMS)*

**9:30 ~ 11:30**

**(Noh Theater Hall “Tenjin9”)**

## Creation of Spin Defects in Silicon Carbide by Particle Irradiation for Quantum Applications

Takeshi Ohshima<sup>1\*</sup>

<sup>1</sup>*Quantum Materials and Applications Research Center (Quarc), National Institutes for Quantum Science and Technology (QST), 1233 Watanuki, Takasaki, 370-1292, Japan*

e-mail: ohshima.takeshi@qst.go.jp

### Abstract

Point defects in silicon carbide (SiC) attract a great attention from quantum technologies since some of them act as single photon emitters and/or spin defects which can be applied to quantum qubits and/or quantum sensors. Energetic particle irradiation is one of the useful methods to create such defects in SiC. Here, irradiation methodologies for the creation of defects are introduced. Quantum sensing using silicon vacancies ( $V_{Si}$ ) which are created in SiC by particle beam writing (PBW) technique is also shown.

### Introduction

Spin defects in wide bandgap semiconductors are expected to be applied to spin qubits and quantum sensors. Negatively charged nitrogen-vacancy in diamond is a well-known spin defect which can act as a spin qubit and a quantum center at room temperature [1]. However, diamond has an issue such as a host material since a large size wafer with high quality has not yet been achieved. Silicon carbide (SiC) is paid attention to as a host material for spin defects since SiC has been developed as a host material for power electronics and as a result large wafers with relatively high quality are commercially available. Besides, device fabrication process has been developed.

In previous studies [2-5], following spin defects in SiC have been reported. Negatively charged silicon vacancy ( $V_{Si}$ ) is known as a spin defect which has  $S = 3/2$ .  $V_{Si}$  shows luminescence at wavelengths around 900 nm, and its luminescence can be detected even at room temperature [2]. Electron spin in  $V_{Si}$  can be manipulated at room temperature, and the intensity of its luminescence depends on spin states ( $m_s = \pm 3/2$  or  $\pm 1/2$ ). Then, its spin states can be clarified using optically detected magnetic resonance (ODMR) [2]. Neutral divacancy ( $V_{Si}V_C$ ) is also known as a spin defect in SiC, which has  $S = 1$  and luminescence around 1100 nm.  $V_{Si}V_C$  is expected to be applied to a spin qubit since its luminescence peak is sharp although its spin can be manipulated at only low temperature using ODMR [3]. Carbon anti-site carbon vacancy pair ( $C_{Si}V_C$ ) is a very bright single photon emitter with luminescence around 700 nm even at room temperature [4]. However, spin manipulation for  $C_{Si}V_C$  has not yet been achieved. Negatively charged nitrogen-vacancy ( $N_C V_{Si}$ ) in SiC is also known as a spin defect ( $S = 1$ ) and acts as single photon emitter which shows luminescence around 1300 nm at room temperature although so far, its creation methodology has not yet developed well [5].

Particle irradiation is one of the useful as well as powerful methods to create spin defects because energetic particles can create displace damage in materials. Electron beams with energies of MeV range are often used to create uniform spin defects in depth since the penetration depth of MeV-range electrons are milli-meter or more (more than the thickness of wafers). On the other hand, ion beams are useful if spin defects should be locally created in samples. Thus, choosing ion species and energy, spin defects can be created in the certain depth.

In this study, we create  $V_{Si}$  in SiC using the PBW technique and demonstrate quantum sensing at local areas in SiC devices using  $V_{Si}$ .

## Experimental

Planar diodes were fabricated on an epitaxial layer of 4H-SiC grown on a 4H-SiC substrate by chemical vapor deposition. N-/p-type regions were formed by phosphorus (P) /aluminum (Al) ion implantation and subsequently annealing at 1800°C for 5 min in argon atmosphere. The details for the fabrication of SiC pn diodes are described in elsewhere [6]. For the creation of  $V_{Si}$ , particle beam writing (PBW) was carried out at TIARA, QST Takasaki (Fig. 1) [7]. Focused proton or helium (He) beams with a diameter of 1 $\mu$ m in energy ranges between 0.5 and 3 MeV were applied to create  $V_{Si}$  in SiC pn diodes.

Photoluminescence (PL) was measured using a home-built confocal microscope (CFM) at room temperature. Laser with a wavelength of 532 or 671 nm was used for the excitation of  $V_{Si}$ . For the measurement of photons from  $V_{Si}$ , long pass filters (830 and 900 nm) were installed in the CFM system.

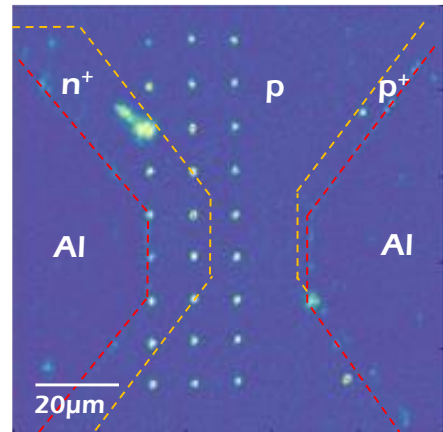
## Results and discussion

Figure 2 shows PL map obtained for a SiC diode irradiated with protons at 0.5 MeV using PBW. Protons at  $1 \times 10^7$  particles were introduced into each spot. Bright spots are observed in the SiC diode. The location for each spot corresponds to locations of proton irradiation. As a result of the PL spectra for spots, it is confirmed that  $V_{Si}$ s are created at the spots. To confirm the change in the electrical characteristics of pn diode irradiated using PBW, current-voltage ( $I$ - $V$ ) characteristics are measured. Figure 3 shows  $I$ - $V$  curves for a SiC pn diode before and after PBW. The irradiation pattern is the same as the pattern shown in Fig. 2. Protons at  $3 \times 10^7$  particles were irradiated into each spot. As shown in Fig. 3, no significant degradation of the characteristics of the SiC diode are obtained.

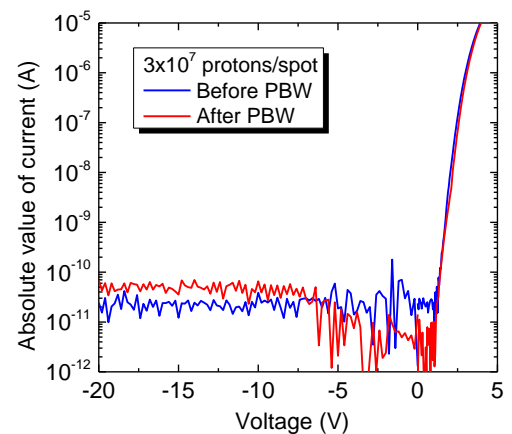
Next, we conduct temperature and magnetic field (induced by current) measurement using quantum sensing based on  $V_{Si}$  created in SiC diodes by PBW. For temperature sensing in SiC diodes, the results are reported in ref. [8]. So, in this study, we will show magnetic field sensing in SiC devices. Figure 4 shows PL map for  $V_{Si}$  created in a SiC diode which was used for local magnetic field sensing induced by current flowing. The external magnetic field at 1 mT was applied



**Fig. 1** Photo of PBW line at TIARA, QST Takasaki

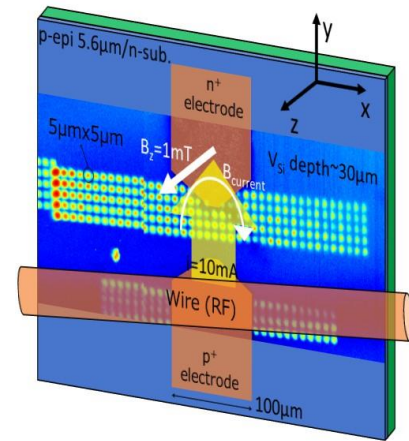


**Fig. 2** PL map for a SiC diode with luminescence from  $V_{Si}$ s created by PBW. Laser with a wavelength of 671 nm was used for excitation.



**Fig. 3** Typical  $I$ - $V$  characteristics of SiC pn diodes before and after PBW. Protons at  $3 \times 10^7$  were introduced into a spot.

perpendicular to the sample surface to obtain clear ODMR signals, and radio frequency was applied to samples using a copper wire on the sample. Schematic images of the magnetic field and wire are also shown in Fig. 4. The forward current at 10 mA is flowed in the diode by applying forward voltage. As a result of ODMR measurements for  $V_{Si}$  created using PBW, the current induced magnetic field about 0.07~0.17 mT are detected. This result suggests that the information at local areas in SiC devices can be obtained by quantum sensing for  $V_{Si}$  locally created in SiC devices.



**Fig. 4** PL map for  $V_{Si}$  created in a SiC diode for quantum sensing.

## Summary

SiC is expected to be applied to a host material for spin defects acting as quantum bits and/or quantum sensors. Particle irradiation, especially PBW, is useful and powerful method to create such spin defects in SiC. In this study, we demonstrated the creation of  $V_{Si}$  in SiC diodes without no significant degradation of their electrical characteristics using PBW. Magnetic field at certain locations in SiC devices, which was induced by forward current flowing, was measured using quantum sensing based on  $V_{Si}$ .

## Acknowledgments

This study was conducted by the collaboration with CREIPI, AIST and Univ. Stuttgart. I am very thankful to them for their support. This study is partially supported by Q-LEAP (JPMXS0118067395), ATLA (JPJ004596) and KAKENHI (20H00355 and 21H04553).

## REFERENCES

- [1] F. Jelezko, J. Wrachtrup, Phys. Stat. Sol. (a) **203**, 3207 (2006) .
- [2] M. Widmann, S.-Y. Lee, T. Rendler, N. T. Son, H. Fedder, S. Paik, L.-P. Yang, N. Zhao, S. Yang, I. Booker, A. Denisenko, M. Jamali, S. A. Momenzadeh, I. Gerhardt, T. Ohshima, A. Gali, E. Janzén, J. Wrachtrup, Nature Materials **14**, 164 (2015).
- [3] D. J. Christle, A. L. Falk, P. Andrich, P. V. Klimov, J. U. Hassan, N. T. Son, E. Janzén, T. Ohshima, D. D. Awschalom, Nature Materials **14**, 160 (2015).
- [4] S. Castelletto, B. C. Johnson, V. Ivdy, N. Stavrias, T. Umeda, A. Gali, T. Ohshima, Nature Materials **13**, 151 (2014).
- [5] S.-i. Sato, T. Narahara, Y. Abe, Y. Hijikata, T. Umeda, T. Ohshima, J. Appl. Phys. **126**, 083105 (2019) 083105-1-10.
- [6] Y. Yamazaki, Y. Chiba, T. Makino, S. -I. Sato, N. Yamada, T. Satoh, Y. Hijikata, K. Kojima, S.-Y. Lee, T. Ohshima, J. Mater. Res. **33**, 3355 (2018).
- [7] <https://www.qst.go.jp/site/taka-english/2498.html>
- [8] T. M. Hoang, H. Ishiwata, Y. Masuyama, Y. Yamazaki, K. Kojima, S.-Y. Lee, T. Ohshima, T. Iwasaki, D. Hisamoto, M. Hatano, Appl. Phys. Lett. **118**, 044001 (2021).

Characteristics and its control of white spot defects on Image Sensor

Nobuhiko SATO\*, Kazuhiro MORIMOTO, Nobuyuki ENDO, Hiroshi YUZURIHARA

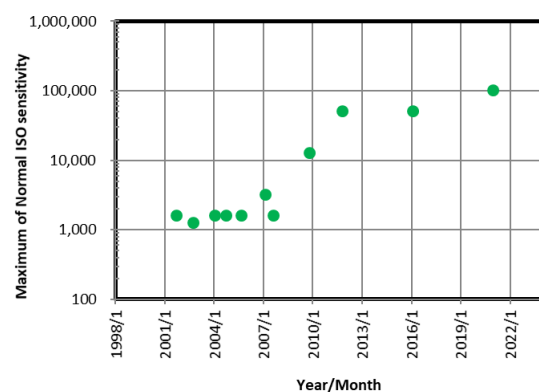
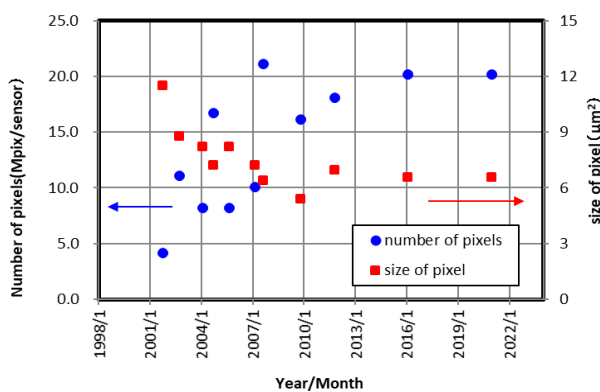
Device Technology Development Headquarters, Canon Inc., 70-1, Yanagi-cho, Saiwai-ku, Kawasaki, kanagawa, 212-8602, Japan

e-mail: sato.nobuhiko@mail.canon

**Abstract**

CMOS image sensors have been used in digital cameras and other applications. Despite the reduction in pixel size as the number of pixels increases, the sensor sensitivity have been improved since the 1990s. In addition to these, Digital Camera has also introduced video performance for higher resolution such as FHD, 4k and 8k standard in recent years. We report on methods for evaluating and reducing dark currents caused by dangling bonds at the SiO<sub>2</sub>-Si interface around photodiodes and fixed pattern noise such as white spot defects caused by metal impurities in photodiodes, which were essential for the evolution of image sensors.

**1. Introduction**



**Fig. 1** Annual changes of number of pixels in a sensor of our professional use cameras

**Fig. 2** Annual changes in maximum of normal ISO sensitivity in a sensor of our professional-use cameras

The development of image sensors using Si substrates led to the practical use of CCD (Charge-coupled-devices) and MOS (Metal-oxide-semi-conductor) type image sensors in the 1980s, and CMOS image sensors using CMOS LSI process in the 1990s. In the 2000s, with the increase in the number of pixels in CCD and CMOS image sensors, the shift from film cameras to digital cameras has progressed. Furthermore, CMOS image sensors has been continue to improve the number of pixels with pixel size shrinkage, sensitivity, and video performance as the mainstream of image sensors for digital cameras, video cameras, and even smartphones.

Figure 1 and 2 shows annual changes in the number of pixels in our commercially available professional model single-lens reflex (SLR) digital cameras and the normal ISO sensitivity. The size of imaging surface with pixels arranged is 24 x 36 mm<sup>2</sup> so-called 35 mm film size, which is equivalent to the film size of conventional single-lens reflex film cameras, or 29 x 19 mm<sup>2</sup> as APS-H size, which is slightly smaller. The 2001 model had 4.15 million pixels and a normal maximum ISO of 1600, while the 2020 model had 20.2 million pixels and a maximum of normal ISO sensitivity of 10,400. In other words, the number of pixels has increased approximately 5 times in

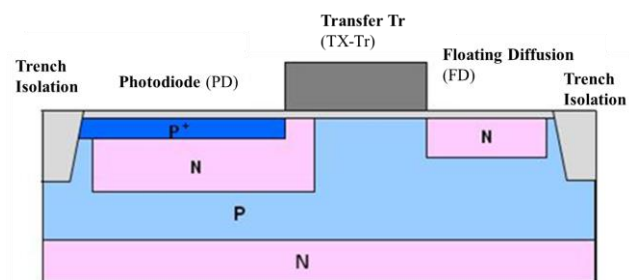
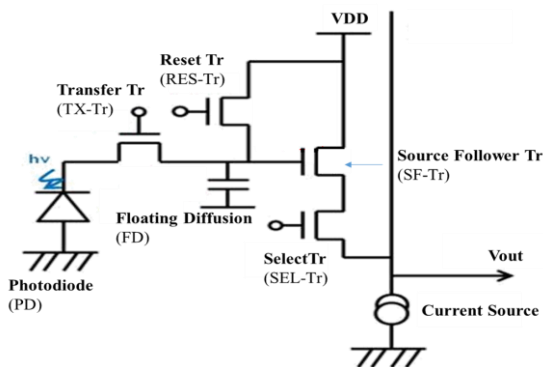
about 20 years, and ISO sensitivity has evolved 5 steps higher, even though the pixel size has shrunk from  $11.5 \times 11.5$  to  $6.5 \times 6.5 \mu\text{m}^2$ , correspond to an area ratio of about 1/3.

Further higher sensitivity as well as higher speed operation has been developed by using single photon avalanche photodiode (SPAD) type image sensor<sup>1</sup> with 3.2 million pixels. The number of photons entering the avalanche photodiode is counted one by one in SPAD type sensors, while the CMOS Image Sensor measures voltage according to the amount of electric charge generated by photoelectric conversion of photons entering the photodiode.

## 2. Noise in CMOS image sensors

To maintain and improve the sensor's sensitivity and dynamic range even when the pixel size is reduced, various improvements have been made in addition to the miniaturization of the process design. An example of a pixel circuit diagram of a CMOS image sensor is shown in Fig. 3. A schematic cross section of the photodiode, transfer transistor (TX-Tr) and floating diffusion (FD) section is shown in Fig. 4.

The operating principle of the CMOS image sensor is briefly explained as follows. First, the charge in the PN photodiode (PD) part formed in Si is discharged through the TX-Tr to floating diffusion (FD) part to deplete the PD. Then light enters the PD, electric charges “q” are generated and electrons are accumulated in the PD according to the amount of light intensity. The FD part, which is an N-type region formed in a silicon P-type well, discharges electric charge by turning on a reset transistor (RES-Tr) connected to a positive voltage, in advance. Then, by turning the TX-Tr on, the charges “q” accumulated in the PD region are transferred to the FD region. Next, the charges transferred to the FD is applied to the gate of the source follower transistor (SF-Tr), when the voltage defined by  $q/C_{fd}$  determined by the transferred charge amount q and the capacitance  $C_{fd}$  of the FD part. In response to this voltage, a voltage  $V_{out}$  corresponding to the amount of charge “q” accumulated in the PD is output through the vertical output line. Therefore, the sensitivity of the CMOS image sensor is mainly governed by the optical efficiency of incident light into the PD part, the efficiency of photoelectric conversion of light incident into the PD, and the FD capacitance  $C_{fd}$  that governs the conversion factor of the charge amount of the SF-Tr to the gate voltage.



**Fig. 3** Example of Pixel Circuit of CMOS image sensor **Fig. 4** Schematic cross-sectional view of a pixel of CMOS image sensor

Noise components in pixels are roughly classified into random noise (RN) and fixed pattern noise (FPN). The former includes dark current components in the PD section and reset noise in the FD section. The dark current in the PD region is mostly due to dangling bonds at the  $\text{SiO}_2$ -Si interface, which is formed between the photodiode and the device isolation region made by  $\text{SiO}_2$  trench structure or the Si surface. Noise suppression is enabled such

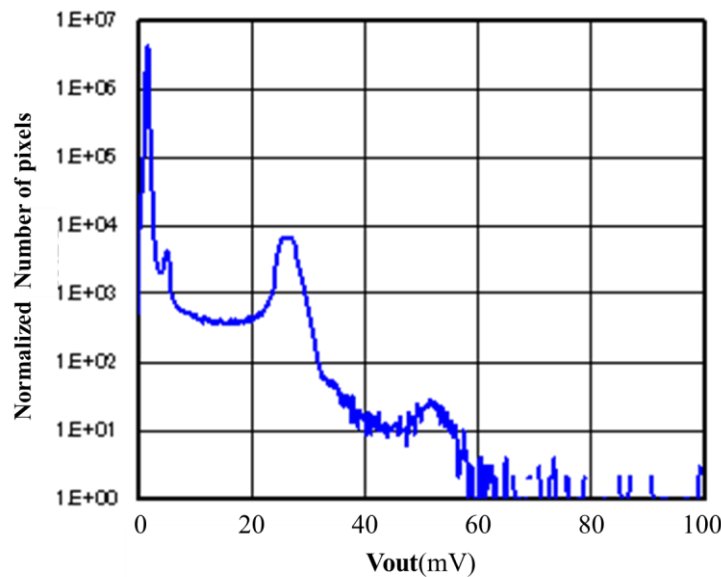
as hydrogen termination of the dangling bonds or the formation of P-type regions near the SiO<sub>2</sub>-Si interface.

The latter FPN occurs only in some pixels where metal impurities, crystal defects and oxygen precipitates exist. FPNs are suppressed below a certain number, and the few remaining FPNs become invisible by image processing in commercially available cameras, videos, and smartphones, so they are hardly a problem for practical use. However, in the process of refining processes and improving ISO sensitivity, it is often a problem to be solved. The reset noise can be suppressed by correlated double sampling processing.

### 3. Noise generation mechanism in photodiode

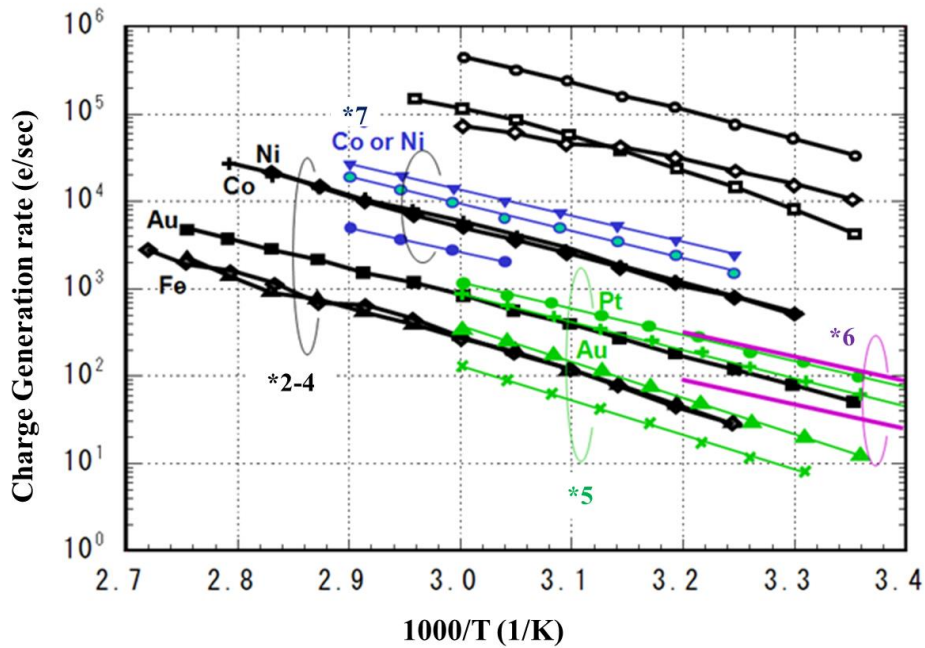
FPN caused by dark current and metal impurities generated in photodiodes is explained. In the PD part of Fig. 4, charges other than that generated by photoelectric conversion become noise. Especially in the N region, which is depleted by applying a reverse voltage, electrons and holes are generated based on the Shockley-Read-Hall (SRH) model if some energy levels exist in the bandgap of silicon. Since holes are ejected through the P-type region, only electrons remain in the photodiode, resulting in an increase of charges in the corresponding pixels even if there is no light incident. The energy levels in the band gap are formed by metal impurities, crystal defects (such as residual defects after ion implantation), and oxygen precipitates. The charge generation rate is determined by the energy level, the impact cross section, and the temperature. The generation rate of some metals is too high to generate hundreds of electrons per second with only one atom in the PD.

A histogram of the amount of charge accumulated in the photodiode section of each pixel when the CMOS image sensor is not illuminated with light (1 second, 60 deg. C) is shown in Fig. 5. The horizontal axis corresponds to the output voltage of the SF-Tr. The peak around 3 mV is the dark current component, and this dispersion component corresponds to the random noise of the pixels. In addition to this, there are pixels with distinctive generated charge amounts around 7, 27 and 54 mV, although they are less frequent than random noise. The peaks, 7 mV and 27 mV are caused by one specific metal impurity in the PD part of each pixel. On the other hand, the number of pixels at 54 mV, which is twice of 27mV, is equivalent to the reciprocal of squared the number of 27 mV peak. This indicates that 27 mV has just one metal atom and 54 mV has 2 atoms in one photodiode respectively<sup>2</sup>.



**Fig. 5** Histogram of voltage output of pixels in the Dark

The identification of metals that generate distinctive peaks of FPD has been reported by several researchers on CCD as shown in Fig. 6, in which Fe, Ni, Co etc. is identified<sup>2-7</sup>.



**Fig.6** Charge Generation rate due to several metals versus temperature in the previous reports<sup>2-7</sup>

#### 4. Sources and detection of metal impurities

The sources of metal impurities in PDs vary from components of manufacturing equipment for CMOS image sensor processes to impurities in gas and chemical solutions. From the beginning of development, we have also taken steps to identify the origin of the process steps and equipment, improve the process, change materials and parts of the equipment, or getter metal impurities.

While the impact of metal impurities becomes more severe as the sensitivity of sensors better, we have reduced the metal impurity levels below a practical level. As a result, the concentrations of these metal impurities are extremely small compared to analytical methods. The sum of the volume of the PD of the pixels of a entire CMOS image sensor is approximately to  $10^{-4}$  cm<sup>3</sup> in the latest model of the professional model digital cameras as mentioned above, and the metal impurity concentration in Si in the PD is equivalent to  $10^6$  atoms/cm<sup>3</sup>, assuming that approximately 200 pixels (10ppm of entire pixels) that produce FPN of a specific output.

The lifetime and diffusion length of charges excited by light irradiation on Si correlate with the density of traps such as metal impurities and dangling bonds in Si. In surface photovoltage (SPV) method, the diffusion length in Si affected by metal impurities or other traps is measured by the surface potential of a Si wafer. We experienced that the origin of the metal impurities is lift pins of process equipment by comparing the map of the diffusion length with FPN patterns of the image sensors. In the  $\mu$ PCD method, the lifetime is measured by time-dependent decay of the reflectance of microwaves due to the electric charge generated in Si by the pulsed light. The lifetime value is the inverse sum of the bulk lifetime in the wafer and that of the wafer surface, so the suppression of the recombination of the wafer surface is essential for high sensitivity for the bulk lifetime in Si. We applied

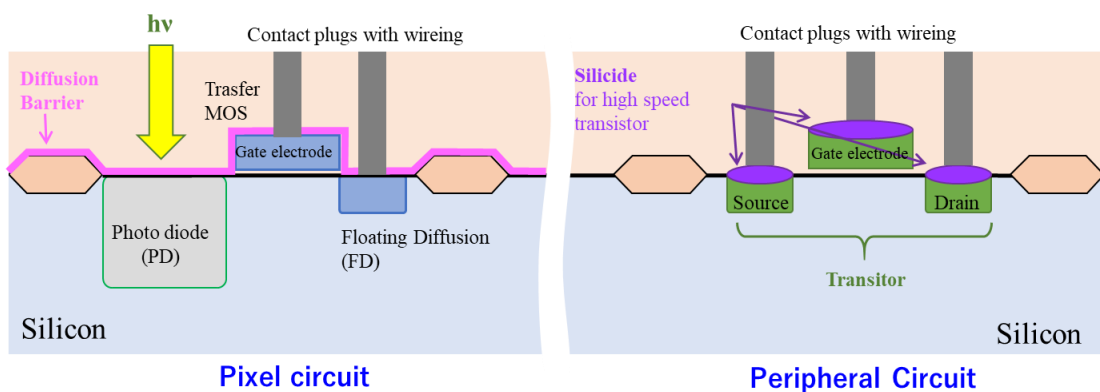


quinhydrone/ethanol solution coating method<sup>8</sup> to the wafer surface to suppress the surface recombination. The measured lifetime correlated with the increase of sensors with higher FPD, but further reduction of metal impurity has been resulted in below the lifetime sensitivity limit.

Measuring methods for metal impurities can be divided into two methods: physicochemical analysis such as inductively coupled plasma mass spectrometry (ICPMS) and total reflection X-ray fluorescence (TXRF) to identify and directly detect metal species, and measurement of the trapping of photoelectrons generated in Si to interband levels caused by metal impurities, defects, etc. as a decrease in lifetime and diffusion length. TXRF is used to measure impurity concentration from the intensity of fluorescence X-rays emitted from metal impurities adhering on the surface of a wafer by irradiating X-rays, and the detection limit is approximately  $10^9$  atoms/cm<sup>2</sup>. In the ICP-MS method, metal impurities on the Si surface is collected by desolving the native oxide film on the Si wafer surface by dropping hydrofluoric acid aqueous solution, and is quantified it by ICP-MS. The amount of metal impurities in surface layer of Si can also be possible by dissolving Si. In both methods, the detection limit has been improved by improving the pre-treatment method.

### 5. High speed operation of peripheral circuits and suppression of metal impurity in pixel Circuits

Increasing the number of pixels in an image sensor to increase the number of frames per second, or to support full-HD, 4k, 8k video format, for example, requires miniaturization of transistors in order to speed up peripheral circuits (driving and readout circuits) around the pixels imaging region. As transistors are getting miniaturized, silicide with metals such as Ni and Co, which have large diffusion coefficients in Si, are used to reduce the resistance of the junction between Si and metal wiring for higher operation. On the other hand, these metals may play as FPN generation center if they diffuse into photodiodes during heat treatment at the manufacturing process. As shown in Fig. 6, metal silicide for higher operation is formed only in the peripheral circuit section at the junction with the metal wiring, while such metal silicide is not formed in the pixel circuit in addition to diffusion barrier layer formed above the photodiode region, because the photodiode pixels does not need such higher operation in comparison with peripheral circuit. Moreover, in the stacked type image sensor, peripheral circuits and pixels are formed on separate Si wafers, respectively. FPN can be more effectively reduced by forming such metal silicide only on the wafer apart from the silicon wafer for the photodiode.



**Fig. 7** Schematics cross section of pixel circuit and peripheral circuit

## 6. Summary

Noise performance, which contributes to the high sensitivity of CMOS image sensors, is greatly affected by metal impurities and dangling bonds at the SiO<sub>2</sub>-Si interface. In addition, the metal silicide that makes up the higher operation of transistors, may also be a source of FPN, so we form the junction of Si with the wiring of the pixels and the peripheral circuits separately. In addition, the development of highly sensitive monitoring methods for metal impurities corresponding to higher sensitivity and lower noise of CMOS image sensors is continuously desired.

## REFERENCES

- [1] K. Morimoto et al. Tech. Dig. Of the IEDM (2021) p. 20,
- [2] W. C. McColgin et al. Tech. Dig. of the IEDM (1992), p.113.
- [3] W. C. McColgin et al. Tech. Dig. of the IEDM (1995), p. 163.
- [4] W. C. McColgin et al. Mat. Res. Soc. Symp. Proc. **510**, 475 (1998).
- [5] I. M. Peters et al. IEEE Int. Workshop on CCD and Adv. Image Sensors (2005), R15.
- [6] R. D. McGrath et al. IEEE Trans. On Electron Devices **ED34**, 2555 (1987).
- [7] H.I. Kwon et al. IEEE Trans. On Electron Devices **51**, 178 (2004).
- [8] H. Takato et al, Jpn, J. Appl. Phys. **41**, L870 (2002).

## Toward Silicon Quantum Computers: Challenges in Devices, Integration, and Circuits

Takahiro Mori<sup>1\*</sup>

<sup>1</sup>*Device Technology Research Institute, National Institute of Advanced Industrial Science and Technology (AIST), Central 2, Umezono 1-1-1, Tsukuba, Ibaraki, 305-8568, Japan*

e-mail: mori-takahiro@aist.go.jp

### Abstract

Silicon quantum computers are attractive because of their capability of large-scale integration thanks to the established fabrication technology for miniaturized transistors. However, toward their practical realization, many challenges remain regarding device, integration, and circuit technologies. This presentation reviews the issues and introduces the recent progress of silicon quantum technology.

### Introduction

LSI technology has continuously supported the progress of computer performance in the current information age. Transistor miniaturization has been the essence of progress. The miniaturization increases the degree of integration per unit area. At the same time, the miniaturization increases the number of transistors we can use under the limited power supply because the miniaturization also realizes the improvement of the transistor's current-voltage characteristics resulting in low power consumption. Today, transistor miniaturization almost reaches its limitation; however, efforts of semiconductor society have realized continuous increment of the number of transistors per unit area, with the development of new technologies such as the scaling of interconnect wiring, area reduction of circuit cells, etc. Also, regarding power consumption, new device technologies have come to continue the trend of low power consumption. These new technologies, such as nanosheet transistors, could further reduce device resistance to realizing high drive current realizing high-speed operation. In addition, circuit-level technology to reduce power consumption has been a kind of common one. Thus, there is no doubt that the transistor and its integrated circuit technologies continue to be the driving force for the progress of computer performance.

However, it is evident that the speed of the progress has slowed down with approaching the miniaturization limit. Then, in recent years, there has been a demand to seek a new driving force. The non-Neumann computation technologies are promising candidates, and the neural network computation technology is the most successful example. Among these, quantum computing technology has been quite attractive and promising for the future. These kinds of new computation technologies cannot replace the role of central processing units (CPUs), which realizes general-purpose computation. They play the role of so-called accelerators providing high computation performance for specific problems. Quantum computers are also the case. The most promising applications of quantum computers are combinatorial optimization problems, which are with social significance in many cases, and quantum chemical calculation, which accounts for much of modern supercomputer usage.

Today, quantum computers have been realized. We can use quantum computers, whose hardware is mostly superconductor-based or ion-trap-based, via the internet with cloud-enabled environments. However, it is certain that their performance is not satisfactory. This is because the number of qubits we can use with the ongoing

quantum computers is insufficient. Quantum computers are classified into two types: quantum annealing machines with several thousand qubits [1] and universal quantum computers with around a hundred qubits [2]. In both cases, toward realizing their full potential, we must succeed the integration of a large number of qubits, close to million qubits. Therefore, the integration technology for quantum computers is now on focus.

Silicon quantum computers are attractive from this point of view. Needless to say, silicon technology cultivated in LSI technology can achieve large-scale integration of small devices. Recently, companies that have supported the semiconductor industry, such as Intel and Global Foundries, have participated in quantum technology research and development. For example, Intel has demonstrated the operation of their silicon qubits fabricated in their mass-production-ready fabrication line using 300mm-scale wafers [3]. Also, the top conferences regarding semiconductor integrated devices and circuits (IEDM, VLSI, and ISSCC, for example) have included at least one session on quantum computing technologies, indicating the growing-up activity in research and development of quantum integration technologies.

This presentation aims to summarize the issues toward large-scale integration of silicon qubits and introduce recent significant research results.

## **Silicon Qubits**

Silicon qubits, as a building block for quantum computers, are classified into two types according to quantum information carriers: they are charge qubits and spin qubits. Many researchers consider spin qubits to be the most promising because of their longer spin coherence time which corresponds to the retention time of quantum information. So then, this presentation also deals with spin qubits.

Now I will briefly describe the operation of silicon spin qubits. First, a single electron system is prepared in the quantum dot, taking advantage of the Coulomb blockade phenomenon. This can be thought of as similar to a single-electron transistor. Then, by applying an external static magnetic field, Zeeman splitting occurs, providing an energy difference between the up and down spin states. This forms a quantum two-level system corresponding to the  $|0\rangle$  and  $|1\rangle$  states of quantum information. Finally, microwave signals manipulate the spin states. The input of the microwave signal having an energy equivalent to the Zeeman splitting energy causes Rabi resonance with the spin, resulting in spin rotation. This spin manipulation corresponds to a one-qubit logical operation. Spin manipulation is a kind of electron-spin resonance; therefore, the magnetic component plays an essential role in the manipulation. Electric signals are much more convenient from the integration viewpoint; however, this requires a mechanism to convert the electric to spin signals. Spin-orbit interaction, inherent in host materials, can be the conversion mechanism; unfortunately, its conversion efficiency is relatively low in silicon. Then, a method to realize the pseudo-ESR situation has been proposed taking advantage of the slanting magnetic field caused by micromagnets placed near the qubits and commonly used today [4, 5]. After finishing the spin operation, we have to read out the results. The readout by a current is the simplest method; however, since the spin operation is a single-electron phenomenon, we must proceed with the same operation many times to obtain sufficient current for detection. Then, a technique called single-shot readout has been generally used, by which a single charge can be detected. The simplest one is with a charge sensor as an amplifier. In addition, a two-qubit logical operation must be realized, requiring two interacting quantum dots. This means that the quantum dots, which are to be qubits, must be coupled with neighboring dots. It would be ideal if there were a method to make them interact at a controllable and reasonable distance; however, unfortunately, the interaction has only been possible at short

distances less than 100 nm with Heisenberg-type exchange interaction or at long distances on the scale of 1 mm with the link by superconducting devices [6]. Considering the integration, we must choose the short distance. This fact causes that the qubits must be placed in large numbers at very close distances, which could realize the interaction.

As described above, silicon quantum technology requires integrating both qubit devices and other components such as micromagnets and charge sensors. Therefore, the silicon quantum integration technology would be much more complicated than the modern technology for logic LSIs, where the integration of transistors should only be considered. This perspective can also help us understand the importance of integration technology development.

### **Challenges in Devices**

Silicon qubit research has mainly utilized so-called gate-defined-type qubits in history, producing most of the top-level experimental data [7]. This kind of device has a simple structure: just gate electrodes are on the wafer. In this device, gate voltage manipulation controls depletion regions in the semiconductor layer, produces microscopic areas to confine carriers, and realizes quantum dot formation. The gate-defined qubits exhibit the advantage of minimum process damage induced because of the minimum processing procedure; however, they require a lot of electrodes, which complicates interconnect wiring from the integration viewpoint. Therefore, following the standard silicon device structure, the qubit structure with device isolation has also been proposed. There have long been device structures so-called the physically defined type, in which the number of electrodes is minimized, and the curvilinear qubit isolation pattern defines the quantum dot region [8]. However, in recent years, devices that employ a linear isolation structure combined with gate-controlled channel depletion have been used in many experimental reports. A typical example is the finFET-like qubits fabricated by Intel [3], and we can find other examples employing SOI-FET-like qubits [9]. Since such devices are fabricated with a complicated fabrication process, some researchers have doubted their performance due to process damage. However, the devices fabricated by Intel exhibit comparable performance to that achieved by gate-defined qubits [3], demonstrating that advanced semiconductor processes can also produce qubit performance sufficiently. On the other hand, the cause-and-effect between the process damage and qubit performance has not been tackled yet. I believe this issue could be one of the crucial issues regarding the further progress of the physics of qubit devices.

It is speculated that process damage causes the degradation of the spin coherence time. In the early decade of silicon qubit research, the coherence time was limited by the magnetic noise originating from nuclear spins in the silicon host. Indeed,  $^{29}\text{Si}$  isotopes have nuclear spins. The isotope condensation technique helps this situation. We can reduce the nuclear spins by using a  $^{28}\text{Si}$ -enriched host, suppressing the magnetic noise, and resulting in a longer coherence time [10]. So now, the electric noise limits the coherence time [ref]. According to the knowledge about transistors, it is supposed that some defects cause electric noise. Although the electric noise source has not been clarified so far, the experiment by Oka et al. implies that [11]. They revealed that the origin of the electric noise in MOS structures at cryogenic temperature is due to interface defects. First, they controlled the interface trap density between the  $\text{SiO}_2$  insulator and silicon by changing the silicon surface orientation. Then, they investigated the relationship between the noise level and interface trap density, which indicates the noise level increase with the interface trap density increase. It is noted that this relationship was not observed at room temperature. Therefore, we can imply that the interface trap regulates the coherence time. The research regarding

the interface probably pioneers the investigation of the relationship between the fabrication process and the qubit performance.

### **Challenges in Integration**

Integration is the process of mounting many necessary parts in a limited area. The greatest challenge is regarding the variation of characteristics of the parts. In the case of transistors, the threshold voltage variation is the most critical issue. The variation of the gate metal workfunction is the main component of the variability of current-voltage characteristics in the state-of-the-art transistors. It is easy to speculate that the silicon qubits, which operate based on single-electron phenomena, could exhibit more significant variability. The variability issue is also important in superconducting qubits, although their device size is larger. For example, the flux qubits used in the D-wave quantum annealing machine equip a function to adjust their characteristic variation individually [12]. The operation of many flux qubits has been realized by taking advantage of this function. Considering the same way in silicon qubits, we have to adjust their threshold voltage individually, which is extremely difficult. Therefore, I believe silicon's way is different from that. Following the conventional transistor technology, we should go the way to suppress the characteristic variation by developing device and process technologies able to suppress the variation.

There are a few reports regarding the variability issue on silicon qubits, and AIST of Japan is the first to tackle this issue. They have developed a device simulation technique for semiconductor qubits [13] and utilized it to investigate the fidelity variation caused by the size variation in the device structure. They reported the case of two-element integration of the qubits and micromagnets for a one-qubit logical operation [14] and the case of the interaction between the qubits for a two-qubit logical operation [15]. Indeed, the speculation is true; the fidelity variation of the qubits is huge. In both cases, the qubits assumed here employed the finFET-like structure. Then, the results exhibited that a slight fin-width variation (line-width variation, LWR) even at 1 nm results in a significant fidelity variation, by which not all qubits cannot achieve 99 % fidelity that must be realized toward fault-tolerant quantum computing. According to this result, they have also proposed new integration structures that can achieve acceptable fidelity variation. The variability issue is essential for large-scale integration; therefore, we will see more examples regarding this issue in the future.

Here, I would point out the importance of device simulation technology. The experimental approach is also important in tackling variability issues. However, this requires a fabrication line with certain process stability and measurement instruments capable of continuously measuring many devices. Regarding the qubits, there is a bottleneck on the measurement side. Now instruments realizing continuous measurement of many devices are a few and expensive. Recently, automated cryogenic measurement instruments capable of using 300 mm wafers have been launched; however, we can see only four installation cases [16]. Nevertheless, it is possible to experimentally evaluate variations in current-voltage characteristics by taking advantage of such instruments [17]. However, there are no cases so far to evaluate the qubit variation. The difficulty is that an external static magnetic field and microwaves are required for the qubit characterization, which is not needed for conventional transistor characterization. Due to this situation, device simulation technology becomes highly important. The development of quantum device simulation technology has started in these few years, and we can find three successful examples [13, 18, 19]. The simulation technology should be validated by comparing the simulation results to the experimental, which are still on the way. However, considering the current status of the limited experimental

situation about silicon qubits, it would be very meaningful to proceed with integration technology development using such a computational approach in combination with the experimental.

### **Challenges in Circuits**

Finally, I would like to change the topic from qubit-related to control circuits. As for conventional computers, a CPU plays a central role in the operation. CPUs comprise control units instructing calculation based on the program code and arithmetic logic units executing addition, multiplication, etc. Those units are fabricated as integrated circuits of transistors and are on the same chip; therefore, device or process engineers are rarely aware of the difference in manufacturing. However, quantum computers are different. Because qubits in charge of calculation are unique devices, their controller has to be ready separately. The current quantum computers equip their control unit comprising electric test/measurement instruments such as microwave generators and IQ mixers, and a computer to control these instruments. This is now the so-called brute-force method. This method will fail when the number of integrated qubits increases in the future; thus, a new direction arises: the integrated circuits for the qubit control function. In addition, it is desired that such integrated circuits operate at cryogenic temperature, namely inside refrigerators, for superconducting and silicon quantum computers. The integrated device and circuit technology for cryogenic operation are called cryo-CMOS technology. It should be noted that it is possible to integrate both qubits and control circuits on one chip regarding silicon if their process integration is realized. The required functions for silicon spin qubit control are microwave signal generation for spin manipulation and readout function for calculation results; these are a kind of analog circuit. A famous example has been presented by Intel [20]. Furthermore, the benefit of the one-chip integration has been demonstrated for readout circuits by AIST [21].

Indeed, transistor operation at cryogenic temperatures is quite different from that at room temperature. Therefore, a compact model has been proposed for cryo-CMOS [22]. According to this research, basic device behaviors such as threshold voltage, subthreshold slope, and on-current are different from the ones at room temperature, and the limitation of existing models for room temperature operation has been pointed out. Now the investigation regarding the device behaviors is ongoing; researchers have individually tackled carrier mobility [23], subthreshold slope [24], drain-induced barrier lowering [25], and so on, and also investigated advanced issues such as noise [11] or variability [26]. Unfortunately, reports related to compact models are not so many. Therefore, I believe that scientific discussion related to compact models is insufficient, particularly the limitation of existing models should be discussed in detail.

Power consumption is a crucial issue when considering the goal of cryo-CMOS control circuits. We cannot allow heat generation from the circuits exceeding the cooling power of refrigerators because of cryogenic operation. We are supposed not to achieve sufficiently low power consumption for control circuits capable of one-million-class qubits control if the technology does not progress much more. I believe the progress of transistor technology would help this situation. In short, many issues remain to be solved toward the realization of cryo-CMOS control circuits, both in terms of devices and circuits.

### **Summary**

In this presentation, I have reviewed the challenges toward large-scale integrated silicon quantum computers from three perspectives: device, integration, and circuits. The efforts of many researchers in various fields promise

providing the solutions to realize practical silicon quantum computers.

## Acknowledgments

This research is supported by MEXT, Japan, Quantum Leap Flagship Program (Q-LEAP) JPMXS0118069228.

## REFERENCES

- [1] <https://www.dwavesys.com/company/newsroom/press-release/d-wave-demonstrates-large-scale-coherent-quantum-annealing/>
- [2] <https://newsroom.ibm.com/2021-11-16-IBM-Unveils-Breakthrough-127-Qubit-Quantum-Processor>
- [3] A.M.J. Zwerver et al., *Nat. Electronics* **5**, 184 (2022).
- [4] Y. Tokura, W. G. van der Wiel, T. Obata, and S. Tarucha, *Phys. Rev. Lett.* **96**, 047202 (2006).
- [5] E. Kawakami et al., *Nat. Nanotechnol.* **9**, 666 (2014).
- [6] X. Mi et al., *Nature* **555**, 593 (2018).
- [7] for example, S.G.J. Philips et al., *Nature* **609**, 919 (2022), K. Takeda et al., *Nat. Nanotechnol.* **19**, 965 (2021).
- [8] for example, R. Mizokuchi, S. Oda, and T. Kodera, *Appl. Phys. Lett.* **114**, 073104 (2019).
- [9] R. Maurand et al., *Nat. Communications* **7**, 13575 (2016).
- [10] E. Abe et al., *Phys. Rev. B* **82**, 121201 (2010).
- [11] H. Oka, T. Matsukawa, K. Kato, S. Iizuka, W. Mizubayashi, K. Endo, T. Yasuda, and T. Mori, 2020 Symp. VLSI. Technol. Dig. Tech. Papers, TN2.2.
- [12] R. Harris et al., *Phys. Rev. B* **81**, 134510 (2010).
- [13] H. Asai, S. Iizuka, T. Ikegami, J. Hattori, K. Fukuda, H. Oka, K. Kato, H. Ota, and T. Mori, 2021 Electron Devices Technology and Manufacturing Conference (EDTM) Dig. Tech. Papers, pp.1-3.
- [14] S. Iizuka, K. Kato, A. Yagishita, H. Asai, T. Ueda, H. Oka, J. Hattori, T. Ikegami, K. Fukuda, and T. Mori, 2021 Symp. VLSI. Technol. Dig. Tech. Papers, JFS5-5.
- [15] H. Asai, S. Iizuka, T. Mogami, J. Hattori, K. Fukuda, T. Ikegami, K. Kato, H. Oka, and T. Mori, Ext. Abstr. 2022 Int. Conf. on Solid State Devices and Materials, pp. 503-504.
- [16] Intel, CEA-Leti, AIST, and Northrop Grumman.
- [17] O. Zietz et al., Ext. Abstr. 2022 Int. Conf. on Solid State Devices and Materials, pp. 509-510.
- [18] F. A. Mohiyaddin et al., 2019 Int. Electron Devices Meeting Dig. Tech. Papers, pp. 959-962.
- [19] <https://nanoacademic.com/qtcad-has-launched/>
- [20] J.-S. Park et al., 2021 Int. Solid-State Circuits Conference Dig. Tech. Papers, pp. 208-210.
- [21] H. Fuketa, I. Akita, T. Ishikawa, H. Koike, and T. Mori, 2022 Symp. VLSI. Technol. & Circuits Dig. Tech. Papers, pp. 234-235.
- [22] A. Beckers, F. Jazaeri, and C. Enz, *IEEE Trans. Electron Devices* **65**, 3617 (2018).
- [23] H. Oka, T. Inaba, S. Iizuka, H. Asai, K. Kato, and T. Mori, 2022 Symp. VLSI. Technol. & Circuits Dig. Tech. Papers, pp. 334-335.
- [24] M.-S. Kang, K. Toprasertpong, M. Takenaka, H. Oka, T. Mori, and S. Takagi, *Jpn. J. Appl. Phys.* **61**, SC1032 (2022).
- [25] T. Inaba, H. Asai, J. Hattori, K. Fukuda, H. Oka, and T. Mori, *Appl. Phys. Express* **15**, 084004 (2022).
- [26] T. Mizutani, K. Takeuchi, T. Saraya, H. Oka, T. Mori, M. Kobayashi, and T. Hiramoto, *Jpn. J. Appl. Phys.* **61**, SC1006 (2022).



**November 8 (Tuesday)**

# **Session G**

Chair: *S. Nishizawa (Kyushu Univ.)*

**13:00 ~ 14:00**

(Noh Theater Hall “Tenjin9”)

## Silicon wafer cleaning technology

Yuji.Nagashima\*<sup>1</sup>, Yuichi Imaoka<sup>1</sup>, Masafumi Suzuki<sup>1</sup>, Yotaro Fukuoka<sup>1</sup>, Katsuhiro Yamazaki<sup>1</sup>

<sup>1</sup>Shibaura Mechatronics Corporation, 2-5-1, Kasama, Sakae-ku, Yokohama, Kanagawa, Pref. 247-8560, Japan

E-mail: yuji.nagashima@shibaura.co.jp Phone: +81-45-897-2668 Fax+81-45-897-2664

### Abstract

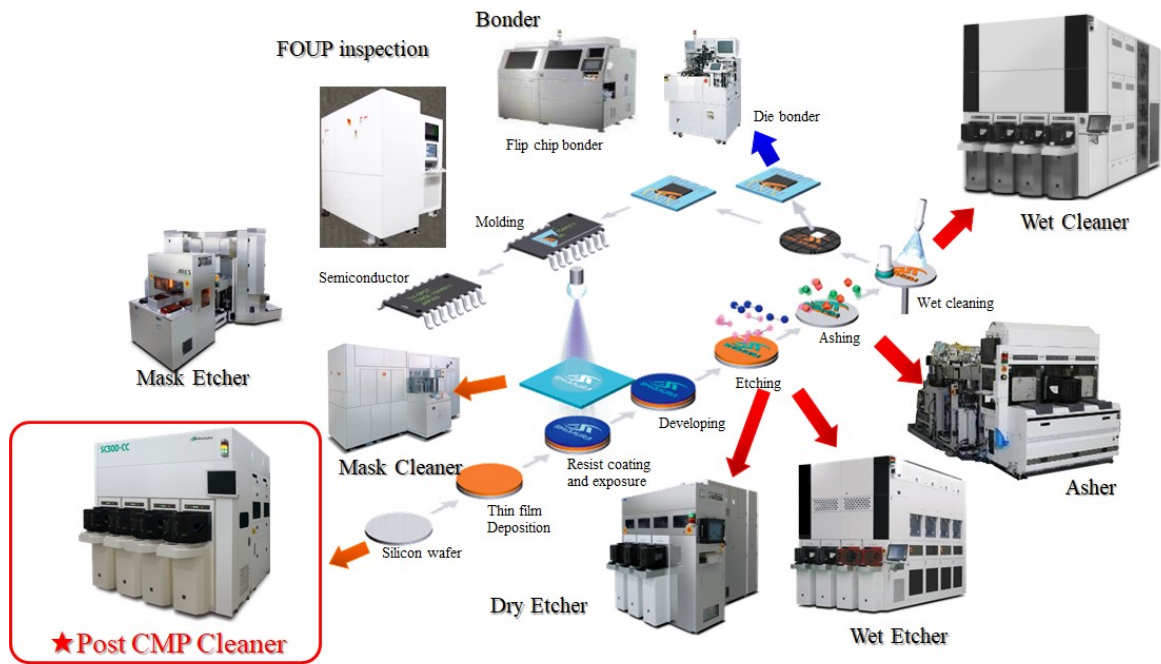
We will introduce our company's main equipment lineup, and explain the cleaning technology and cleaning flow of the single-wafer-type silicon wafer cleaning equipment. We will also report the latest particle performance evaluation results with a particle size of 19nmUP for the performance evaluation of a single-wafer-type post-polishing cleaning system that uses wafers that were polished by a chemical mechanical polisher. In recent years, in wafer cleaning, it has become important to optimize not only the cleaning conditions in the cleaning equipment but also the conditions in the chemical mechanical polisher (e.g., polishing conditions, slurry conditions).

### 1. Introduction

Silicon wafers are the basic material of semiconductors, and semiconductors are used in all electronics-related products, including computers, communication equipment, and home appliances. A global increase in demand for semiconductors has resulted in the increased demand for silicon wafers, which are the basic material for semiconductors. Furthermore, there are stricter requirements for the particle performance of the basic material that is the silicon wafer due to the miniaturization of semiconductor devices in recent years. In this regard, further improvements in particle performance are needed to our single-wafer-type silicon wafer cleaning equipment in order to meet this increasing demand [1].

### 2. Main equipment lineup

Fig. 1 shows our company's lineup of semiconductor manufacturing equipment. Our company manufactures and sells not only the single-wafer-type cleaning equipment introduced in this report but also Dry etching equipment, Wet etching equipment, Asher equipment, Bonder equipment, Cassette inspection equipment, Mask etching equipment, and Mask cleaning equipment.



**Fig. 1: Shibaura Mechatronics semiconductor manufacturing equipment lineup**

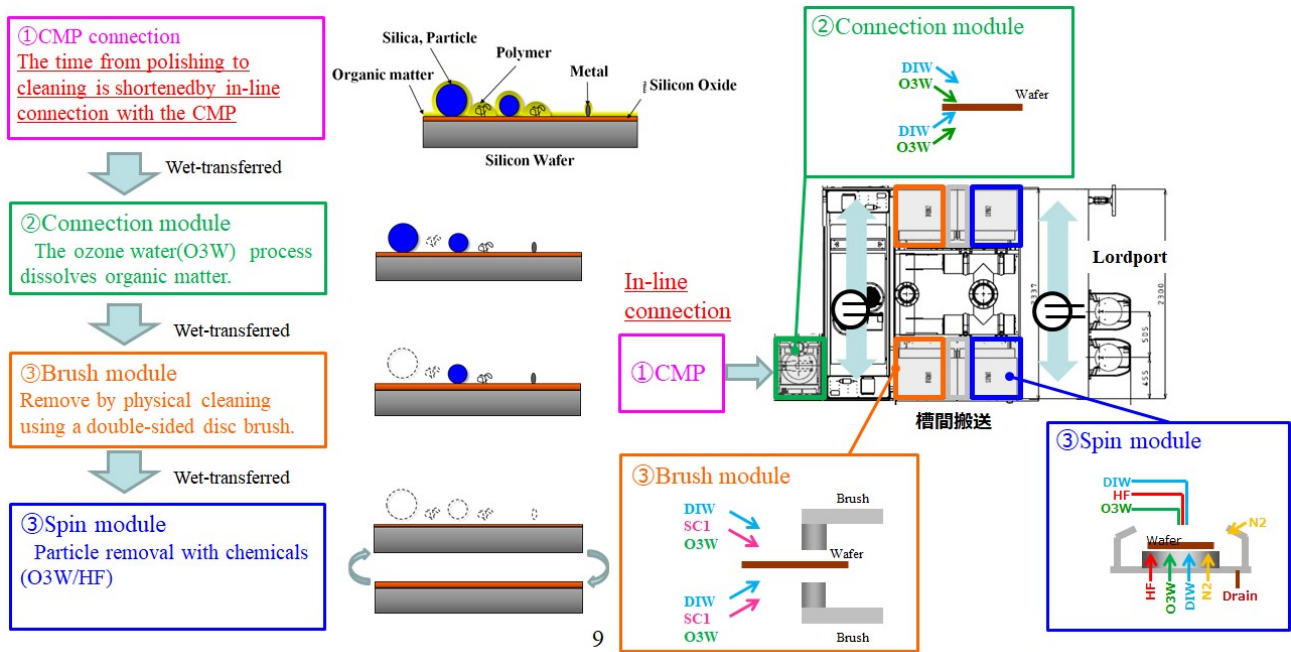
### 3. Shibaura Mechatronics post-polishing cleaning technology

We will focus on the single-wafer-type post-polishing cleaning equipment among the silicon wafer cleaning equipment in this introduction. Our company's post-polishing cleaning equipment adopts a single-wafer-type system instead of a batch-type system for the following reasons.

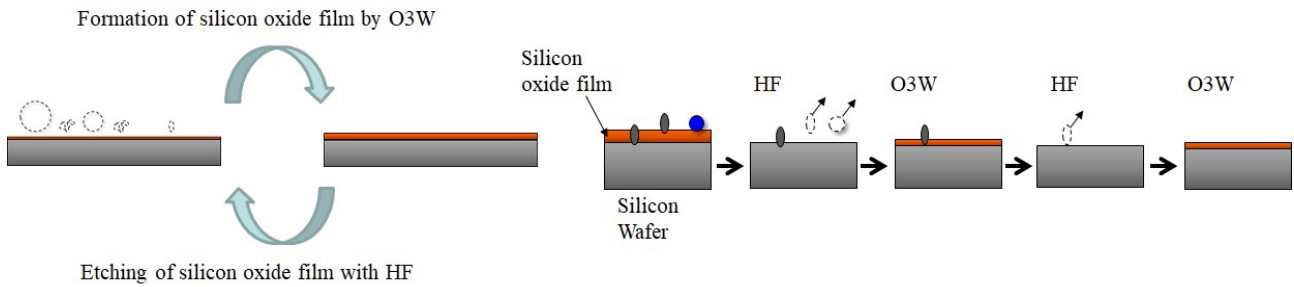
- The single-wafer-type system processes wafers one by one, so it is capable of processing without cross-contamination.
- The batch-type system is easily affected by particles contained in the liquid when it is pulled out of the processing tank during drying, but the single-wafer-type system can suppress the effect of particles by drying at high rotations with spin drying.
- The single-wafer-type system allows for continuous changing of the processing solution and easy control of the oxide film thickness and etching amount, so processing can be conducted with high accuracy.

Fig. 2 shows the cleaning flow and functions of our company's post-polishing cleaning equipment.

- ①Chemical mechanical polisher (henceforth referred to as CMP) connection: the time from polishing to cleaning is shortened by in-line connection with the CMP.
- ②Connection module: Wafers that were wet-transferred from the CMP are quickly treated with ozone water (henceforth referred to as O3W) in order to decompose organic substances and form an oxide film in order to make them hydrophilic, thereby increasing the cleaning effect of chemicals.
- ③Brush module: Wafers that were wet-transferred from the connection module are removed by physical cleaning using a double-sided disc brush.
- ④Spin module: Clean wafers that were wet-transferred from the brush module by repeated HF and O3W processing.



**Fig. 2 Wafer cleaning flow and its functions**



**Fig. 3 Image of O3W/HF processing**

Fig. 3 shows an image of the O3W/HF processing. First, HF is used to remove the fine particles, organic matter, etc., that remain on the O3W oxidized wafer surface and metal contaminants, etc., that are present in the oxide film. Next, after an oxide film is formed with O3W, repeated oxide film etching with HF and oxide film formation with O3W is conducted so that the wafer can have a cleaner surface condition.

In the oxidation by O3W, it is possible to form a uniform oxide film by oxidizing the outer periphery of the wafer in a short period of time by conducting alternate delivery from the center nozzle and edge nozzle, which is a unique cleaning technology from our company (Fig. 4). We name this nozzle the Chopped Shot(CS) nozzle. The oxide film thickness and its uniformity at this point can be controlled by changing the liquid delivery time from CS nozzle.

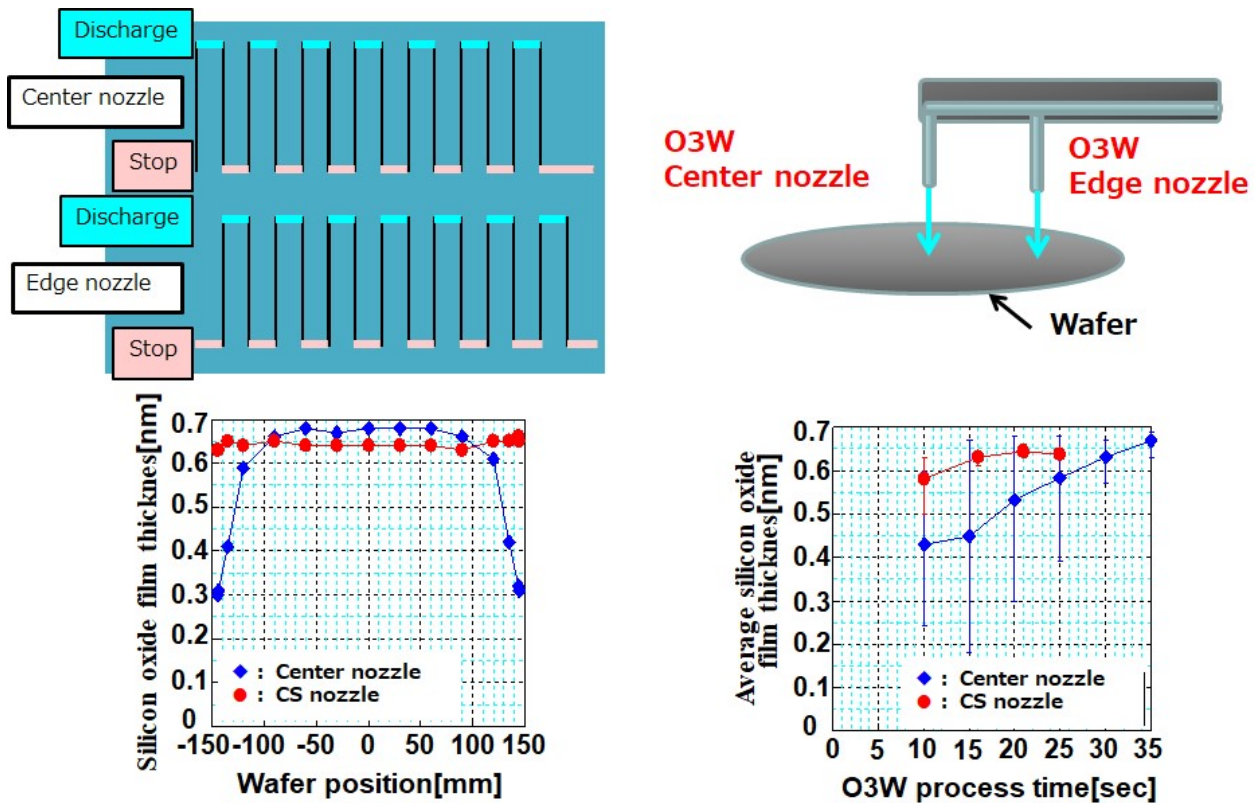


Fig. 4 Silicon oxide film thickness by O3W center or CS nozzle

#### 4. Post-polishing cleaning particle performance results

Conventional particle performance evaluation for post-polishing cleaning was conducted using silicon wafers that were forcibly contaminated by sprinkling microparticles. However, this evaluation method often does not reproduce the cleaning results of actual silicon wafer manufacturers. Therefore, in the present post-polishing cleaning evaluation, we conducted particle performance evaluation in in-line connections using wafers that were polished by a CMP (slurry used: manufactured by GLANZOX/Fujimi Incorporated, CMP used: PNX 332B/manufactured by Okamoto Machine Tool Works Ltd.). Fig. 5 shows the results of post-cleaning particles that were processed under conventional post-polishing cleaning condition. We were able to confirm that the performance of an average of 50 particles or less (19nmUP), which is the particle specification for conventional advanced silicon wafers, was satisfied. However, in actual in-line cleaning of wafers after polishing, it was found that many particles were distributed around the outer periphery of the wafer. It was confirmed from the particle component analysis of this outer periphery that it was SiO-based, and it was found that the residual slurry had an effect.

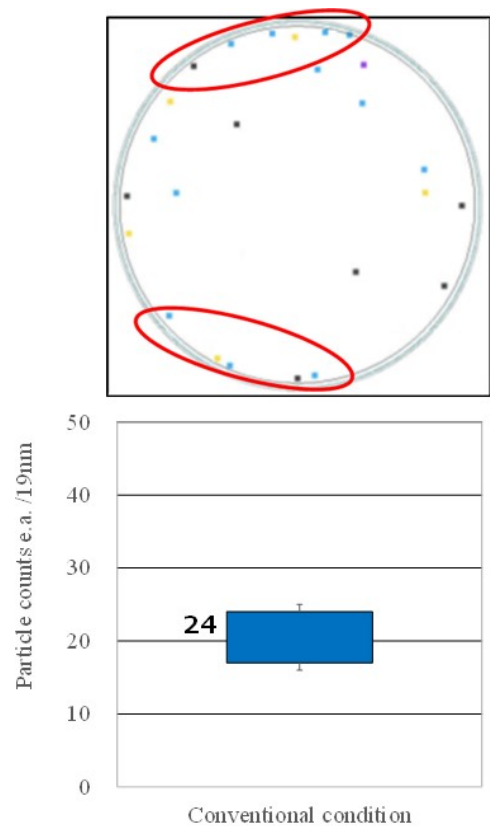
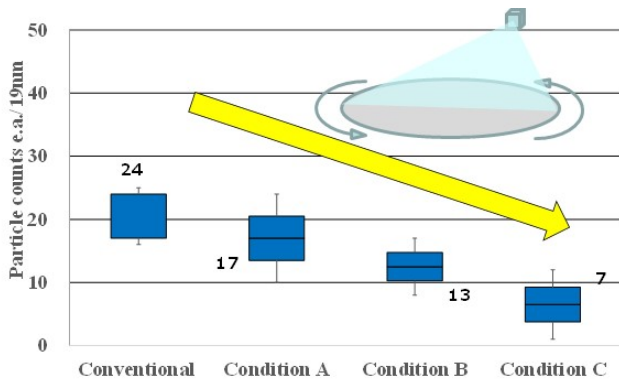


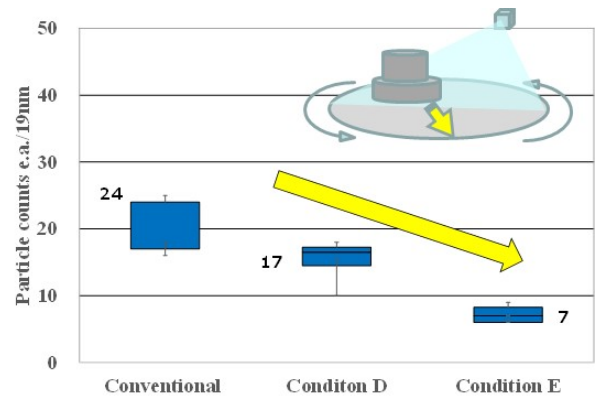
Fig. 5 Cleaning results under conventional condition

We evaluated the improvement of the cleaning conditions in the brush module, which mainly removes the residual slurry, in order to improve the removability of the residual slurry. Figs. 6 and 7 show the evaluation results for the wafer rotation speed and brush rotation speed as parameters that affect the improvement of the particle removability of the outer periphery of the wafer.

It was shown in each evaluation that the particles were improved after cleaning and that the improvement of the discharge performance due to the rotation speed of the wafer and improvement of the sweeping performance due to the rotation speed of the brush were effective for cleaning the wafer after polishing.

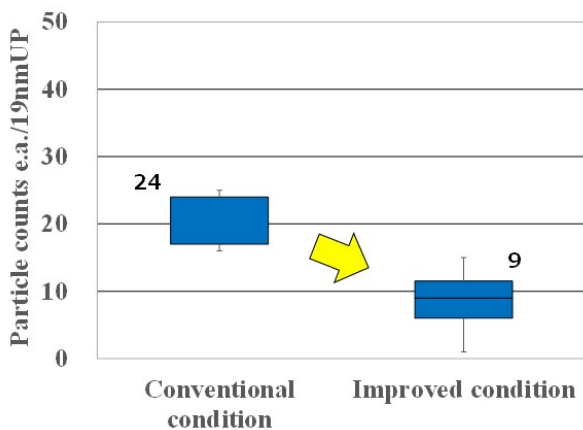


**Fig. 6 Cleaning results under improved wafer rotation speed**

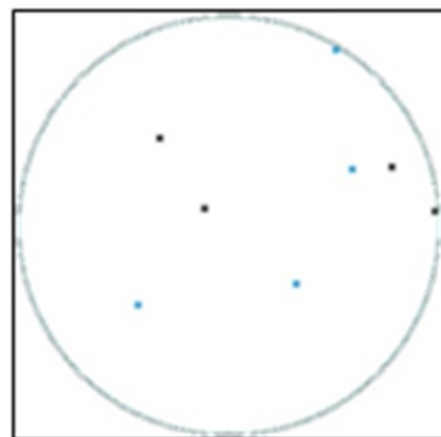


**Fig. 7 Cleaning results under improved brush rotation speed**

Figs. 8 and 9 show the results of evaluation under optimal conditions that combine parameters that show effects under each cleaning condition. The number of particles on the entire surface of the wafer was reduced along with the number of particles on the outer periphery, which was seen under the conventional conditions, and results showed an improvement to an average of 10 particles or less (19nmUP) in terms of particle performance.



**Fig. 8 Cleaning results under the improved condition**

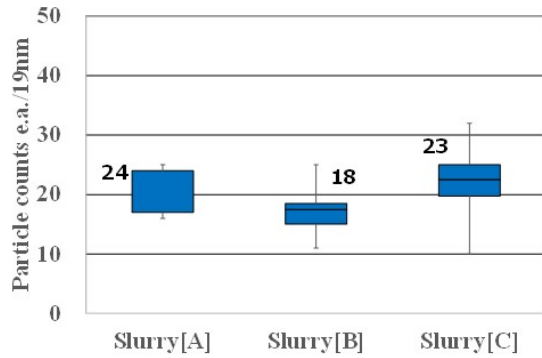


**Fig. 9 Particle map under the improved condition**

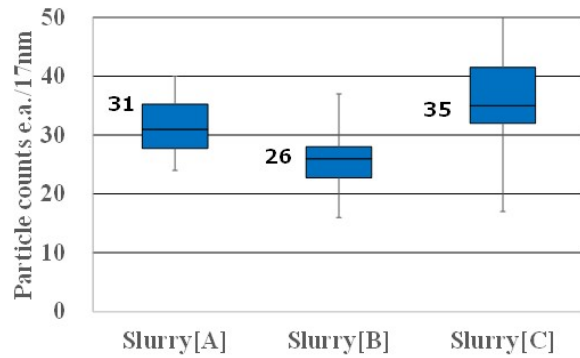
The particles after the cleaning of the post-polishing wafer are thought to be affected by slurry conditions such as the polishing conditions of the CMP and the slurry type. Therefore, Fig. 10 shows the evaluation results of using different types of slurries under the same polishing conditions. There was a difference in the number of particles

after cleaning depending on the type of slurry.

Fig. 11 shows the result of measuring the results in Fig. 10 with an even smaller 17nmUP. There was a tendency for the variation at 17nmUP to increase, and the difference was confirmed. It will be necessary to optimize the cleaning conditions according to the type of slurry, etc., to conduct cleaning that corresponds to the particle sizes that will become even smaller in the future.



**Fig. 10** Cleaning results with different slurry types (19nm)



**Fig. 11** Cleaning results with different slurry types (17nm)

## 5. Conclusion

We introduced cleaning flow and cleaning technologies, with a focus on our company's post-polishing cleaning equipment. It was shown from the evaluation of cleaning performance using post-polishing wafers that it has become important to optimize cleaning conditions, including polishing conditions and slurry conditions, for wafer cleaning in the future.

## References

[1] Y.Imaoka et al. The Committee No. 145 for Crystal Processing and Evaluation Technology, The175th Seminar Materials (2021).

**November 7 (Monday)**

# **Session P**

**“Poster Session”**

Chair: *S. Nishizawa (Kyushu Univ.)*

**17:20 ~ 19:50**

(Robby)



## Theoretical Study on Binding of Vacancy–Oxygen Complex ( $VO_x$ ) to Metals in RTP Wafers

Hiroya Iwashiro<sup>1\*</sup>, Haruo Sudo<sup>1</sup>, Ken Hayakawa<sup>1</sup>, and Eiji Kamiyama<sup>1</sup>

<sup>1</sup> *GlobalWafers Japan Co., Ltd., 6-861-5, Seiro-machi Higashiko, Kitakanbara-gun, Niigata 957-0197, Japan*

\*Hiroya\_Iwashiro@sas-globalwafers.co.jp

### Abstract

The objective of this study was to investigate the possibility of vacancy-oxygen complexes ( $VO_4$ ), which are presumed to be generated in the rapid thermal process (RTP) wafers, exhibiting a gettering effect on typical metal impurities (Al, Fe, Cu, and Ni) in semiconductor manufacturing. The binding energy ( $E_b$ ) was obtained using the first-principles calculation. The calculated  $E_b$  of metastable  $VO_4$  and metals ranged between 0.9 and 1.4 eV, which is higher than that of Fe-B (0.65 eV). These values are close to  $E_b$  of  $VO$  (1.1–1.9 eV), whose gettering effect has been confirmed experimentally, indicating the possibility of  $VO_4$  gettering in RTP wafers.

### 1. Introduction

The rapid thermal process (RTP) induces bulk micro defect (BMD) formation by generating a high concentration of vacancies ( $V_s$ ) in Si wafers [1]. Vacancy–oxygen complexes ( $VO_x$ ) are formed when the RTP-generated vacancy ( $V$ ) binds with the oxygen (O) in Si wafers, thereby contributing to the nucleation of BMDs. Experimental results have reported that  $VO$  generated by electron beam irradiation exhibits a gettering effect on metal impurities [2–4], and the same can be expected in the RTP wafers.

The direct observation of the form of  $VO_x$  is difficult. Based on the theoretical calculations,  $VO_2$  is presumed to be dominant during the crystal growth [5], and can be considered as a dominant form in RTP wafers as well. However, an analysis of the RTP wafer conducted using Fourier transform infrared spectroscopy (FTIR) revealed a trace amount of  $VO_4$  as a residual  $V$  morphology [6,7]. This confirmed that  $V$  generated by RTP attained stability by binding to four O atoms. In addition, previous experiments confirmed that the BMD density after RTP is proportional to the fourth power of the estimated  $V$  concentration [8]. This result suggests that  $4VO_4$  may be a constituent unit of BMD nuclei in RTP wafers. Furthermore, the theoretical calculations reported high binding energy ( $E_b$ ) of  $VO$  with metal atoms (metals) [9]; however, the calculations of  $E_b$  for  $VO_4$  and  $4VO_4$  with metals have not been reported so far. Obtaining  $E_b$  of  $VO_4$  and  $4VO_4$  with metals is important for elucidating the gettering performance of BMD nuclei. Therefore, in this theoretical study, we considered  $VO_4$ , which is a simple structure. First-principles calculations were applied to: (1) obtain the  $E_b$  of  $V$  and O, (2) explore the possibility of a  $VO_4$  structure for RTP wafers, and (3) obtain the  $E_b$  of  $VO_4$  and metal. We considered four representative metals (Al, Fe, Cu, and Ni) that are typical impurities in the semiconductor manufacturing process.

### 2. Calculation details

In this study, we conducted density functional theory (DFT) calculations within the generalized gradient approximation for electron exchange and correlation using CASTEP software [10]. A cut-off energy of 310 eV was obtained for the plane wave under the application of three-dimensional periodic boundary conditions. The k-point was set at  $2 \times 2 \times 2$  points in a Monkhorst-Pack [11] grid. Only the electrically neutral state was treated, whereas

the electron spin interaction was negligible. A 64-Si-atom model was created by multiplying the conventional Si unit cell by  $2 \times 2 \times 2$  times. The application of the three-dimensional periodic boundary conditions resulted in a dense model with one  $VO_x$  and metal per 64 Si atoms. Therefore, by fixing the outermost atoms of the model and the length of the lattice, the interaction with adjacent cells was reduced to negligible.

First, we obtained the  $E_b$  of  $V$  and O using Eq. (1) to explore the  $VO_4$  structure in the RTP wafer.

$$E_b = (E_{tot}[Si_{63}VO_{x-1}] + E_{tot}[Si_{64}O_1]) - (E_{tot}[Si_{63}VO_x] + E_{tot}[Si_{64}]), \quad (1)$$

where  $E_{tot}[Si_{63}VO_{x-1}]$ ,  $E_{tot}[Si_{64}O_1]$ , and  $E_{tot}[Si_{63}VO_x]$  are the total energies of models with the inclusion of one  $VO_{x-1}$ , one O, and one  $VO_x$ , respectively.  $E_{tot}[Si_{64}]$  represents the total energy of a 64-Si-atom structure.

Next, the metal was arranged to the most stable site {Al: Substitutional (Sub), Fe: Tetrahedral (T), Ni: Hexagonal (H), Cu: Tetrahedral (T)} near  $VO_4$  in Si structure. The  $E_b$ s of  $VO_4$  and the metals placed on the interstitial and substitutional sites were obtained using Eq. (2a) and (2b) as follows:

$$E_b = (E_{tot}[Si_{63}VO_4] + E_{tot}[Si_{64}M_1]) - (E_{tot}[Si_{63}VO_4\_M_1] + E_{tot}[Si_{64}]), \quad (2a)$$

$$E_b = (E_{tot}[Si_{63}VO_4] + E_{tot}[Si_{63}M_1]) - (E_{tot}[Si_{62}VO_4\_M_1] + E_{tot}[Si_{64}]), \quad (2b)$$

where  $E_{tot}[Si_{63}VO_4]$ ,  $E_{tot}[Si_{64}M_1]$ ,  $E_{tot}[Si_{63}M_1]$ ,  $E_{tot}[Si_{63}VO_4\_M_1]$ , and  $E_{tot}[Si_{62}VO_4\_M_1]$  are the total energies of models with the inclusion of one  $VO_4$ , one metal at the interstitial site, one metal at the substitutional site, one  $VO_4$  and one metal at the interstitial site, and one  $VO_4$  and one metal at the substitutional site, respectively.

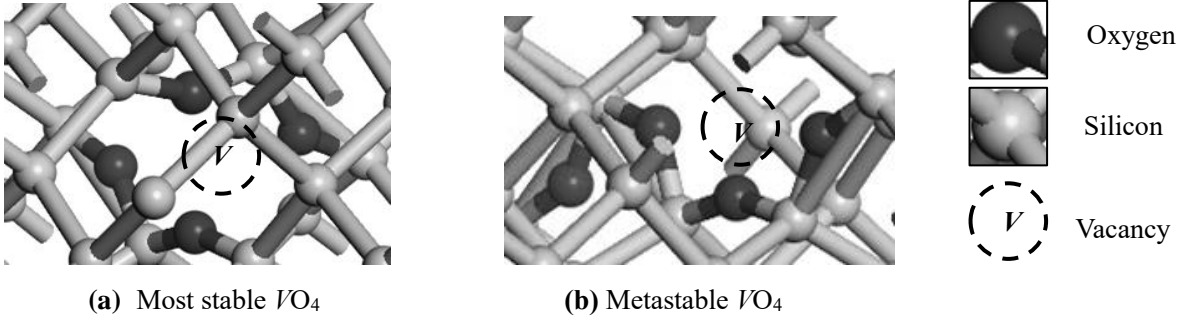
### 3. Results and discussion

#### 3.1 $VO_4$ structure of RTP wafers

Because FTIR detected the presence of  $VO_4$ , it can be considered that  $V$  forms a stable bond with four O atoms in the RTP wafer. The  $E_b$  of  $V$  and O was determined to explore the  $VO_4$  structure. Table 1 shows the  $E_b$  accumulation of  $V$  and O. From Table 1,  $V$  indicates a higher  $E_b$  as the number of O increases. This means that the energy gain increased as the number of O that binds with  $V$  increased, and the binding of  $V$  and O progressed with ease in the RTP wafers. Furthermore, when  $V$  and O were combined in a configuration that was different from the most stable structure,  $E_b$  increased, and an energy gain was observed. A higher accumulation  $E_b$  and energy gain of the metastable  $VO_4$  than that of the most stable  $VO_3$  structure is suggestive of the existence of the metastable  $VO_4$  in the RTP wafer. Figure 1 represents the most stable (a) and metastable (b)  $VO_4$  model structures. In the most stable  $VO_4$  structure one  $V$  is surrounded by O atoms, whereas O atoms are arranged in series near  $V$  in the metastable  $VO_4$ .  $E_b$  was obtained by arranging metals near  $VO_4$ .

**Table 1.**  $E_b$  accumulation between  $V$  and O (eV)

	Most stable (eV)	Metastable (eV)
$VO$	1.416	1.416
$VO_2$	2.964	2.733
$VO_3$	4.424	3.857
$VO_4$	5.858	4.754

**Fig. 1.** Structure of (a) most stable  $VO_4$  and (b) metastable  $VO_4$ 

### 3.2 $E_b$ of $VO_4$ with metals

Figure 2 shows the  $E_b$  of  $VO_x$  with metals. The  $E_b$  was compared with that of Fe-B (0.65 eV), which is commonly used as an index for complex formations. The  $E_b$  of  $VO$  with different metals, and that of  $VO_2$  with Al and Fe were above 0.65 eV, indicating the formation of respective complexes with ease. In contrast, the  $E_b$  of  $VO_2$  with Ni and Cu were below 0.65 eV, indicating difficulty to form their complexes. These results agree with those obtained in a previous study [9]. Further,  $E_b$  of the most stable  $VO_4$  was lower than 0.65 eV and exhibited the lowest total energy, suggesting difficulty to form complexes. However, calculated  $E_b$  of the metastable  $VO_4$  was higher than 0.65 eV and ranged between 0.9 and 1.4 eV, implying the formation of complexes with ease.

Regarding the differences in  $E_b$  owing to the  $VO_4$  structure, we assumed that the metastable  $VO_4$  has a larger space around  $V$  compared to the most stable  $VO_4$ , and the metal can diffuse with ease. Therefore, the atomic distances, between the metal with the highest  $E_b$  configuration and the surrounding Si, for the most stable  $VO_4$  and metastable  $VO_4$  were calculated. Figure 3 shows the atomic distance dependence of  $E_b$  in the most stable  $VO_4$  (black symbols) and metastable  $VO_4$  (white symbols). The average values of the atomic distances, measured from the metal placed at the interstitial site to the first and the second neighboring Si, were obtained. For the metal placed at the substitutional position, distance from the metal to the first neighboring Si was measured and the average value was obtained. In addition, Fig. 4 represents examples of the typical Ni arrangement in which  $E_b$  is the highest near the most stable and metastable  $VO_4$ .

The  $E_b$ s of Fe, Ni, and Cu tend to increase when the average atomic distance is large as clearly seen from Fig. 3(a). As shown in Fig. 4(a), the most stable  $VO_4$  is a structure in which O surrounds  $V$ ; hence the metal cannot move to the vicinity of  $V$  where the space is large, and calculated  $E_b$  is low. However, as shown in Fig. 4(b), in the metastable  $VO_4$ , the arrangement of O is different, and the metal can move to the vicinity of  $V$ ; hence  $E_b$  is considered to be high. Fig. 3(b) shows shorter average atomic distance for Al when  $E_b$  is high. Because Al is located at the substitutional site, a significant change in  $E_b$  was observed due to the influence of factors different from those of

metals.

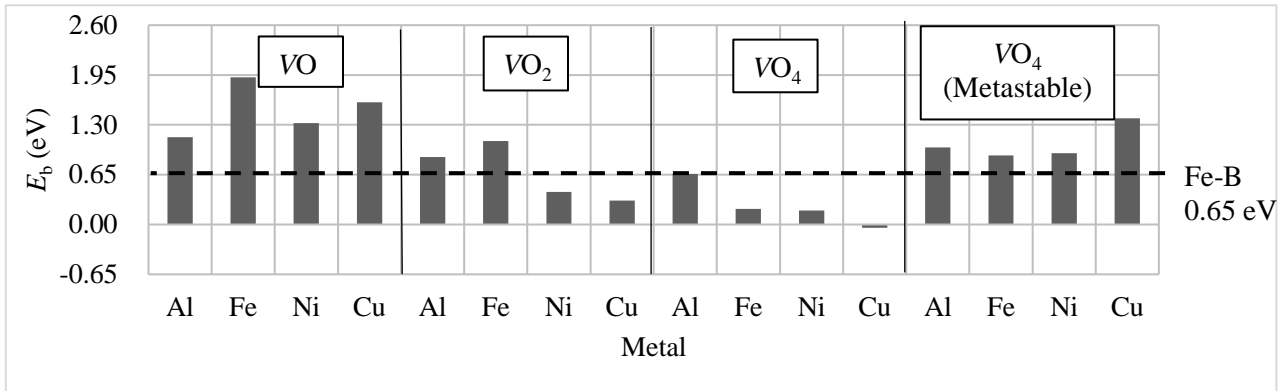


Fig. 2.  $E_b$  of  $VO$ ,  $VO_2$ ,  $VO_4$ , and  $VO_4$  (metastable) with metal.

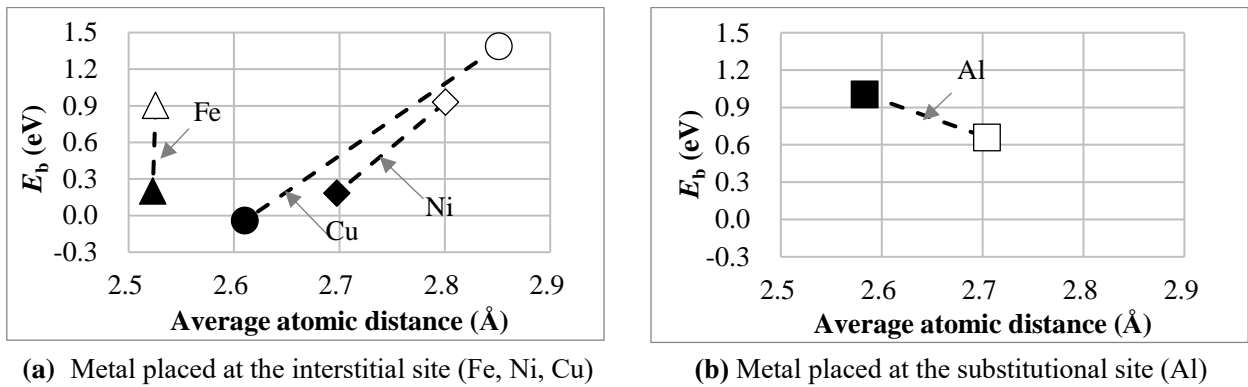
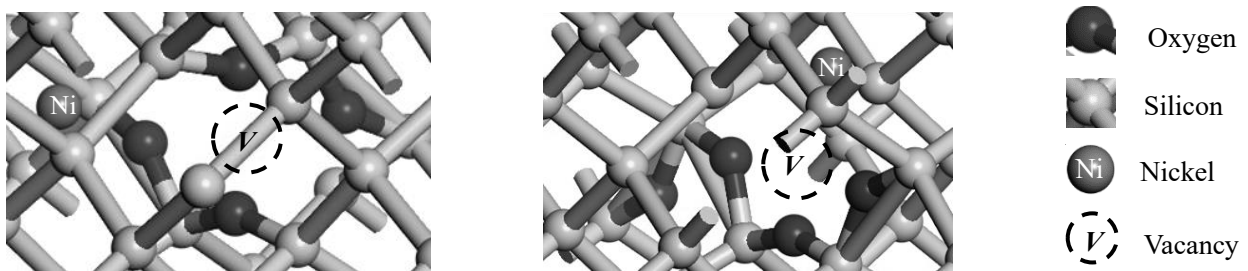


Fig. 3. Atomic distance dependence of  $E_b$  for  $VO_4$  and metals at (a) the interstitial site and (b) the substitutional site.

(Black Symbols indicate binding with most stable  $VO_4$ . White symbols indicate binding with metastable  $VO_4$ .)



(a) Complex of Most stable  $VO_4$  with Ni

(b) Complex of metastable  $VO_4$  with Ni

Fig. 4. Complexes of (a) most stable  $VO_4$  with Ni and (b) metastable  $VO_4$  with Ni

#### 4. Conclusion

In this study, to investigate whether  $VO_x$  in RTP wafers functions as a gettering site, the  $E_b$  values of  $VO_4$  and metal were obtained using the first-principles calculations. The  $E_b$  of the most stable  $VO_4$  with different metals was evaluated to be lower than that of Fe-B (0.65 eV), and the formation of complexes was difficult. However, the calculated  $E_b$  of the metastable  $VO_4$  with the metals was in the range of 0.9–1.4 eV, and the complexes could form with ease. This is because, O arrangement in the metastable state is different from that of the most stable  $VO_4$ ; the

metal tends to approach to the vicinity of  $V$  where the space is large. These results indicate that RTP wafers can have a gettering effect on metals without BMDs.

## REFERENCES

- [1] R. Falster, V. V. Voronkov, F. Quast, *Physica Status Solidi (b)*, Volume 222, Issue 1, pp. 219-244 (2000).
- [2] Nikolai Yarykin and Jorg Weber, *Applied Physics Letters* 109, 102101 (2016).
- [3] Nikolai Yarykin and Jorg Weber, *Solid State Phenomena Vols. 205-206* (2014), pp. 255-259.
- [4] V. P. Markevich, A. R. Peaker, I. F. Medvedeva, V. E. Gusakov, L. I. Murin, and B. G. Svenson, *ECS Transactions*, 18 (1) 1013-1018 (2009).
- [5] V. V. Voronkov, and R. Falster, *Journal of The Electrochemical Society*, 149 (3) G167–G174 (2002).
- [6] V. Akhmetov, G. Kissinger, and W. von Ammon, *Physica B*, 404 (2009) p.4572.
- [7] D. Kot, G. Kissinger, J. Dabrowski, and A. Sattler, *ECS Journal of Solid State Science and Technology*, 7 (12) (2018) P.707.
- [8] Haruo Sudo, et al., *ECS Journal of Solid State Science and Technology*, 8 (1) pp. 35-40 (2019).
- [9] Sho Shirasawa, Koji Sueoka, Tadashi Yamaguchi, Kazuyoshi Maekawa, *Materials Science in Semiconductor Processing* 44 (2016) pp. 13-17.
- [10] The CASTEP code is available from Dassault Systems Biovia Inc.
- [11] H. Monkhorst and J. Pack, *Physcal Review B.*, 13, 5188, (1976).

## Numerical Modeling and Evaluation of Constitutional Supercooling during Silicon Single Crystal Growth by Cz Method

Yuji Mukaiyama<sup>1,2\*</sup>, Yuki Fukui<sup>3</sup>, Toshinori Taishi<sup>3</sup>, Vladimir Artemiev<sup>4</sup>, Yusuke Noda<sup>2</sup>, Koji Sueoka<sup>2</sup>

<sup>1</sup>STR Japan K.K., East Tower 15F, Yokohama Business Park, 134, Goudo-cho, Hodogaya-ku, Yokohama, Kanagawa 240-0005, Japan

<sup>2</sup>Department of Information and Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama, 719-1197, Japan

<sup>3</sup>Faculty of Engineering, Shinshu University, Wakasato, Nagano 380-8553, Japan

<sup>4</sup>Semiconductor Technology Research d.o.o. Beograd (STR Belgrade), Belgrade, Serbia

E-mail address: [yuji.mukaiyama@str-soft.co.jp](mailto:yuji.mukaiyama@str-soft.co.jp)

### Abstract

Heavy doping of impurities like boron (B) and phosphorus (P) during silicon (Si) single-crystal growth by the Cz method has been known to degrade the quality of Si single-crystals. The degradation is associated with a morphological instability such as cellular growth caused by constitutional supercooling (CS) at the growth interface in the melt. Therefore, it is necessary to prevent CS to grow high-quality heavy-doped Si single crystals. In this study, we performed a three-dimensional numerical simulation considering the transport of B, including segregation, in the melt to predict CS formation during Si single crystal growth by the Cz method. Within the simulations, the actual and equilibrium temperature gradient in the melt near the growth interface was obtained, where the latter was calculated by the local gradient of B concentration. The difference between the gradient of actual and equilibrium temperature is defined as the constitutional supercooling gradient (CSG). The negative value of CSG indicates the possibility of CS occurrence at the growth interface. We evaluated the numerical model by comparing the calculated CSG distributions with experimental data. It was confirmed that the cellular growth region observed in the experiment agreed well with the CS region predicted by numerical simulation.

### 1. Introduction

The Czochralski (Cz) method has been used in the manufacturing industry to produce doped-silicon (Si) single crystals to prepare Si wafers with low electrical resistivity. The typical species used as dopants are B, P, and As; required concentrations are varied depending on the desirable resistivity [1]. The Si crystals with heavily doping, grown using the Cz method, as substrates for electrical devices, such as MOSFET and CMOS, have been applied. The quality improvement of the substrate is continuously required to increase the performance of such an electrical device. Heavily doped Si crystals include a dopant concentration larger than  $1 \times 10^{19}$  (1/cm<sup>3</sup>), which is limited by the solubility of each dopant species. However, it is well known that the deterioration of crystal quality happens during heavy-doped Si crystals growth using the Cz method owing to constitutional supercooling (CS) [2-5]. Several theoretical models have been applied to determine the criterion that CS occurs during crystal growth [2, 6]. According to these theories, a higher growth rate and the concentration of the dopant in the melt and a lower temperature gradient in the melt near the growth interface are preferable for CS occurrence. These theories are

useful to estimate the criterion on CS occurrence approximately; however, it is hard to directly predict the distribution of CS and investigate the mechanism of CS formation associated with the growth conditions like crystal/crucible rotation and gas flow, and furnace design. Recently, a new approach based on a three-dimensional (3D) unsteady simulation accounting for the transport of dopant species in the melt, including the segregation effect has been proposed [7]. In this study, the new approach was evaluated with experiments of B heavily doped Cz Si crystal growth.

## 2. Numerical simulation

### 2-1. Mathematical description

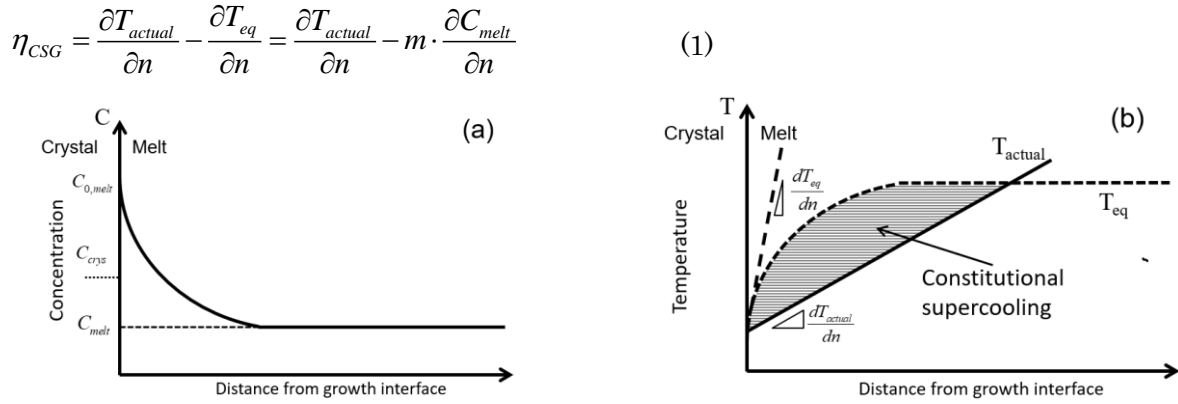
Two-dimensional (2D) axisymmetric steady simulations were conducted to calculate the global heat and mass transfer over the entire furnace, turbulent melt convection, and argon gas flow using the Basic module of the CGSim commercial software [8]. Subsequently, 3D unsteady simulations were performed for more detailed computations accounting for the turbulent convection, heat transfer, and dopant species transport using the Flow module of the CGSim software package.

Series governing differential equations for momentum, heat transfer (conduction, convection, and radiation), and mass transfer in the computational domain are solved self-consistently in the computations [9]. Turbulent mixing of the flow in the melt is modeled based on the Reynolds-averaged Navier-Stokes equation approach for 2D global simulation and the Large Eddy Simulation for 3D unsteady simulation. Along the free melt surface, the Marangoni effect is considered in the boundary condition for the tangential velocity component. The material properties of the Si melt and crystal used in the simulations were borrowed from [10]. In 3D unsteady simulations, the concentration of B in the melt was assumed to be a passive scalar, and the transport of the concentration was solved by accounting for convection and diffusion. Moreover, B is assumed to be incorporated into the growing Si crystal by the segregation effect, and the mass of B between the crystal and melt through the growth interface is balanced.

### 2-2. Evaluation model for constitutional supercooling

An evaluation model was proposed to predict the possibility of CS occurrence near the growth interface. Figure 1 shows the scheme that theoretically describes the CS occurrence near the growth interface. Figure 1 (a) shows the distribution of dopant concentration near the growth interface in the melt;  $C_{cryst}$  is the concentration incorporated in the crystal,  $C_{0,melt}$  is the concentration near the interface in the melt, and  $C_{melt}$  is the concentration in the bulk melt region. Because the equilibrium segregation coefficient of dopant is generally smaller than unity ( $k < 1$ ), the dopant is exhausted from the growing interface and accumulated near the growth interface in the melt, leading to a higher concentration of dopant near the interface in the melt than in the bulk melt region. Fig.1 (b) indicates both the distribution of actual  $T_{actual}$  and equilibrium temperature  $T_{eq}$  in front of the growth interface in the melt. The distribution of  $T_{eq}$  can be obtained from that of the dopant concentration shown in Figure 1 (a) and the liquidus line in the phase diagram of the Si-dopant binary compound. According to theoretical studies [2, 6], when  $T_{actual}$  is lower than  $T_{eq}$ , CS may occur in the melt. In this work, we accounted for the difference between the calculated gradient of  $T_{actual}$  and  $T_{eq}$ , as shown in Fig. 1 (b), to evaluate the possibility of CS occurrence. The gradient of  $T_{actual}$  was directly calculated by the simulation, whereas the gradient of  $T_{eq}$  was calculated using that of dopant concentration predicted within the simulation and slope ( $m$ ) of the liquidus line reported by Ref. [11]. This difference is called the

constitutional supercooling gradient (CSG), as described in Eq. 1. The first and second terms on the right-hand side of the equation refer to the gradient of  $T_{actual}$  and  $T_{eq}$ , respectively, where the gradient of  $T_{eq}$  is obtained by multiplying the slope of the liquidus line by that of dopant concentration near the growth interface. A negative CSG value indicates a CS state near the growth interface.



**Fig.1.** Schematic view of the (a) dopant concentration distribution and (b) distribution of  $T_{actual}$  and  $T_{eq}$  near the growth interface in the melt.

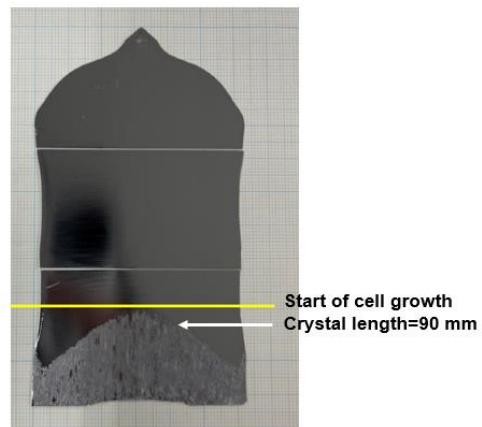
### 3. Experimental setup

Heavily B-doped crystals with a 60 mm diameter were grown using a laboratory scale Cz furnace. The furnace consists of a conventional hot zone with the quartz crucible, graphite heaters, and insulation enclosed in a water-cooled steel container. The initial B concentration of  $4.1 \times 10^{20}$  ( $1/\text{cm}^3$ ) in the melt was prepared by adding B before the melting stage. The basic growth conditions were as follows: the pulling rate was varied during the growth process to approximately maintain the required crystal diameter and the rotation speeds of the crucible and crystal were 10 rpm, in opposite directions.

### 4. Results and discussion

Figure 2 shows the photograph of a vertical cross-sectional grown Si crystal through the center position. The region with gray color indicates the cellular growth state, starting at the crystal length of about 85 mm. As the crystal growth proceeds, the region of the cellular growth gradually extends, and finally cover whole region at the crystal length of about 105 mm.

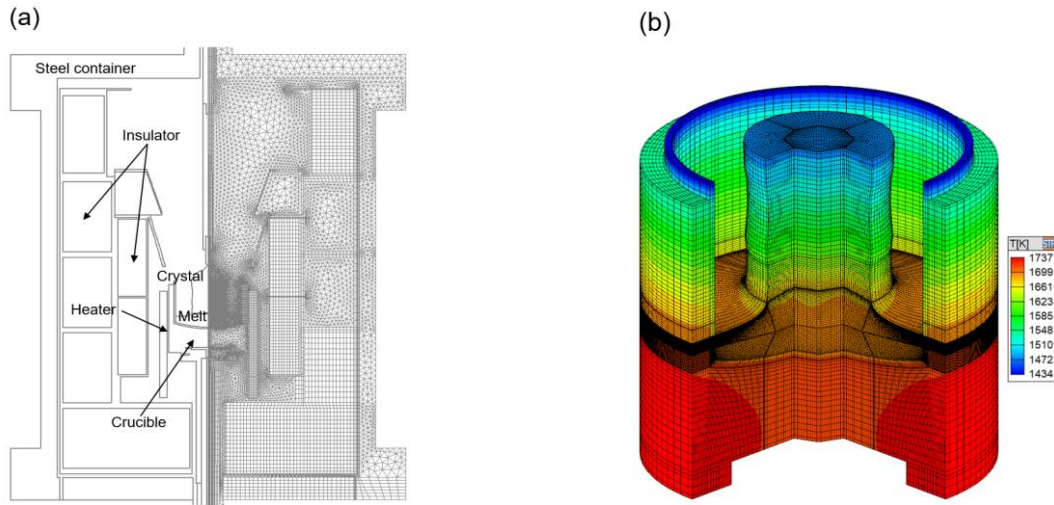
Figure 3 illustrates the computational grid, composite arrangement, and temperature distribution over the entire Cz furnace (a) and within a local 3D growth domain, including the crystal, melt, and crucible (b). In particular, the computational grids in front of the growth interface in the melt are condensed to catch the diffusion boundary layer of B concentration accurately. Figure 4 (a) shows the time-averaged over 60-second interval CSG distribution over the



**Fig.2.** Photograph of a vertical cross-sectional Si crystal through the crystal center position.

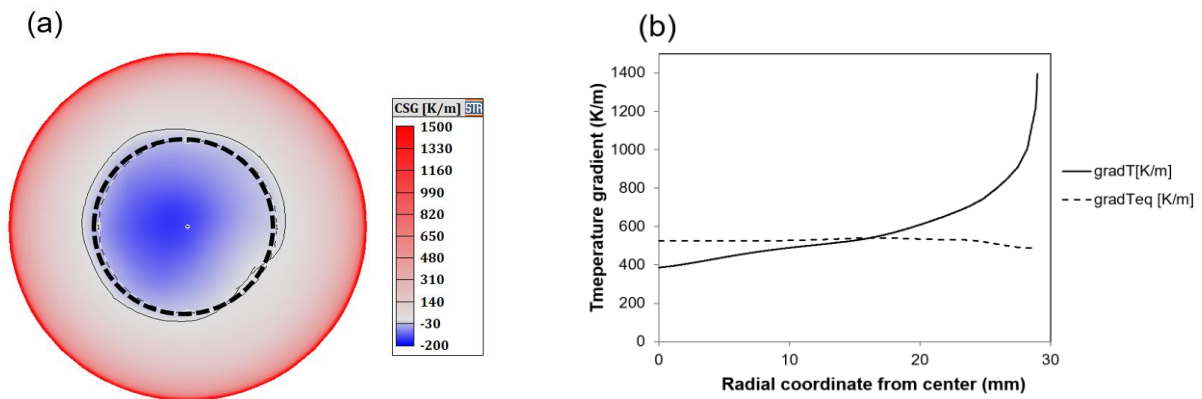


growth interface at the pulling rate of 1.0 mm/min, the crystal length of 90 mm and the B concentration in the melt of  $5.65 \times 10^{20}$  (1/cm<sup>3</sup>). The blue contour indicates the negative CSG value, indicating CS state on the growth interface. Where the circle with a dashed line indicates the periphery of cellular growth region observed in the experiment, which agrees well with the predicted CS region.



**Fig.3.** (a) Material arrangement (left) and computational grids (right) over the entire Cz furnace, and (b) the temperature and grid distributions used in the 3D model.

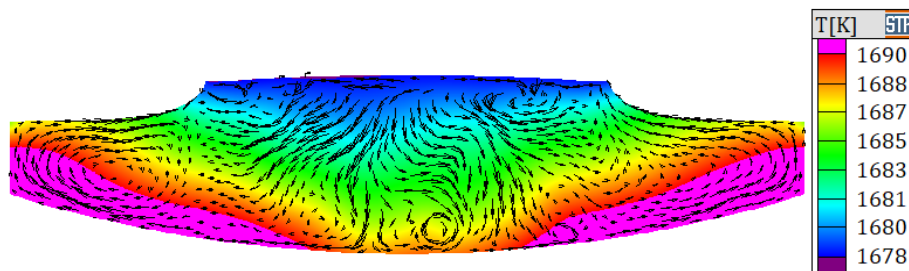
To study the time-averaged distribution of CSG in detail, the time-averaged distributions of  $T_{actual}$  and  $T_{eq}$  gradient in front of the growth interface in the melt, comprising the CSG distribution, were investigated, as shown in Fig. 4 (b). The distribution of  $T_{eq}$  gradient is almost uniform over the growth interface; however, the distribution of  $T_{actual}$  gradient is not uniform, significantly decreases toward the central region of the melt, and is lower than that of  $T_{eq}$ .



**Fig.4.** (a) Time-averaged over 60-second interval CSG distribution and periphery of cellular growth region observed in experiment, and (b) plot of time-averaged gradient of actual (solid line) and equilibrium temperatures (dashed line) from the center to the edge of the growth interface in the horizontal direction.

The heat transfer in the melt should affect the  $T_{actual}$  gradient near the growth interface. Figure 5 demonstrates the instantaneous temperature distribution and flow pattern in the melt. The temperature decreases toward the central region, leading to a lower-temperature gradient around the central region of the growth interface. It is thought that

the melt with high temperature enters the region near the crystal periphery from the hot zone near crucible through melt convection and is gradually cooled toward the central region.



**Fig.5.** Instantaneous temperature distribution and velocity vectors in the melt.

## Conclusion

The numerical simulation model to predict the constitutional supercooling for heavily B -doped Si growth by Cz method was evaluated with experimental data. It was established that the result of the numerical simulation agreed well with the experiment. This numerical approach is expected to be a strong tool to optimize the growth conditions to suppress constitutional supercooling.

## References

- [1] G. Eranna, CRYSTAL GROWTH AND EVALUATION OF SILICON for VLSI and ULSI, CRC Press, (2015).
- [2] J. Friedrich, L. Stockmeier, and G. Müller, ACTA PHYSICA POLONICA A 124, (2013), 219.
- [3] T. Taishi, X. Huang, M. Kubota, T. Kajikaya, T. Fukami, and K. Hoshikawa, Jpn. J. Appl. Phys. 39, (2000), L5.
- [4] T. Taishi, Y. Ohno, and I. Yonenaga, J. Crystal Growth, 393, (2014), 42.
- [5] H. D. Chiou, Journal of The Electrochemical Society, 152(4), (2005), G295.
- [6] W.A. Tiller, K.A. Jackson, J.W. Rutter, and B. Chalmers, Acta Metall. 1, (1953), 428.
- [7] Y. Mukaiyama, V. Artemyev, and K. Sueoka, J. Crystal Growth, 597, (2022), 126844.
- [8] <http://www.str-soft.com/products/CGSim/>
- [9] CGSim Basic Module, Ver. 20, Theory Manual, STR IP Holding, LLC, Richmond, USA
- [10] V. Kalaev, D. Borisov, and A. Smirnov, J. Crystal Growth, 580, (2022), 126464.
- [11] R. W. Olesinski and G. J. Abbaschian, The As-Si (Arsenic-Silicon) system, Bulletin of Alloy Phase Diagrams 6 (1985) 254.

## First-Principles Calculation on N-V Complex Formation in Si Crystal Growth

Akira Sada<sup>1\*</sup>, Yusuke Noda<sup>2</sup>, Koji Sueoka<sup>2</sup>, Kaoru Kajiwara<sup>3</sup> and Masataka Hourai<sup>3</sup>

<sup>1</sup>Graduate School of Computer Science and Systems Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama, 719-1197 Japan

<sup>2</sup>Department of Information and Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama, 719-1197 Japan

<sup>3</sup>SUMCO Corporation, 1-52 Kubara, Yamashiro-cho, Imari-shi, Saga, 849-4256, Japan

e-mail: akira.sd.sub2192@gmail.com

### Abstract

It is known that the nitrogen (N) doping during silicon (Si) single crystal growth significantly reduces the size of voids formed. This is believed to be due to the fact that N prevents the aggregation of vacancies ( $V$ ) by trapping  $V$ . In this study, we performed first-principles calculations of possible N- $V$  complexes in Si exhaustively and investigated their formation process to clarify the mechanism of the void reduction effect by N doping. In our calculations, the energy barriers for the formation process of the N- $V$  complexes were evaluated using linear and quadratic synchronous transit (LST/QST) method. Our theoretical results show that N doping has a good effect on prevention of  $V$  aggregation to form large-sized void defects in Si crystals.

### Introduction

In Si single-crystal growth, void defects formed by the aggregation of vacancies ( $V$ ) cause device performance to deteriorate. Because of this, the control of point defects is an important technological issue. It has been known that nitrogen (N) doped in the crystal prevents  $V$  aggregation and significantly reduces the size of void defects [1,2]. The mechanism is assumed to be that N prevents  $V$  aggregation by trapping vacancies in the atoms [3-7]. However, experimental observation of the point defects behavior is difficult, and the mechanism of void reduction is still unknown. In this study, we analyzed the characteristics of point defects and N atoms by first-principles calculations based on the density functional theory. The structure of complexes composed of N and  $V$  in Si single crystals has been reported in many previous studies on N doping [8-11]. However, there is no systematic investigation of the structural changes between complexes based on a comprehensive search for stable structures of the complexes.

In this paper, we investigate the formation process of various complexes involving N and  $V$ . And, we discuss it based on binding energies and energy barriers of the complexes using theoretical simulations.

### Calculation detail

We focused on all the possible configurations of N- $V$  complexes including N (two atoms or less) and  $V$  (two defects or less) with Si 64-atom crystal structure models ( $2 \times 2 \times 2$  supercells). Si 512-atom crystal structure models ( $4 \times 4 \times 4$  supercells) with energetically stable structures of the N- $V$  complexes extracted from the exhaustive search were adopted to evaluate total energies of those models accurately. In this study, the structural change of the complex including N and  $V$  was investigated by DFT calculations. The PBE function of generalized gradient approximation (GGA) was employed to approximate the exchange-correlation energy, and DFT calculations were performed by the CASTEP software. The details of the calculation procedure can be found in Refs. 12-14. The cutoff energy was

set to 340 eV. The Monkhorst-Pack  $k$ -point samplings of a  $2 \times 2 \times 2$  grid for Si 64-atom models and a  $1 \times 1 \times 1$  grid for Si 512-atom models were adopted. Three-dimensional periodic boundary conditions were applied during the structural optimization calculations for both the 64-atom and the 512-atom models.

We evaluated the binding energy to compare the stability of the N- $V$  complexes. The binding energy for adding a defect  $Y$  into Si  $n$ -atom crystal structure with a defect  $X$  can be expressed by the following equation,

$$E_b^{X-Y} = (E_{tot}[\text{Si}_n X] + E_{tot}[\text{Si}_n Y]) - (E_{tot}[\text{Si}_n XY] + E_{tot}[\text{Si}_n]),$$

where  $E_{tot}[\text{Si}_n X]$ ,  $E_{tot}[\text{Si}_n Y]$ ,  $E_{tot}[\text{Si}_n XY]$  and,  $E_{tot}[\text{Si}_n]$  represent total energies of the  $n$ -atom Si with single  $X$  defect, the  $n$ -atom Si with single  $Y$  defect, the  $n$ -atom Si with both  $X$  and  $Y$  defects, and the perfect  $n$ -atom Si.

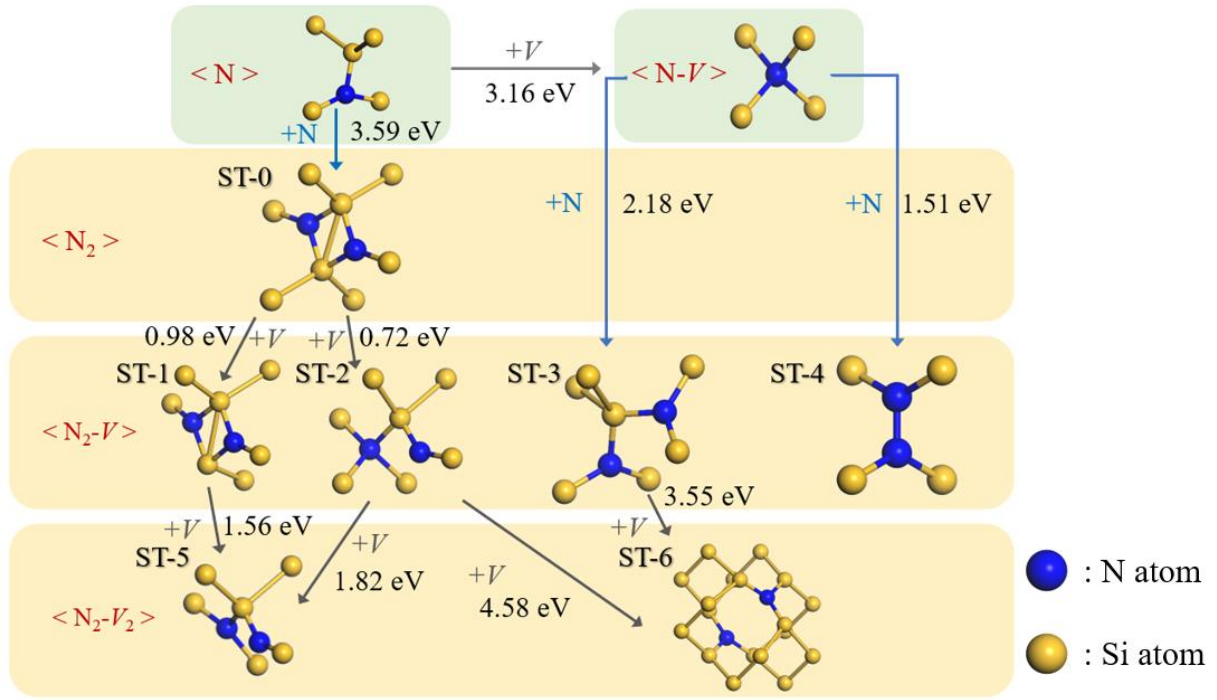
We used linear and quadratic synchronous transit (LST/QST) method [15] to investigate the transition state in a target reaction. And then, an energy barrier of the target reaction was evaluated as the energy difference between total energies of an initial state and a transition state with the Si 64-atom model.

## Result and Discussion

The summary of our calculation results for the N- $V$  complexes are shown in Fig. 1. Values in Fig. 1 represent the binding energies of the complex and the reacting N or  $V$  in the Si 512-atom model. We confirmed that ST-0, ST-3, and ST-6 are the most stable structures of  $\text{N}_2$ ,  $\text{N}_2-V$ , and  $\text{N}_2-V_2$ , respectively. These are stable structures of complexes in Si which have been discussed in previous studies [8].

In the reaction between two interstitial N defects in Si crystal,  $\text{N}_2$  defect (ST-0) was obtained as the most stable structure. This is one of the well-known stable forms of N point defects in Si [8-11]. In the subsequent reactions with  $V$ , stable  $\text{N}_2-V$  structures (ST-1 and ST-2) were found. The binding energy of the ST-1 is about 0.26 eV larger than that of ST-2, and we found that the ST-1 is considered to be more likely to form. However, the most stable structure of  $\text{N}_2-V_2$  (ST-6) cannot be obtained by adding  $V$  into the ST-1. Whereas, we predicted other reaction processes between  $\text{N}_2$  (ST-0) and  $\text{N}_2-V_2$  (ST-5) from our DFT calculations because the binding energy of ST-5 is relatively high.

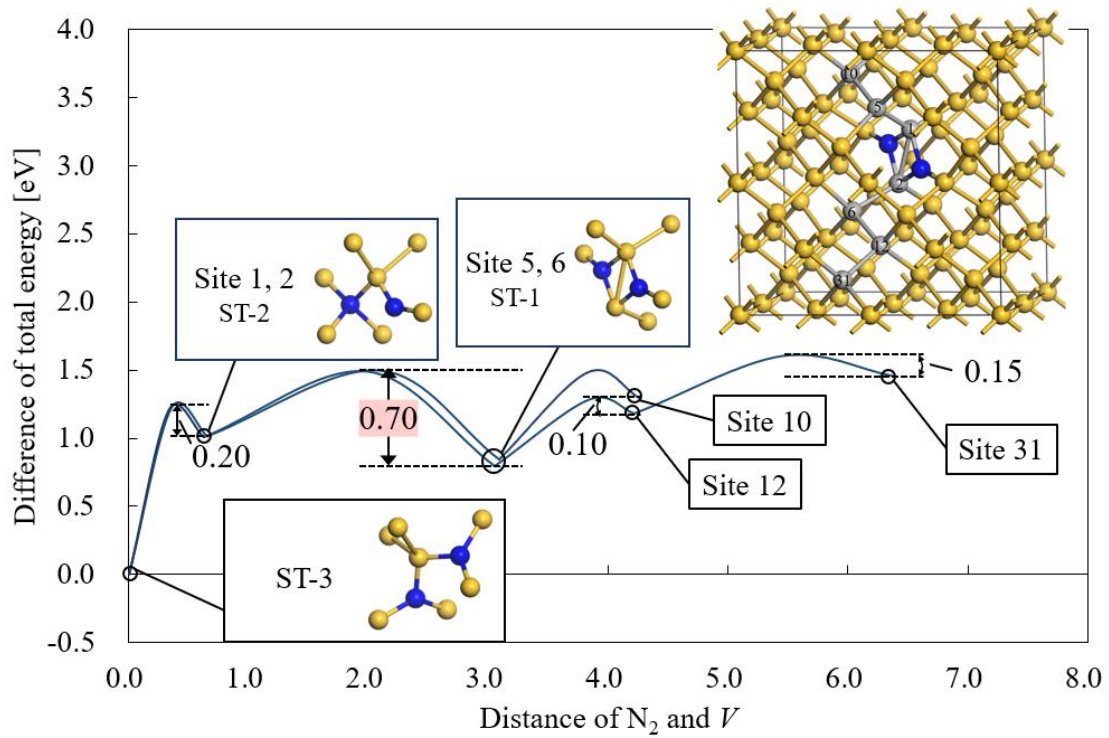
In case of a reaction with single N defect and single  $V$  in Si, a substituted nitrogen (N- $V$  shown in Fig. 1) can be easily formed. In the subsequent reactions with N, stable  $\text{N}_2-V$  structures (ST-3 and ST-4) were found. ST-4 has been well known as a typical stable structure for  $\text{N}_2-V$  [8-10]. However, the ST-6 cannot be obtained by adding  $V$  into the ST-4.



**Fig. 1.** Atomic-level structures and binding energies of N–V complexes in Si (blue balls: N atoms, yellow balls: Si atoms).

In the above paragraphs, we have discussed the various reaction processes of N–V complexes in terms of binding energies. However, we have not considered the structural change between different N–V complexes with the same composition. Here, we discuss the energy barriers to be needed for structural changes in the same composition. In this study, we focused on V migration to N<sub>2</sub> defect in Si, which correspond to the structure changes from the ST-0 (N<sub>2</sub> + V) to the ST-3 (N<sub>2</sub>–V). Fig. 2 shows the calculation results of energy diagram for V migration to N<sub>2</sub> defect with a relatively small energy barrier. The vertical and horizontal axes of Fig. 2 represent energy difference from the total energy of ST-3, and the distance between V and the center of N<sub>2</sub> defect, respectively. Site numbers shown in Fig. 2 indicate positions of migrating V in the Si 64-atom model with the N<sub>2</sub> defect.

Our results show that the energy barrier for V migration from Site 5 or Site 6 (ST-1) to Site 1 or Site 2 (ST-2) is 0.70 eV. This is larger than an energy barrier (0.30 eV) of V migration in a perfect Si crystal. We predicted a reaction pathway from the ST-2 to the ST-3 with the energy barrier of 0.20 eV as the next reaction of the V migration from the ST-1 to the ST-2, indicating that the ST-3 can be easily formed by V migration because the total energy of the ST-3 is about 1 eV lower than that of the ST-2. After the ST-3 is formed, the energy barrier to be needed for returning the previous structure by V migration is about 1.2 eV. This indicates that the N<sub>2</sub> defect can trap V defects easily and prevents V aggregation to form void defects. We confirmed similar results for the reaction pathways from the ST-1 (N<sub>2</sub>–V + V) to the ST-5 (N<sub>2</sub>–V<sub>2</sub>) and from the ST-3 (N<sub>2</sub>–V + V) to the ST-6 (N<sub>2</sub>–V<sub>2</sub>).

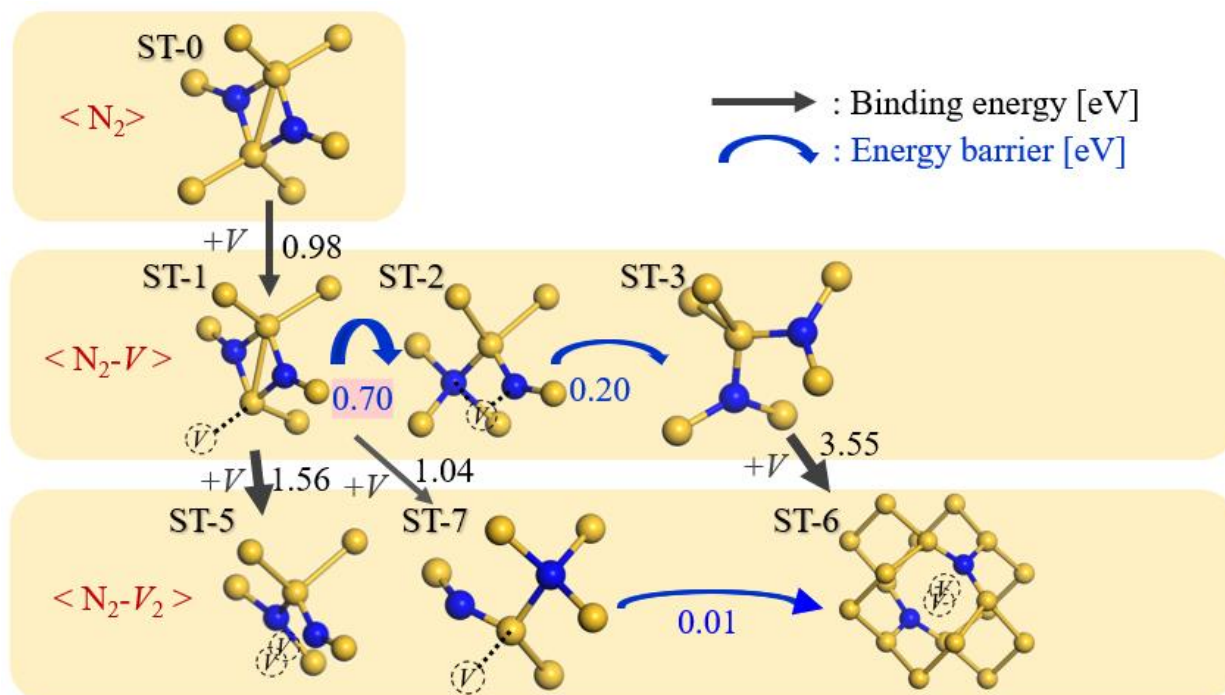


**Fig. 2.** Energy barriers of  $N_2$ - $V$  complexes in structural changes due to  $V$  migration.

Our calculation results on the structural changes and the energy barriers for possible  $N$ - $V$  complexes are summarized in Fig. 3. Values indicated straight and curved arrows are binding energies and energy barriers for reactions of  $N$ - $V$  complexes, respectively. The ST-0 including a pair of two interstitial  $N$  turns into the ST-1 by  $V$  migration. After crossing the energy barrier of 0.7 eV by the first  $V$  migration, the ST-1 can turn into the ST-2 or the ST-3, and then the ST-3 can turn into the ST-6 by the second  $V$  migration. Our results also indicate that the ST-1 can turn into the ST-5 or ST-7 by the second  $V$  migration when the energy barrier of 0.7 eV is not crossed. We predicted another reaction pathway from the ST-7 to the ST-6 with a very small energy barrier of 0.01 eV.

## Conclusion

In this study, the formation processes of  $N$ - $V$  complexes in Si crystals are predicted in terms of binding energies and energy barriers using DFT calculations. The binding energy calculation finds the stable structures of the  $N$ - $V$  complexes, and the energy barrier calculation based on the LST/QST method demonstrates the migration path of single  $V$  defect in Si crystals. Some of the  $N$ - $V$  complexes were obtained by the structural change after  $V$  migration to  $N_2$  defect. We expect that the  $N_2$  defect which can stabilize single  $V$  defect leads to prevention of  $V$  aggregation to form large-sized void defects in Si crystals.



**Fig. 3.** Forming process of N-V complexes including the result of energy barrier.

## REFERENCES

- [1] T.Abe, T.Masui, H.Harada, J.Chikawa, *ECS Proc.* **PV85-5** (1985) 543.
- [2] W.V. Ammon, P. Dreier, W. Hensel, U. Lambert, L. Koster, *Mater. Sci. Eng.* **36** (1996) 33 (and references therein).
- [3] M. Iida, W. Kusaki, M. Tamatsuka, E. Iino, M. Kimura, S. Muraoka, *ECS Proc.* **PV99-1** (1999) 499.
- [4] A. Karoui, F. Karoui, A. Kvit, G. Rozgonyi, Di Yang. *Appl. Phys. Lett.* **80** (2002) 2114.
- [5] K. Nakamura, T. Saishoji, S. Togawa, J. Tomioka, *Proc. Forum on the Sci and Tech. Si Mater.* (1999) 116.
- [6] K. Nakai, Y. Inoue, H. Yokota, A. Ikari, J. Takahashi, A. Tachikawa, K. Kitahara, Y. Ohta, W. Ohashi, *J. Appl. Phys.* **89** (2001) 4301.
- [7] S. Umeno, T. Ono, T. Tanaka, E. Asayama, H. Nishikawa, M. Hourai, H. Katahama, M. Sano, *J. Cryst. Growth* **236** (2002) 46.
- [8] A. Platonenko, F. Gentile, J. Maul, F. Pascale, E. A. Kotomin, R. Dovesi, *Mater. Today Comms.* **21** (2019) 100616.
- [9] A. Karoui, F. Sahtout, G. A. Rozgonyi, M. Hourai, K. Sueoka, *ECS Proc.* **PV-2002-2** (2002) 670.
- [10] R. Jones, I. Hahn, J. P. Goss, P. R. Briddon, S. Öberg, *Solid State Phenomena* **95-96**, (2004) 93.
- [11] M.Taniguchi, K.Sueoka, M.Hourai, *J. Cryst. Growth* **571** (2021) 126249.
- [12] K.Sueoka, E.Kamiyama, J.Vanhellemont, *J. Appl. Phys.* **114** (2013), 153510 (and references therein).
- [13] K. Sueoka, Y. Mukaiyama, S. Maeda, M. Iizuka, V. Mamedov, *ECS, J. Solid State Sci. and Tech.* **8** (2019) 228 (and references therein).
- [14] K. Sueoka, J.Vanhellemont, *Materials Science in Semiconductor Proc.* **9** (2006) 494.
- [15] B. Delley, *J. Chem. Phys.* **92** (1990) 508.

## Theoretical verification of constitutional supercooling and growth conditions in heavily B-doped Si crystal growth by the Czochralski method

Yuki Fukui<sup>1</sup>, Toshinori Taishi<sup>1</sup>, Yuta Watanabe<sup>2</sup>, Nobumasa Kariya<sup>2</sup>

<sup>1</sup>Faculty of Engineering, Shinshu University, Wakasato, Nagano, 380-8553, Japan

<sup>2</sup>M.SETEK Co., Ltd., Myokenmachi, Susaki, Kochi, 785-0042 Japan

e-mail: 21w2056g@shinshu-u.ac.jp, taishi@shinshu-u.ac.jp

### Abstract

In Si single crystal growth using the Czochralski (CZ) method, heavy doping of impurities such as boron (B) and phosphorus (P), with a concentration level of  $10^{19} - 10^{20} \text{ cm}^{-3}$ , is known to degrade the quality of crystals. As one of the phenomena, constitutional supercooling occurs during the growth, and this finally leads to polycrystallization. Therefore, it is necessary to prevent constitutional supercooling in order to grow higher-quality heavily doped Si single crystals. In this study, we grew Si single crystals with a B concentration of  $10^{20} \text{ cm}^{-3}$  using B as a dopant with a large segregation coefficient, and occurrence sites of constitutional supercooling were theoretically verified using two discriminants. The validity of two proposed discriminants is discussed.

### Introduction

Si is used as a semiconductor material as a substrate for various electronic devices, and so research on Si single crystal growth is active. Si single crystals are mainly grown by the CZ method, using mainly B, P, and As as dopants, with the required concentration depending on the desired resistivity. Although heavily doped Si single crystals, with a concentration level of  $10^{19} - 10^{20} \text{ cm}^{-3}$ , are seen as a new possibility for Si processing, it is difficult to grow higher-quality single crystals due to various phenomena. One of the important phenomena encountered in growing higher-quality Si single crystals with uniform composition is segregation of the dopant, and this is linked to the occurrence of constitutional supercooling. A cellular structure is induced by the occurrence of constitutional supercooling, and this leads to polycrystallization. The instability of the growth interface and the occurrence of cellular structures due to constitutional supercooling has been reported in heavily Sb [1], B [2], Ge [3] and As-doping [4] in CZ-Si crystal growth.

For the constitutional supercooling phenomenon, two discriminant formulae have been proposed, by Tiller [5] and by Hurler [6], are these are generally known as eqs. (1) and (2), respectively,

$$\frac{G_L}{v} < \frac{mC_L(1 - k_0)}{k_0D}, \quad (1)$$

$$\frac{G_L}{v} < \frac{mC_L(1 - k_0)k_{eff}}{k_0D}, \quad (2)$$

where  $G_L$  is the temperature gradient in the melt just below the solid-liquid interface,  $v$  is the crystal growth rate,  $m$  is the slope of the liquid phase line,  $C_L$  is the dopant concentration in the melt,  $k_0$  is the equilibrium segregation coefficient,  $k_{eff}$  is the effective segregation coefficient, and  $D$  is the diffusion coefficient of dopants in the melt. Generally, Tiller's model shown in eq. (1) is used to explain constitutional supercooling. The constant parameters  $m$ ,  $k_0$ , and  $D$  are determined by impurities. Therefore, according to these theories, in the case of a crystal with a



higher dopant concentration, a smaller growth rate and a larger temperature gradient are preferred to avoid the occurrence of constitutional supercooling. However, eq. (2) is an improved version of eq. (1), which takes into account the changing dopant concentration in the melt by the segregation during the growth. Since the change in dopant concentration due to segregation becomes more significant with a higher initial melt dopant concentration, it is necessary to clarify the consistency of the two equations for growing heavily doped Si single crystals. In this study, we evaluated the consistency of the two discriminant equations for the occurrence of constitutional supercooling in the growth of heavily B-doped CZ-Si single crystals. The validity of two discriminants is discussed in the light of the results.

### Experimental procedure

A CZ growth furnace was used to grow heavily doped B-doped Si crystals. A quartz crucible with an inner diameter of 120 mm was filled with 1 kg of 11N silicon material and high-purity granular B. The inside of the crucible was filled with an Ar atmosphere at a pressure of 30 Torr before heating to form a melt. The initial B concentration in the melt was  $3 - 5 \times 10^{20} \text{ cm}^{-3}$ , and Si single crystals of approximately 2 inches in diameter were grown using a [001]-oriented seed crystals at a growth rate of approximately 0.6 – 1.4 mm/min. The pulling speed and heater power were varied to maintain the required crystal diameter, and the rotational speed of the crucible and crystal was 10 rpm in opposite directions.

The grown crystals were cut into wafers 1 mm thick along the growth direction. The resistivity along the solidification fraction was measured by the four-probe method and it was converted to B concentration [7]. In addition, selective etching was performed on the wafers using an etchant of HF : HNO<sub>3</sub> : CH<sub>3</sub>COOH = 1 : 4 : 10, and cellular structures due to the occurrence of constitutional supercooling were observed using an optical microscope. Theoretical verification of the constitutional supercooling was performed using the discriminant equations, eqs. (1) and (2), proposed by Tiller [5] and by Hurle [6] respectively, together with the results of temperature distribution numerically analyzed by CGSim [8].

### Results and discussion

When the initial melt B concentrations was  $4 - 5 \times 10^{20} \text{ cm}^{-3}$  in level, habit lines, which indicate a single crystal is growing, disappeared in the middle of the crystals. Figure 1 (a) shows the crystal grown at 1.0 mm/min with an initial melt B concentration of  $4 \times 10^{20} \text{ cm}^{-3}$ . A photograph and an optical microscopic image of wafers cut vertically from grown crystals after selective etching are shown in Figs. 1 (b) and (c), respectively. It was found that a disordered zigzag interface due to the occurrence of constitutional supercooling cloud be seen and the process had finally led to polycrystallization. The B concentration in the crystal at the onset of constitutional supercooling was measured to be  $2.9 \times 10^{20} \text{ cm}^{-3}$ , and a similar value of about  $3 \times 10^{20} \text{ cm}^{-3}$  were obtained in all other grown crystals. The solidification fraction at the onset of constitutional supercooling decreased with increasing the B concentration in the initial melt.

Next, the effective segregation coefficients,  $k_{\text{eff}}$ , of crystals grown with various pulling rate were determined by relationships between the B concentration in the crystal and the solidified fractions using the deformed equation of normal freezing proposed by Pfann [9] as follows,

$$C_s = kC_0(1 - g)^{k_{\text{eff}}-1}, \quad (3)$$

$$\ln(C_S) = (k_{eff} - 1) \ln(1 - g) + \ln kC_0, \quad (4)$$

where  $C_S$  is the dopant concentration in the crystal and  $g$  is the solidified fraction. Figure 2 shows the relationships between B concentration and the solidified fraction of crystals grown at speeds of from 0.6 to 1.4 mm/min. The determined  $k_{eff}$ s were 0.50, 0.52, 0.53 and 0.56 for pulling rates of 0.6, 1.0, 1.2 and 1.4 mm/min, respectively. From these results, the equilibrium segregation coefficient  $k_0$  of B was estimated to be 0.45 from BPS theory [10].

Figs. 3 (a) and (b) show, respectively, the growth model, used in this study, for the two-dimensional axisymmetric steady-state simulation by CGSim [8] and numerically calculated results of temperature distribution in the furnace. From Fig. 3 (b), the temperature gradient in the melt just below the growth interface  $G_L$  was estimated as shown in Fig. 3 (c). The minimum temperature gradient was 2.0 K/cm at the center of the crystal and the maximum was 3.2 K/cm at the periphery. The results obtained show a curve similar to that of the onset of a cellular structure due to the occurrence of constitutional supercooling as shown in Fig. 1 (c), indicating that the constitutional supercooling occurred at the center of the crystal, where the temperature gradient was smallest.

Based on these results, a comparison of the consistency of the two discriminant formulae, eqs (1) and (2), was conducted. First the wafer shown in Fig. 1 (b) was divided into multiple regions and the B concentration in each region were measured, and second,  $C_L$  was calculated from experimental results of  $k_{eff}$ . Third, the values obtained for  $C_L$ ,  $k_0$  and  $G_L$  were substituted in the two equations, and finally the results of applying the discriminant equation to each region were color-coded as red or blue, as shown in Fig. 4. The parameter used in each region was the value at the center of the region, and the B concentration was determined to be the same along the growth direction. Two regions, colored red or blue, represent that constitutional supercooling either occurs or is avoided, respectively using the two theoretical formulae. In the case of Tiller's formula of eq. (1), constitutional supercooling theoretically occurs in the entire wafer, whereas in the case of Hurle's [6] formula of eq. (2), theoretical results were close to the area of actually observed cellular growth. From these results, we conclude that the discriminant formula proposed by Hurle is suitable for judging the occurrence of constitutional supercooling theoretically.

## Conclusion

In this study, Si single crystals with a B concentration of  $10^{20} \text{ cm}^{-3}$  were grown, and sites of the occurrence of constitutional supercooling were investigated experimentally and theoretically. Cellular structures occurring in grown crystals were observed and the effective segregation coefficients of B in crystals grown with several different pulling rates were determined. Using the temperature gradient numerically calculated, constitutional supercooling was verified theoretically using the two discriminants proposed by Tiller [5] and by Hurle [6]. It was found that the theoretical results obtained by Hurle's equation were consistent with experimental results, and it is concluded that Hurle's discriminant equation should be adopted when heavily doped Si single crystals are grown by the CZ method.

## Acknowledgement

The authors wish to thank to Y. Tsukada and Y. Mukaiyama of STR Japan for useful discussions about the numerical simulation and technical support.

## References

- [1] K. M. Kim, J. Electrochem. Soc. 126 (1979) 875.
- [2] T. Taishi, X. Huang, M. Kubota, T. Kajigaya, T. Fukami, K. Hoshikawa, Jpn. J. Appl. Phys. 39 (2000) L5.

[3] T. Taishi, X. Huang, I. Yonenaga, K. Hoshikawa, Mater. Sci. Semicond. Process. 5 (2003) 409.  
 [4] T. Taishi, Y. Ohno, I. Yonenaga, J. Cryst. Growth 393 (2014) 42.  
 [5] W. A. Tiller, Acta Metall. 1 (1953) 428–437.  
 [6] D. T. J. Hurle, Solid-State Electronics 3 (1961) 37–44.  
 [7] H. Kodera, Jpn. J. Appl. Phys. 2 (1963) 212.  
 [8] “CGSim software”, <https://www.semitech.us/>.  
 [9] W. G. Pfann, J. Metals 4 (1952) 747.  
 [10] J. A. Burton, R. C. Prim, W. P. Schlichter, J. Chem. Phys. 21 (1953) 1987.

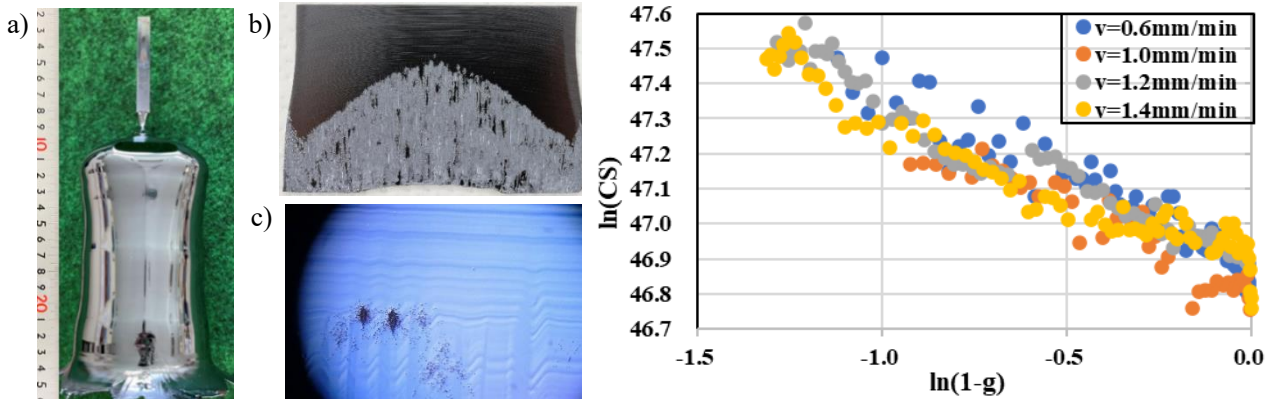


Fig.1 (a) A picture of a B-doped Si crystal, (b) a picture of vertical cut wafer after selective etching and (c) an optical micrograph of a cellular structure where constitutional supercooling occurred.

Fig.2 Relationships between B concentration and solidified fraction of crystals grown at from 0.6 to 1.4 mm/min.

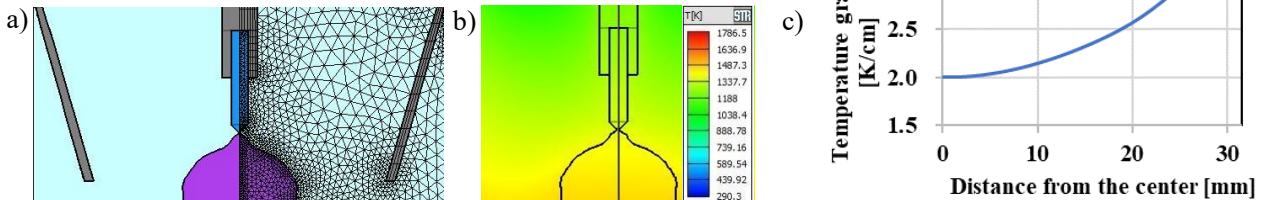


Fig.3. (a) A growth model, used in this study, for the two-dimensional axisymmetric steady-state simulation by CGSim [3] (b) Numerically calculated results of temperature distribution in the furnace. (c) Temperature gradient in the melt just below the growth interface estimated from Fig. 3 (b).

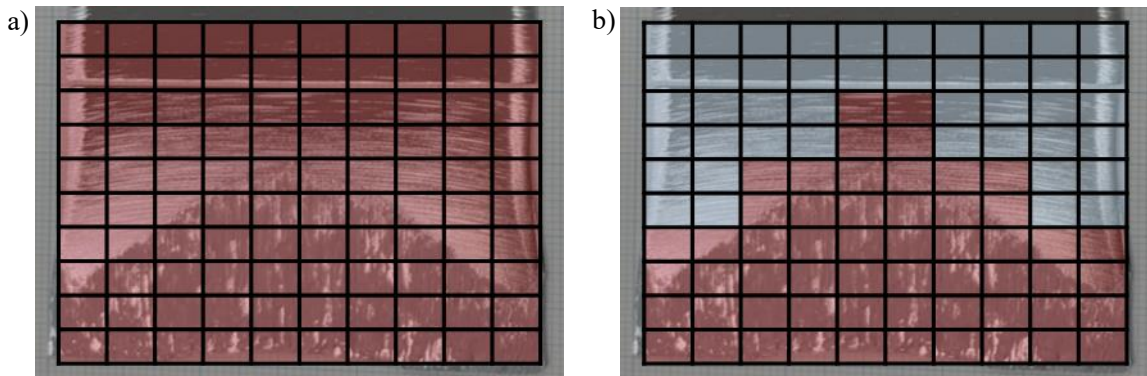


Fig. 4 Discrimination results of occurrence of constitutional supercooling by (a) Tiller's equation and (b) Hurle's equation.

## **A statical study of the effect of interface shape and growth time on dislocation density in multicrystalline Si**

Hiroyuki Tanaka<sup>1\*</sup>, Kentaro Kutsukake<sup>2</sup>, Takuto Kojima<sup>3</sup>, Xin Liu<sup>1</sup>, Noritaka Usami<sup>1</sup>

<sup>1</sup> Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

<sup>2</sup> Center of Advanced Intelligence Project, RIKEN, Nihonbashi, Chuo-ku, Tokyo 103-0027, Japan

<sup>3</sup> Graduate School of Informatics, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan

e-mail: tanaka.hiroyuki.m8@s.mail.nagoya-u.ac.jp

### **Abstract**

There is an implicit understanding that smooth melt-crystal (m-c) interfaces and reduced growth rates during melt growth are effective in reducing dislocation density in Si crystals. However, many previous studies compared the results of changing process conditions, such as heater temperatures, to reduce dislocation density with many constraints coming from the specification of a particular crystal growth furnace. In this study, the relationship between the m-c interface shape, growth rate, and dislocation density is statistically investigated by simulating various temperature distributions without assuming a particular crystal growth furnace. First, we created a silicon-crucible computational geometry assuming an argon atmosphere. Second, we set various time-series temperature boundary conditions around the computational geometry and performed the transient calculations from the crystallization process to the cooling process. Third, from the results of converged simulations, indices for the m-c interface shape, growth time, and dislocation density were calculated to investigate the correlation of each index. We found an apparent correlation between the m-c interface shape and growth time as well as dislocation density. In addition, a weak correlation between the growth time and dislocation density was found, which would be a pseudo-correlation mediated by the m-c interface shape. To confirm the causal relationship between the m-c interface shape and dislocation density, we analyzed the simulation results in detail. As a result, the reduction of the radial temperature gradient near the m-c interface and the low thermal stress was confirmed in the simulation data with a smooth interface shape. This certainly suggests that flattening the m-c interface shape is effective in reducing the dislocation density.

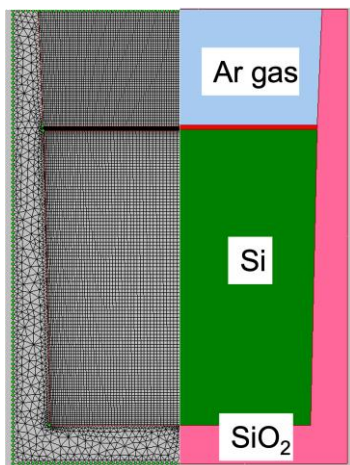
### **Introduction**

Multicrystalline Si, which is used as a base material for solar cells, is industrially produced using the directional solidification (DS) method, in which raw materials are placed in a crucible, heated and melted by a heater, and then the melt is cooled and crystals are grown from the bottom of the crucible to the top. Compared to the Czochralski (CZ) method, which is a method for growing monocrystalline Si, the DS method has the advantages of lower production costs and less scrap material generated during production. On the other hand, the conversion efficiency of multi-crystalline silicon solar cells is inferior to that of monocrystalline silicon solar cells. The reason is that many crystal defects, including dislocations, are introduced during the manufacturing process [1]. Therefore, it is possible to improve the conversion efficiency of solar cells by improving the manufacturing process and reducing the amount of crystal defects. Currently, there are many reports comparing the amount of crystal defects introduced by controlling the temperature distribution during the manufacturing process [2-5]. Among them, it has been suggested that flattening the m-c interface shape during crystal growth and reducing the growth rate are effective in

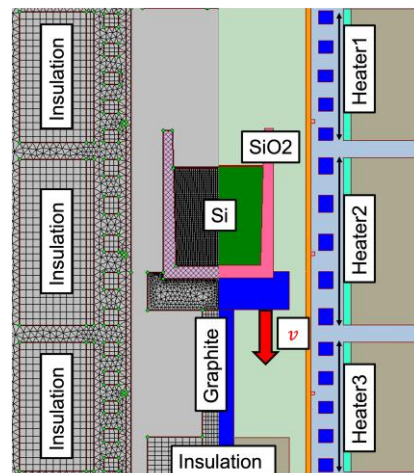
reducing dislocation density [6-7]. However, most of these reports have been compared by changing the temperature field within the constraints caused by the specific furnace structure. In this study, we investigated the relationship between the m-c interface shape, growth rate, and dislocation density in the process under various temperature distributions independent of the furnace structure using crystal growth analysis software.

### Experimental methods

Crystal growth analysis software CGSim (STR) was used for the two-dimensional transient thermo-fluid simulation [8]. The dislocation propagation calculation is based on the Alexander-Haasen model [9]. The equations of mass, momentum, and energy are solved by the finite volume method. The main assumptions of the model are as follows. (1) The Si melt is incompressible, and the Boussinesq assumption is applied. (2) The geometry is modeled as axisymmetric. The model to represent Si in a quartz crucible in an Ar atmosphere is shown in Fig. 1. The geometry is divided into blocks and meshes, which are meshed by structured and unstructured grids. The time series temperatures were given as the boundary conditions on the perimeter of the simulation area for the transient calculations. To verify the validity of the model, we compared the results of the calculation model created in this study (“crucible model”) with that of the “experimental model” to reproduce the whole furnace used in the previous study [2]. Fig. 2 shows the geometry of the experimental model.



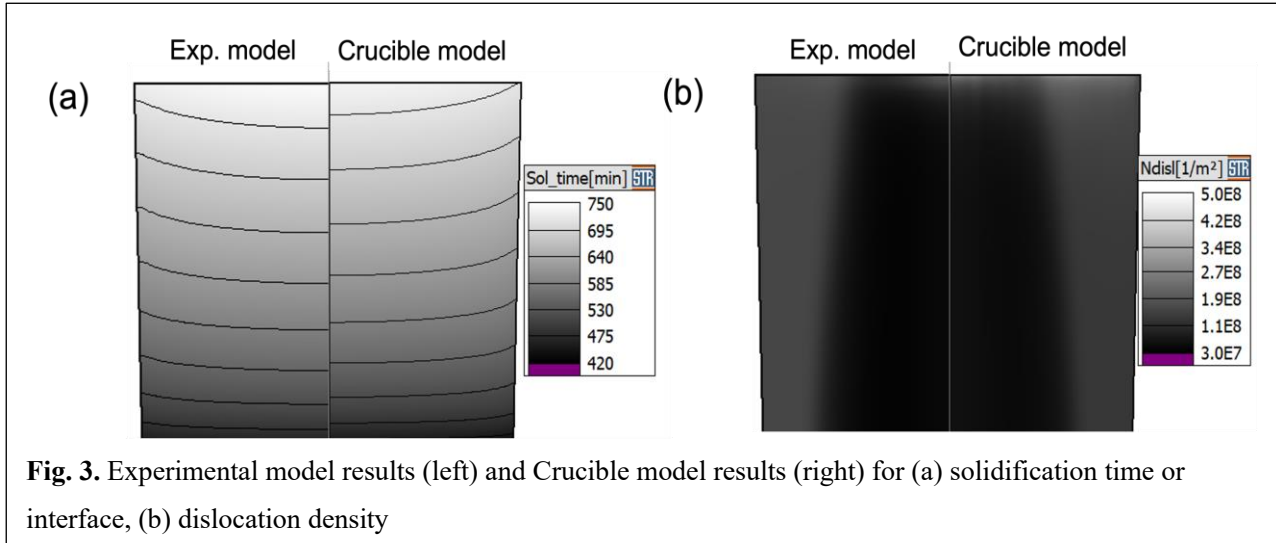
**Fig. 1.** Schematic of crucible model in argon atmosphere and transient global simulations.



**Fig. 2.** Schematic of DS-Si furnace for the growing experiments and transient global simulations.

The specific comparison procedure is described below. First, the transient calculation was performed using the experimental model to obtain the time series temperature distribution around the crucible. Then, the transient calculation was performed using the crucible model with the obtained temperature distribution as the boundary condition. Fig. (3-a) shows a comparison of the crystal growth time distributions. The contour plots correspond to the transition of the m-c interface shape. The time to complete crystal growth was 323.4 minutes for the experimental model, while it was 314.4 minutes for the crucible model with an error of 9.0 minutes. Considering that the time from the melting process to the crystal growth process is approximately 750 minutes, the error is considered small enough. Fig. (3-b) shows a comparison of the dislocation density distribution at the end of the cooling process. It can be confirmed that the results of the crucible model reproduce the characteristics of the experimental model, in which the dislocation density is low in the center of the crystal, and high at the edge and top of the crystal. The results of the transient calculation of the crucible model with time series of temperature boundary conditions on all

four sides of the model are considered to be valid and reliable.



**Fig. 3.** Experimental model results (left) and Crucible model results (right) for (a) solidification time or interface, (b) dislocation density

Using the crucible model, the transient calculations were performed assuming the crystal growth process and the cooling process, with various time-series temperature boundary conditions around the crucible. The melting process was calculated with the temperature around the crucible calculated by the original recipe as the boundary condition. From the crystal growth process to the cooling process, the time-series temperature boundary conditions were randomly given around the crucible and calculated. The method for generating temperature boundary conditions is described below. Firstly, the boundary condition temperatures were randomly generated for selected 13 nodes using a quartic function. The major constraints of quartic functions are as follows: (1) the initial and final temperatures were fixed; (2) the continuity with the melting process; (3) the temperature range. For the temperature range in (3), in addition to the upper and lower limits, we set the lower temperature limit for each node at a specific time. This is to control the temperature gradient in the growth direction, which is characteristic of unidirectional solidification. Then, the temperatures at all boundary nodes were obtained by cubic spline interpolation. From the results of 152 converged simulations, indices for the m-c interface shape, growth time, and dislocation density were calculated. The index for the m-c interface shape,  $h$ , was calculated based on the mean absolute value of the height relative to the ingot center at nine locations at the m-c interface. The growth time,  $t$ , was defined as the time from the start of crystal growth to the complete crystallization of the Si melt and represents the average growth rate. As a measure of the dislocation density, the common logarithm of the average dislocation density at the end of the simulation,  $\log_{10}N$ , was used.

## Results and discussion

A scatter plot matrix (Fig. 4) and a correlation matrix (Fig. 5) using three indices were used to examine the correlation of each index. As can be seen in Fig. 3, there is a clear correlation between the m-c interface shape and the growth time and dislocation density. Furthermore, a weak correlation is found between growth time and dislocation density. This is believed to be a pseudo-correlation mediated by the m-c interface shape.

To confirm the causal relationship between m-c interface shape, dislocation density, and crystal growth time, the simulation results were analyzed in detail. Fig. 6 compares the Von-Mises stress and radial temperature gradient of Si crystals with different interface shapes during the crystal growth process. When the interface shape is flat, the radial temperature gradient near the interface is small and the stress is uniformly distributed. On the other hand,

when the interface shape is concave, the radial temperature gradient is locally higher at the interface curvature, and the stress is also locally higher in some areas.

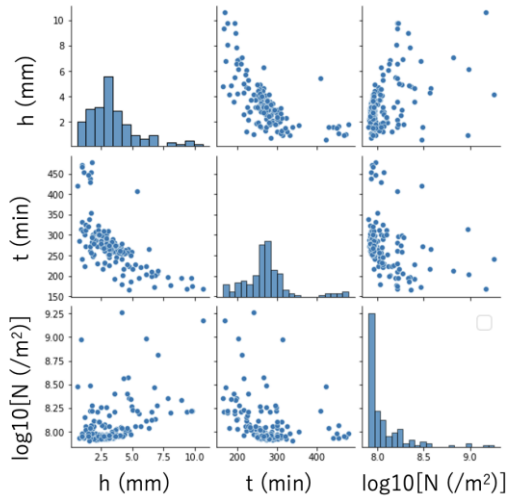


Fig. 4. Scatter plot matrix

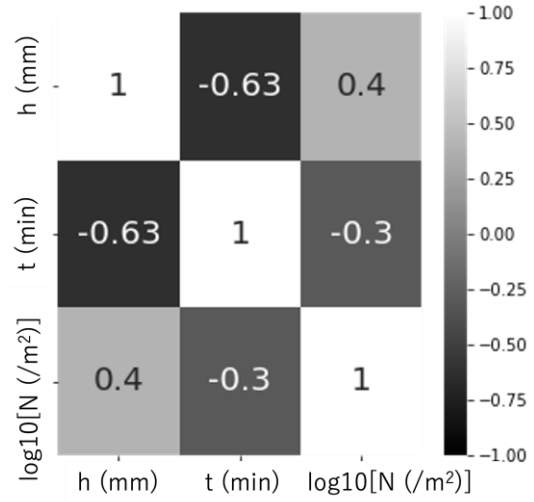


Fig. 5. Correlation matrix

$$\sigma = \alpha E \Delta T \quad (1)$$

Equation (1) describes thermal stress.  $\alpha$  is the coefficient of thermal expansion,  $E$  is Young's modulus, and  $T$  is temperature. From Eq. (1), the thermal stress decreases when the temperature gradient is small. In general, the latent heat of solidification generated at the m-c interface during crystal growth is released through the crucible. Therefore, it is considered that the Si melt near the crucible wall is cooled more easily than that in the center of the crucible, and crystal growth tends to progress earlier.

When the crystal growth progressed with a flat interface shape, the thermal stress on the crystal was decreased by the suppression of the radial temperature gradient, and the amount of dislocation generated was suppressed. From the above, it is considered that a positive correlation between the interface shape and dislocation density appears mediated by the radial temperature gradient. The relationship between the interface geometry and growth time was then investigated.

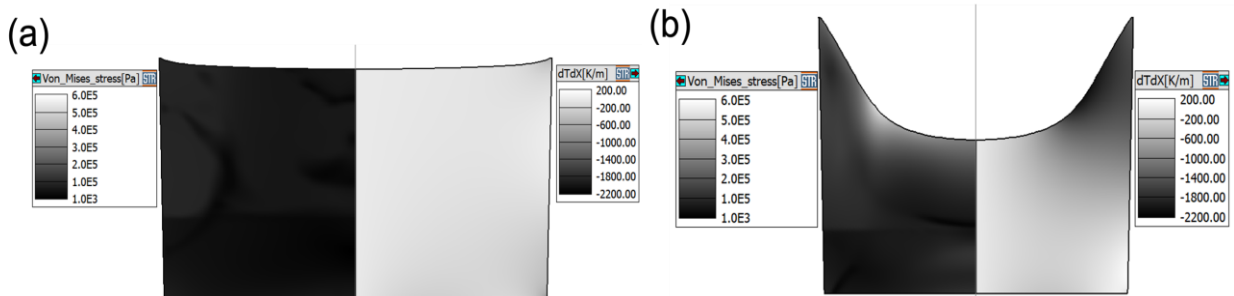


Fig. 6 Comparison of radial temperature gradient and stress distribution due to differences in interface shape (a) The flat interface shape; (b) The convex interface shape

$$-k_m \Delta T_m = -k_c \Delta T_c - \rho_c v_g \Delta H \quad (2)$$

Equation (2) represents the equation for heat transport at the m-c interface, where  $k_m$  is the thermal conductivity of the melt,  $T_m$  is the temperature of the melt,  $k_c$  is the thermal conductivity of the crystal,  $T_c$  is the temperature

of the crystal,  $\rho_c$  is the heat capacity of the crystal,  $v_g$  is the growth rate, and  $\Delta H$  is the freezing enthalpy. The second term in Eq. (2) represents the latent heat of solidification. Eq. (2) shows that the latent heat of solidification is proportional to the growth time. When the growth rate is high, a large amount of latent heat of solidification is generated in a short time, and heat accumulates in the center of the crucible, resulting in a concave shape at the interface. Therefore, it is considered that a negative correlation appears between the growth time, which represents the average growth time, and the interface shape.

## Conclusions

A calculation model of silicon in argon atmosphere-crucible was created, and the validity of the calculation model was evaluated. As a result, it was found that the calculation results obtained by changing the temperature distribution around the crucible using the crucible model were valid and reliable. Then, the correlation between the m-c interface shape, dislocation density, and crystal growth time was statistically investigated by performing transient calculations given various time series of temperature boundary conditions. As a result, it was confirmed that there is a positive correlation between interface shape and dislocation density, and a negative correlation between interface shape and growth time. It was also confirmed that a negative pseudo-correlation appeared between the growth time and the dislocation density. It was suggested that both correlations are strongly influenced by the large amount of latent heat generated during the growth of crystalline silicon. The results statistically confirmed that controlling the crucible wall temperature and suppressing the radial temperature gradient is necessary to grow high-quality crystalline silicon in a short time by DS method.

## Acknowledgement

This work was partly supported by JST/CREST, Grant No. JPMJCR17J1 (2017-2023).

## REFERENCES

- [1] Isao Takahashi *et al*, *J. Cryst. Growth* **312**, 897 (2010).
- [2] Xin Liu *et al.*, *ACS Omega* **7**, 6665 (2022).
- [3] S. G. Nagarajan *et al*, *Silicon* **11**, 603 (2019).
- [4] Aravindan Gurusamy *et al*, *Cryst. Res. Technol.* **56**, 2100018 (2021).
- [5] Natasha Dropka and Martin Holena, *J. Cryst. Growth* **471**, 53 (2017).
- [6] Xi Yang *et al*, *J. Cryst. Growth* **400**, 7, (2014).
- [7] Bei Wu *et al*, *J. Cryst. Growth* **310**, 2178 (2008).
- [8] STR, US. CGSim Theory Manual v. 20; STR IP Holding, LLC:Richmond, VA, USA (2019)
- [9] Satoshi Nakano *et al*, *J. Cryst. Growth* **474**, 130 (2017).



# Formation of microroughness during plasma chemical vaporization machining of silicon wafer and a way to reduce it

Daichi Takeuchi<sup>1\*</sup>, Ryohei Asada<sup>1</sup>, Kazuto Yamauchi<sup>1</sup>, and Yasuhisa Sano<sup>1</sup>

<sup>1</sup>*Graduate School of Engineering, University of Osaka, Yamadaoka Suita Osaka, 565-0871, Japan*

e-mail: [takeuchi@up.prec.eng.osaka-u.ac.jp](mailto:takeuchi@up.prec.eng.osaka-u.ac.jp)

## Abstract

The cause of surface microroughness formation in plasma chemical vaporization machining (PCVM), a highly efficient plasma etching technique, and a method to suppress the formation were investigated. The results of the analysis of the surface after machining showed that the reaction products adsorbed on the surface contributed to the formation of microroughness and that extremely good surface roughness could be obtained by machining while heating the surface above the desorption temperature of the reaction products.

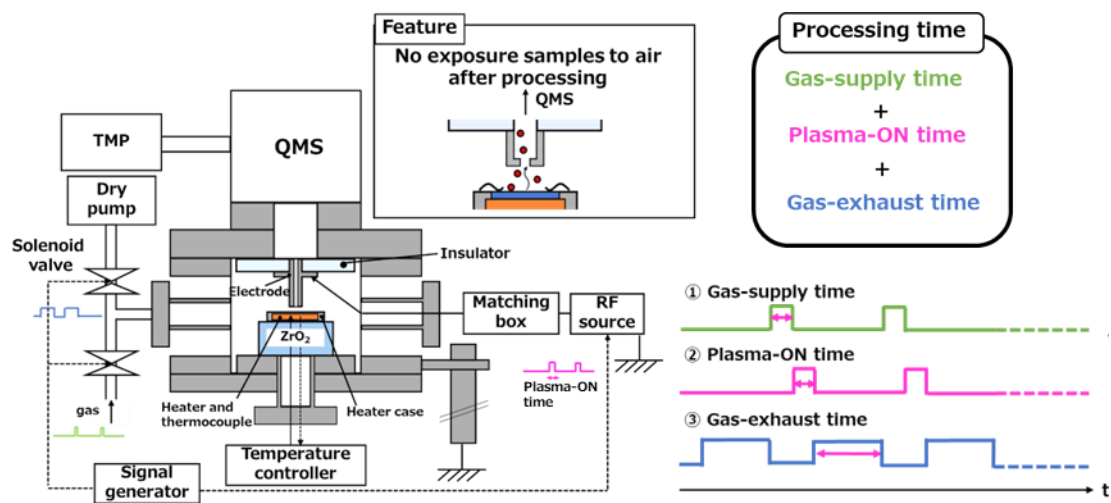
## Introduction

Optical elements and semiconductor substrates with extremely high shape accuracy have been required in the fields of advanced measurement equipment and cutting-edge electronic devices. Optical elements, such as aspherical mirrors for hard X-ray focusing and aspherical mirrors for X-ray telescopes, require nanometer-level shape accuracy. Numerically controlled machining, which performs an arbitrary amount of machining at an arbitrary position based on a pre-measured shape, has been developed as a machining method to achieve high shape accuracy. This method corrects shape errors by scanning a locally-machining head over the entire surface of the workpiece while controlling the scanning speed. However, this method is difficult to apply to the machining of semiconductor substrates that require mass production because it requires a long time to scan the entire workpiece surface with a single machining head. Therefore, instead of scanning the entire surface of the workpiece with a single machining head, we propose a completely new all-in-one numerically controlled machining method in which many processing heads are arranged to cover the entire surface of the workpiece, and the processing time of each processing head is individually controlled [1]. In the batch numerically controlled machining using the plasma chemical vaporization machining (PCVM) method [2], which is an ultra-precision machining method using chemical reactions between radicals in plasma and the workpiece surface, a new high-speed gas displacement machining method was developed to suppress the machining speed distribution in the gas flow direction. To suppress the machining speed distribution in the gas flow direction, a new high-speed gas displacement machining method was devised, and highly efficient numerically controlled machining was successfully achieved [3]. However, machining deteriorated the surface roughness, and its improvement is a challenge. Recently, it has been found that the surface roughness after machining and the concentration of reaction products are correlated. Thus, in this study, we report the results of a detailed investigation of how the concentration of reaction products affects surface roughness.

## Experimental equipment and method

Fig. 1 shows the apparatus used in the experiment. To perform a qualitative spectrometer of reaction products adsorbed on the surface, the electrodes facing the sample were perforated to enable an analysis of gas molecules

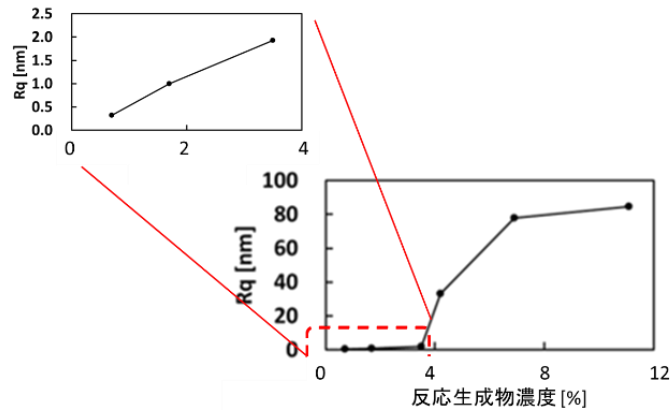
desorbed from the sample surface using a quadrupole mass spectrometer (QMS). The sample table can be heated up to approximately 600 °C using an electric heater, enabling temperature-increased desorption analysis. To perform high-speed gas displacement processing experiments like those in multi-electrode systems, electromagnetic valves for gas supply and exhaust were connected to the system, and the timing of their opening and closing was controlled using a signal generator, as well as the ON time of the RF power supply during one cycle. A silicon substrate was used as the sample, and after cleaning with a sulfuric acid solution, the sample was set and evacuated to perform high-speed gas displacement processing. The amount of machining was evaluated using a white interference microscope, the surface topography was observed using a scanning electron microscope (SEM), and the quantitative evaluation of surface roughness was performed using an atomic force microscope (AFM) to determine the root mean square surface roughness ( $R_q$ ).



**Fig. 1 .** Schematic diagram of plasma processing equipment with thermal desorption analysis function.

### **Relationship between reaction product concentration and surface roughness**

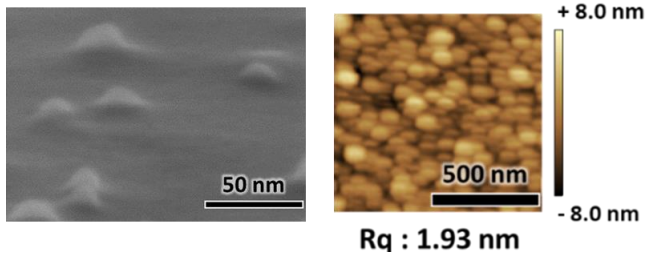
The concentration of reaction products was varied by changing the plasma ON time during one cycle, and the surface roughness after machining was measured (Fig. 2). As the concentration of reaction products increased, the surface roughness became worse, and the roughness changed rapidly after 5%. AFM and SEM measurements of the post-processed surface at high reaction product concentrations revealed micrometer-order deposits on the surface. The mechanism of surface roughness deterioration in the case of a large reaction product concentration was considered to be the adhesion of particles formed by the agglomeration of decomposed reaction products. However, even when the concentration of reaction products was small, the surface roughness worsened as the concentration increased. SEM observation of the surface after processing revealed the formation of microscopic protrusions (Fig. 3), which were determined to be the true cause of the surface microroughness.



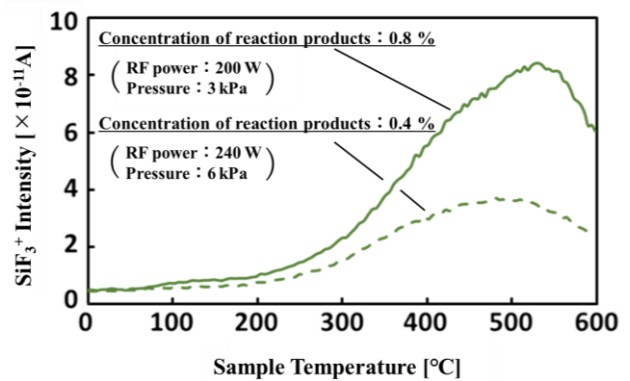
**Fig. 2.** Relationship between reaction product concentration and surface roughness.

### Results of thermal desorption gas analysis

Based on the previous results, we believe that the aggregation of reaction products adsorbed and diffused on the sample surface is a factor in the formation of microroughness. Therefore, we conducted a thermal desorption gas analysis of the sample surface, focusing on  $\text{SiF}_3^+$  as the main peak derived from the reaction products because it is known that more than 90% of the  $\text{SiF}_4$  that reaches the ionization zone of the QMS dissociates to  $\text{SiF}_3^+$ . We conducted a temperature-programmed desorption gas analysis under two conditions with the same processing rate but different reaction product concentrations (Fig. 4). The results show that  $\text{SiF}_3^+$  desorption corresponds to the concentration of reaction products. Therefore, if the number of reaction products adsorbed on the sample surface is reduced, a reduction in microroughness can be expected.



**Fig. 3.** Results of surface topography observation by SEM and AFM (Concentration of reaction products: 4.0 %).

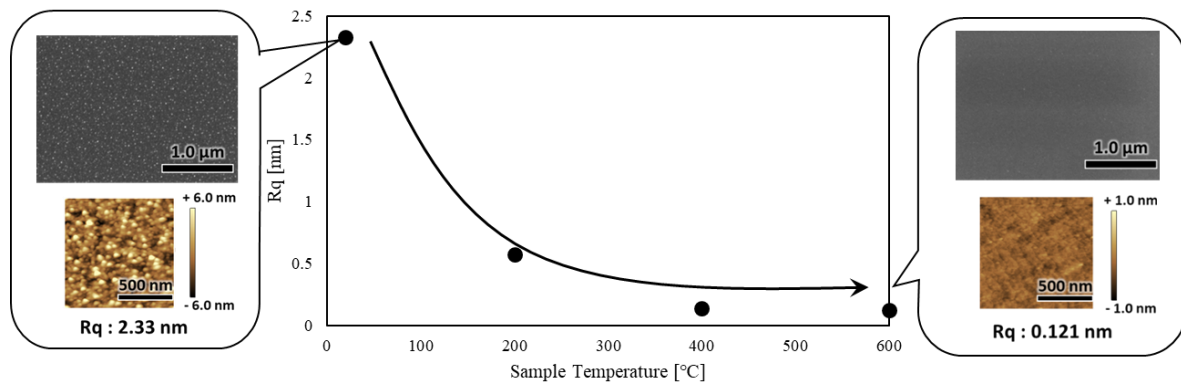


**Fig. 4.** Results of thermal desorption gas analysis  $\text{SiF}_3^+$  of samples with different concentrations of reaction products.

### Roughness evaluation experiment using sample temperature as a parameter

We hypothesized that raising the sample temperature during processing would suppress the adsorption of reaction products and reduce the formation of microroughness. Therefore, we conducted an experiment to evaluate roughness using sample temperature as a parameter. Fig. 5 shows the results of SEM and AFM observations of the processed surface when the sample temperature was varied between 20 °C, 200 °C, 400 °C,

and 600 °C during processing. Fig. 5 shows that the density of microparticles decreased and the Rq value improved as the temperature was increased. At 600 °C, which is above the peak desorption temperature in Fig. 4, the Rq value was 0.121 nm, which is almost the same as that before processing.



**Fig. 5.** Change in surface roughness with increasing processing temperature.

## Conclusions

It was concluded that microroughness formation on the surface after machining in PCVM was caused by the adsorption and aggregation of reaction products generated during the machining of the sample surface. Based on this conclusion, the surface roughness was successfully improved by raising the sample temperature above the temperature at which the gas was desorbed.

## REFERENCES

- [1] H. Takei, S. Kurio, S. Matsuyama, K. Yamauchi, and Y. Sano, *Rev. Sci. Instrum.* 87(2016)105121.
- [2] Y. Mori, K. Yamauchi, K. Ymanaka, and Y. Sano, *Rev. Sci. Instrum.* 71(2000)4627.
- [3] Y. Sano, K. Nishida, R. Asada, S. Okayama, D. Toh, S. Matsuyama, and K. Yamauchi, *Rev. Sci. Instrum.* 92(2021)125107.

## The Study of Dislocation Propagation in Si Wafer during IGBT High Thermal Budget Process

Jiuyang Yuan<sup>1\*</sup>, Yoshiji Miyamura<sup>1</sup>, Satoshi Nakano<sup>1</sup>, Wataru Saito<sup>1</sup>, and Shin-ichi Nishizawa<sup>1</sup>

<sup>1</sup>Research Institute for Applied, Kyushu University, 6-1 Kasuga-koen, Kasuga City, 816-8580, Japan

e-mail: yuan.jiuyang@riam.kyushu-u.ac.jp

### Abstract

There are several thermal budget processes for Si-IGBT fabrication, which sometimes cause dislocation propagation. The dislocation propagation depends on temperature and time of the process. In this paper, we analyzed the dislocation propagation in Si wafer during Si-IGBT fabrication process. We also calculated the dislocation density during diffusion process with several temperatures and times, and we confirmed that the lower temperature process causes the smaller dislocation propagation which may carry out the good device performance.

(Keywords: Si wafer, IGBT fabrication, Diffusion process, Dislocation)

### Introduction

In high thermal budget process of Si-IGBT, such as oxidation, diffusion process as shown in Table. 1 [1], the stress is generated by the temperature distribution inside the wafer, and causes dislocation propagation, which may degrade the performance of power device. The degradation is more pronounced in large diameter Si wafers like 200mm and 300mm processes which for high productivity and low-cost power device. Therefore, it becomes important to suppress the dislocation propagation in Si wafer during high thermal budget process.

In a previous study [2], Sato et al. clarified the relationship between dislocation propagation and the rate of temperature change of ramping up and cooling down processes. They found that controlling the temperature change as a logarithmic function, fast in the low-temperature region, and slow in the high-temperature region, can suppress the dislocation propagation significantly.

In this paper, we first discuss the dislocation density in the Si wafer during the full Si-IGBT fabrication process. Then we discuss the dependence of the dislocation propagation on temperature during diffusion process to conclude that lower temperature process is beneficial for IGBT fabrication.

No.	Thermal process	Condition
1	1 <sup>st</sup> oxidation	Pyro 1100°C 180min
2	GR diffusion	N <sub>2</sub> 1100°C 1300min
3	2 <sup>nd</sup> oxidation	Pyro 1050°C 48min
4	p float	N <sub>2</sub> 1100°C 20min
5	Gate oxidation	Dry 1050°C 16min
6	Poly-oxidation	Dry 1000°C 20min
7	p-base diffusion	N <sub>2</sub> 1050°C 50min

Table. 1 High-temperature Thermal Process for Si-IGBT

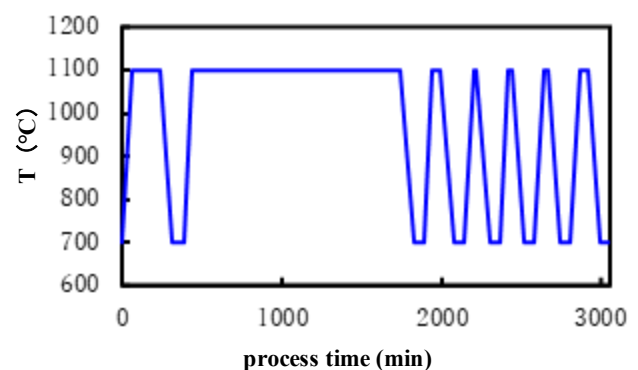


Fig. 1: Temperature profile of IGBT process

## Simulation

First, we simulated the dislocation density of Si wafer in IGBT fabrication process. The dominant thermal processes are listed in Table. 1. In this simulation, we assumed that all thermal process temperature is 1100°C. The temperature profile is shown in Fig. 1. In each process, we set the temperature at the start of heating to 700°C. The rate of ramping up and cooling down are 6.67°C/min and 5°C/min, respectively.

To suppress the dislocation propagation in wafer, we analyzed diffusion process, shown in No.2, 4 and 7 of Table. 1. The profile of the dopant concentration is determined mainly by the temperature and diffusion time. The diffusion length  $L$  (cm) can be expressed as shown in Eq. (1).

$$L = \sqrt{Dt} \quad (1)$$

where  $t$  (s) is the diffusion time,  $D$  (cm<sup>2</sup>/s) is diffusion coefficient and depends on temperature. Fig. 2 shows the relationship between diffusion temperature and diffusion coefficient of boron in silicon. In this simulation, we assume that boron is diffused in n- type wafer.

In this study, we selected the diffusion temperature as 950°C, 1000°C and 1050°C, respectively. First, the diffusion time at 1050°C process is fixed as 1 hour, in which condition the diffusion length is about 1.4μm. And then, we determined the diffusion time for 1000°C and 950°C process, to diffuse boron by the same length in 1050°C process. The diffusion time of 1000°C process and 950°C process were 1 hour 50 minutes and 8 hours 40 minutes, respectively. The temperature profiles of each process are shown in Fig. 3. The temperature at the start of heating was 700°C, and the temperature was raised to the specific diffusion temperature at a rate of 5°C/min, then kept for the required diffusion time, and finally cooled to 700°C at a rate of 2°C/min.

We modeled the vertical thermal furnace by using a commercial software CFD-ACE+ as shown in Fig. 4 [4]. We controlled the wall temperature by the profiles in Fig. 1 and Fig. 3, and calculated temperature difference and stress in the Si wafer.

Then We used the Haasen-Alexander-Sumino (HAS) model to do a three-dimensional numerical analysis of dislocation density based on the result of temperature difference and stress in wafer [2, 5, 6].

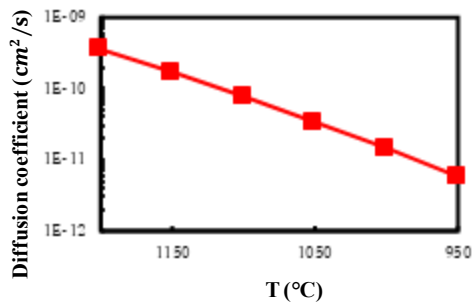


Fig. 2: Temperature dependence of diffusion coefficient of Boron

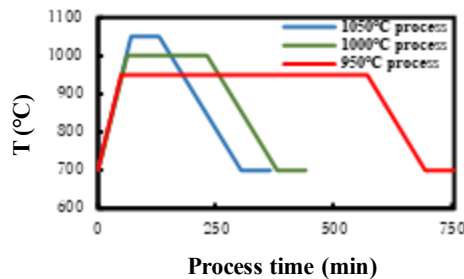


Fig. 3: Diffusion process temperature with process time

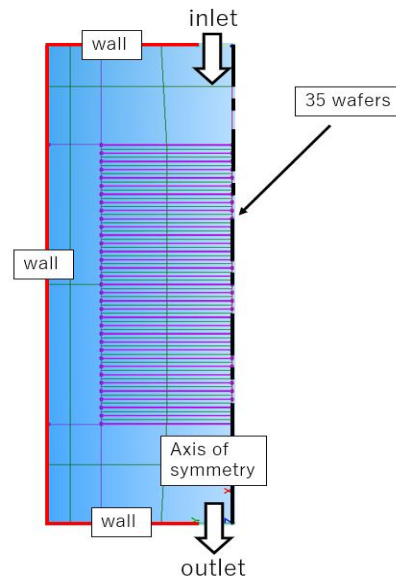


Fig. 4: Model of vertical furnace for 8-inch wafer

## Results and discussion

A large temperature difference as shown in Fig. 5 was observed during ramping up and cooling down processes. The maximum stress in the wafer (shown in Fig. 6) was found to show similar profile to the temperature difference. The stress in Si wafer at the end of the ramping up process ( $t=60\text{min}$ ) as is shown in Fig. 7. The stress in wafer edge is larger than on wafer center. In addition, the stress on front surface is larger at the wafer edge, while the stress on back surface is larger at wafer center. The gravity also affects the stress distribution.

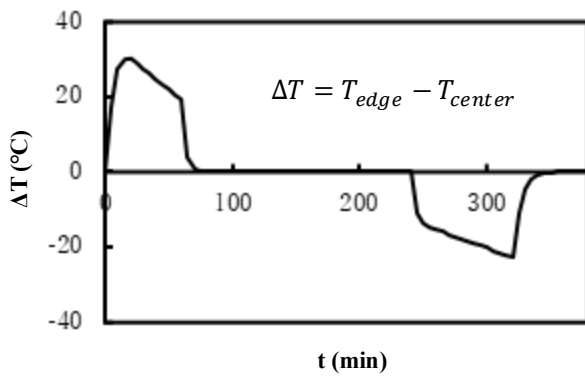


Fig. 5: Temperature difference during first process of IGBT fabrication

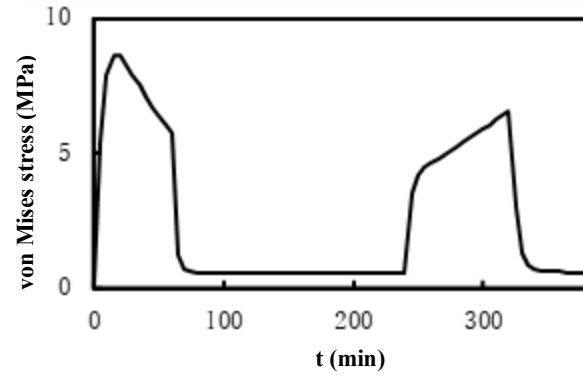


Fig. 6: von Mises stress during first process of IGBT fabrication

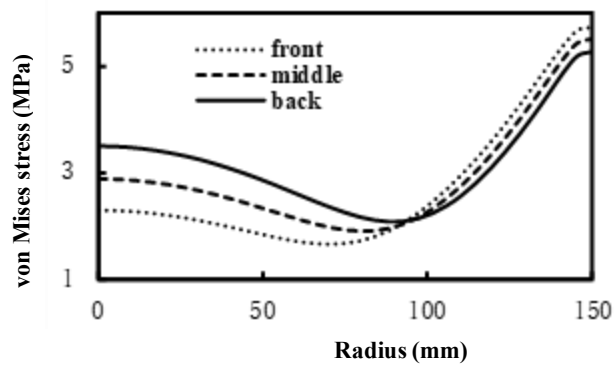


Fig. 7: Von Mises stress distribution in wafer at end of ramping up process

Fig. 8(a) and (b) show the dislocation density during the IGBT fabrication process of Fig. 1 in the wafer center and wafer edge, respectively. We can see that the dislocation density reached about  $10^5$  in the wafer center and  $10^6$  in the wafer edge. About the dislocation density distribution as shown in Fig. 9, we can see that it has almost the same distribution as stress in Fig. 7.

Fig. 10 shows the dislocation density during diffusion process at wafer center. In the higher temperature process, the time of ramping-up step, in which step the delta-T is large and stress is high, is long, as shown in Fig. 11 and 12, and then dislocations propagate widely. Fig. 13 shows the dislocation distribution at the end of diffusion process. We can see the dislocation density after the high temperature process is higher than that after low temperature process, both in wafer center and edge.

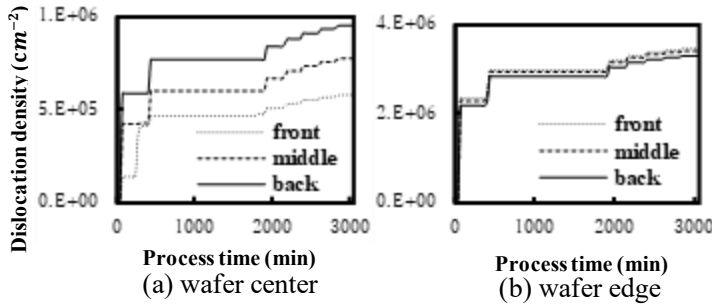


Fig. 8: Dislocation density during IGBT process

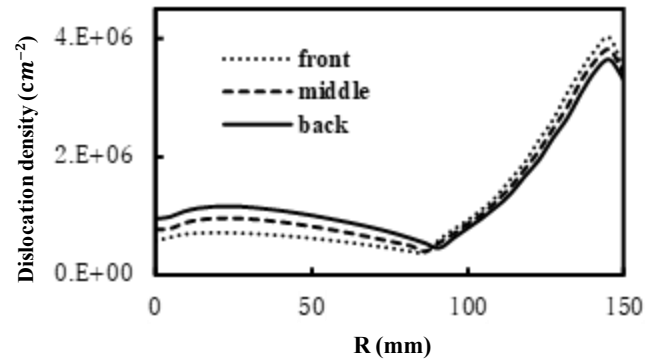


Fig. 9: Dislocation density distribution in radial direction at the end of IGBT process

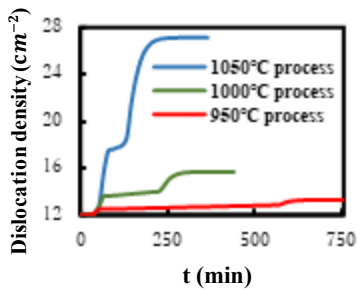


Fig. 10: Dislocation density during diffusion process at the wafer center

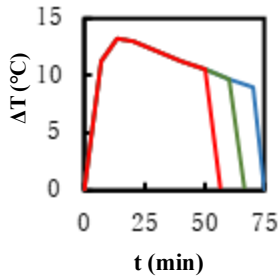


Fig. 11: Temperature difference during ramping up process

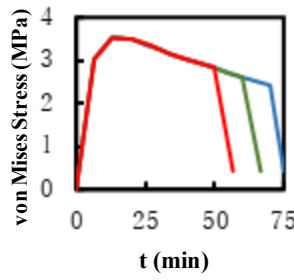


Fig. 12: Wafer stress during ramping up process

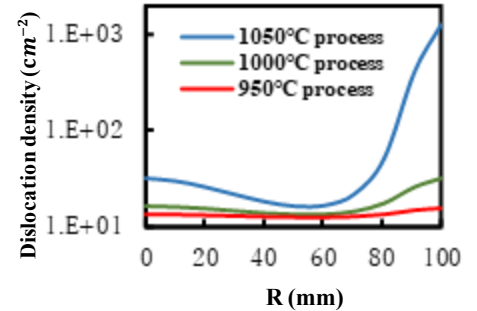


Fig. 13: Dislocation density distribution in radial direction at the end of diffusion process

## Conclusion

We simulated the dislocation density in the wafer during IGBT fabrication process by the HAS model. After the process, dislocation propagation occurred both wafer center and wafer edge.

To suppress the dislocation propagation, we discussed diffusion process among IGBT processes. We analyzed the diffusion temperatures and times, and found that the dislocation density after low temperature process is much lower than that after high temperature process. Therefore, from the viewpoint of crystal engineering, we can conclude that the lower temperature process may improve the performance of power device.

## Acknowledgment

This work was partially supported by NEDO (JPNP21009).

## REFERENCES

- [1] T. Saraya et al., "Demonstration of 1200V Scaled IGBTs Driven by 5V Gate Voltage with Superiorly Low Switching Loss," IEDM), 2018, pp. 8.4.1-8.4.4
- [2] R. Sato, K. Kakimoto, W. Saito and S. -i. Nishizawa, "Dislocation Propagation in Si 300 mm Wafer during High Thermal Budget Process and Its Optimization," ISPSD, 2020, pp. 494-497
- [3] S. M. Sze, "SEMICONDUCTOR DEVICES Physics and Technology", pp. 471-476
- [4] CFD-ACE+ software manual, <https://myesi.esi-group.com/>
- [5] H. Alexander, P. Haasen, "Dislocations and Plastic Flow in the Diamond Structure", Solid State Physics, Volume 22, 1969, pp. 27-158
- [6] B. Gao et al, "Applicability of the three-dimensional Alexander-Haasen mode for the analysis of dislocation distributions in single-crystal silicon", J. Cryst. Growth, 411 (2015) 49–55.



## Evaluation of Crystal Quality by High-Speed, High-Resolution Hybrid X-ray Topography System

Kazuhiko OMOTE\*, Kenta Shimamoto, Yoshinori Ueji, and Keiich Morikawa  
*Rigaku Corporation, 3-9-12 Matsubara-cho, 196-8666, Akishima, Tokyo, Japan*  
e-mail: omote@rigaku.co.jp

### Abstract

We are currently supplying an x-ray topography instrument that can measure high resolution image capable to identify individual dislocations. In addition, it is also possible to take cross-section topography with special resolution of ten to twenty micrometers and construct three-dimensional dislocation images. However, measurement speed of the system is not fast and take long time to measure larger size wafers and rapid scan for the whole wafer is strongly demanded from wafer and device industries. For satisfying such requirements, we have employed photon counting pixel detector with 100  $\mu\text{m}$  pixel size for improving signal to noise ratio and capable to scan whole 300 mm wafer within four minutes. It can detect average dislocation density and/or large size defects. The present hybrid system has both high-speed and high-resolution functions and enable to find defect area first and analyze precisely around there.

### Introduction

Recently, lots of crystalline substrates, such as SiC, GaN, and Ga<sub>2</sub>O<sub>3</sub>, are extensively developed<sup>1)</sup> and quality of the crystals are key for the devices. Even for the Si, since device manufacturing processes are getting complex, dislocation and/or defects are often introduced into the wafer. X-ray topography is one of the powerful techniques to investigate crystal quality, such as dislocation densities, existence of grain boundaries, and so on. In order to investigate individual dislocations precisely, it is required higher spatial-resolution images, typically, 10  $\mu\text{m}$ . We are already supplying a high-resolution X-ray topography instrument for such purpose<sup>2)</sup>. On the other hand, rapid inspection of dislocation arrays and/or large size defects for the whole wafer is also demanded for quality control of product wafers and devices. For those requirements, we have developed a hybrid system, which employs both high-resolution and high-speed detectors. The pixel size of the former is 5.4  $\mu\text{m}$  and 2.4  $\mu\text{m}$ , and that of the later 100  $\mu\text{m}$ .

### High-resolution mode of the topography

By means of the high-resolution detector, the individual dislocations are clearly identified both transmission and reflection geometry as shown in Fig.1 and Fig.2 for SiC bulk crystal and surface epitaxial layer, respectively. The transmission topography (Fig. 1) was measured with Mo  $K\alpha_1$  (0.71  $\text{\AA}$ ) and pixel size of 5.4  $\mu\text{m}$  detector and reflection topography (Fig. 2) was measured with Cu  $K\alpha_1$  (1.54  $\text{\AA}$ ) and pixel size of 2.4  $\mu\text{m}$  detector. In Fig.1, one can distinguish threading screw (TSD, dens dots),

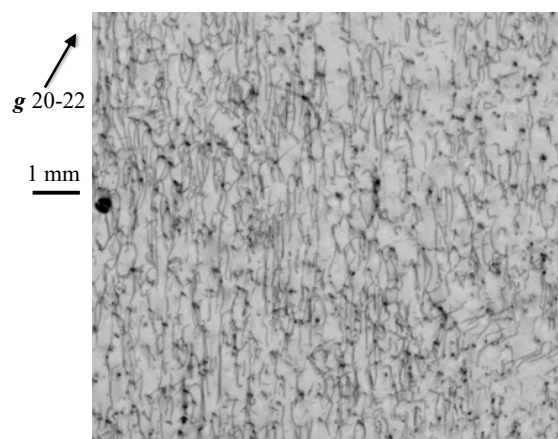
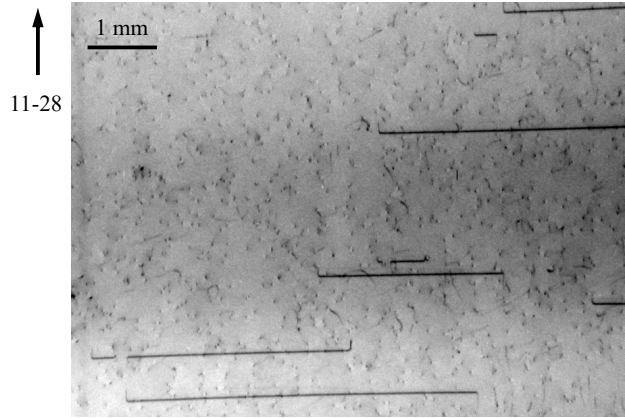


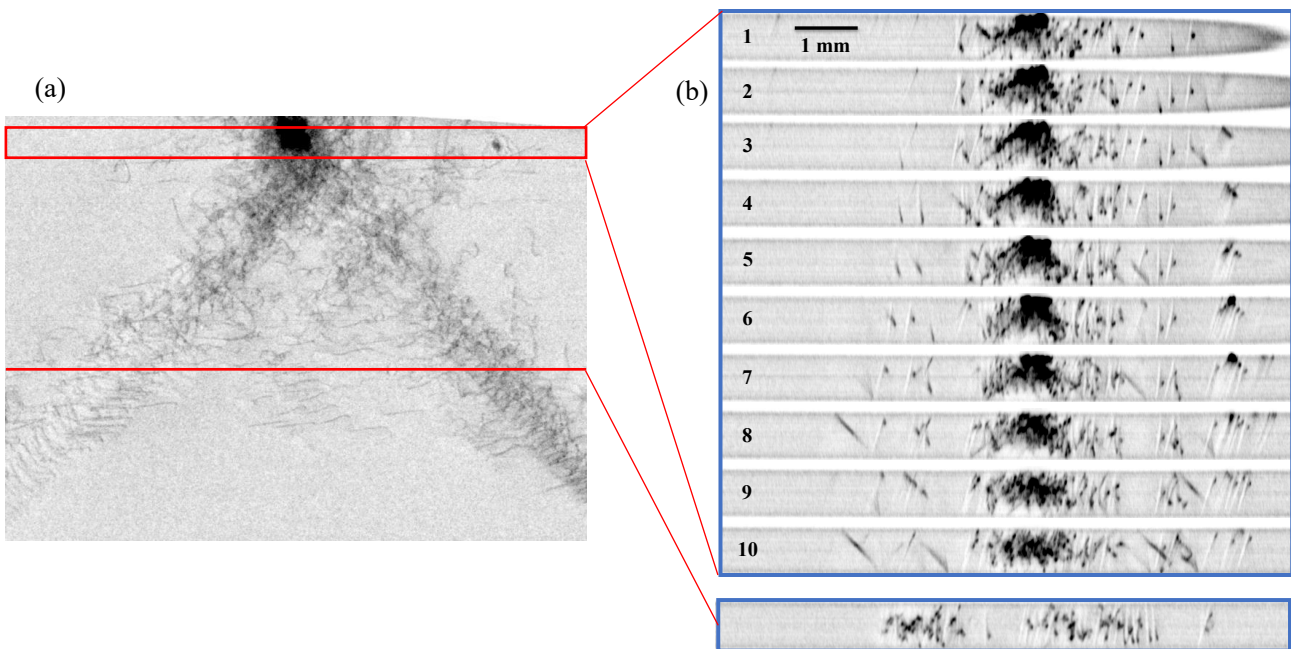
Fig. 1. Transmission topography for 4H SiC.

basal plane (BPD, longer line), and threading edge (TED, shorter line) dislocations. In Fig. 2, one can find mismatch dislocation between bulk crystal with epitaxial layer (long horizontal black line). TSDs are recognized as dot shape and BPD line shape.

We have also introduced three-dimensional dislocation visualization with stacking large amount of section topography images<sup>3</sup>). In the case of conventional traverse topography, all dislocations are overlapped in depth as shown in Fig. 3(a). By employing the section topography with utilizing narrow slit in front of the sample, dislocation images of wafer cross section can be observed shown in Fig. 3(b). We can recognize the origin of the defect is from top surface and created dislocations penetrate to the wafer, then they mainly propagate center of the depth region. It is very powerful tool to investigate where the dislocations are induced and how to propagate inside the crystal.



**Fig. 2.** Reflection topography for epitaxial 4H SiC

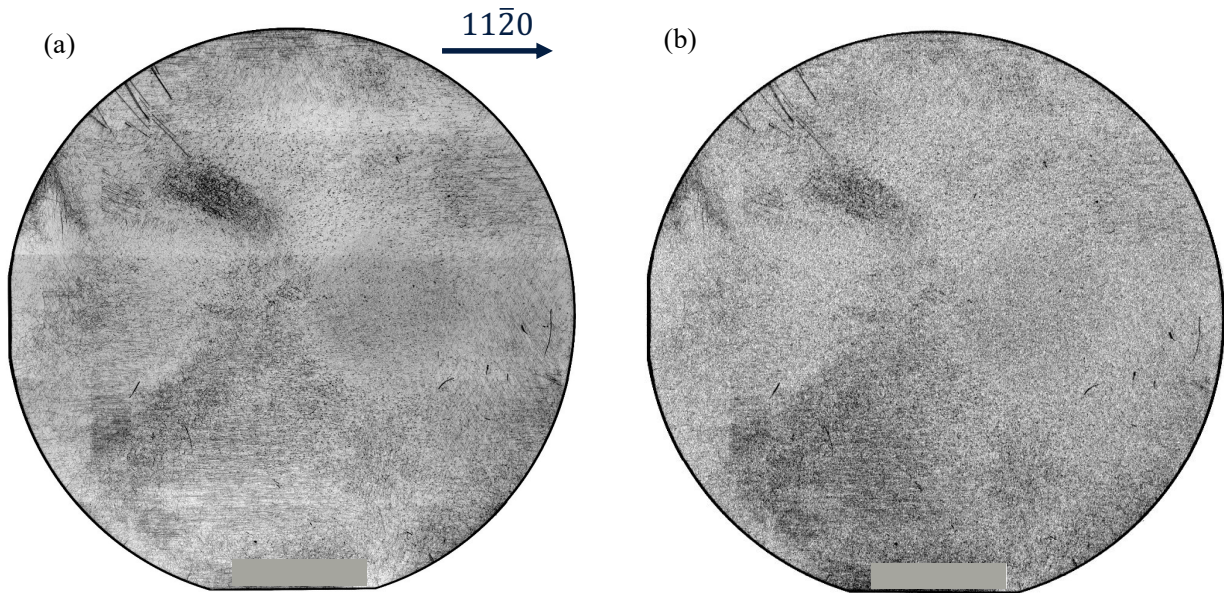


**Fig. 3.** (a) X-ray traverse topography of Si 400 reflection with Mo  $K\alpha_1$ . (b) Section topographies with the same reflection. The first tens are taken at every 50  $\mu\text{m}$  in the red squared region and the position of the last one is indicated by the red line.

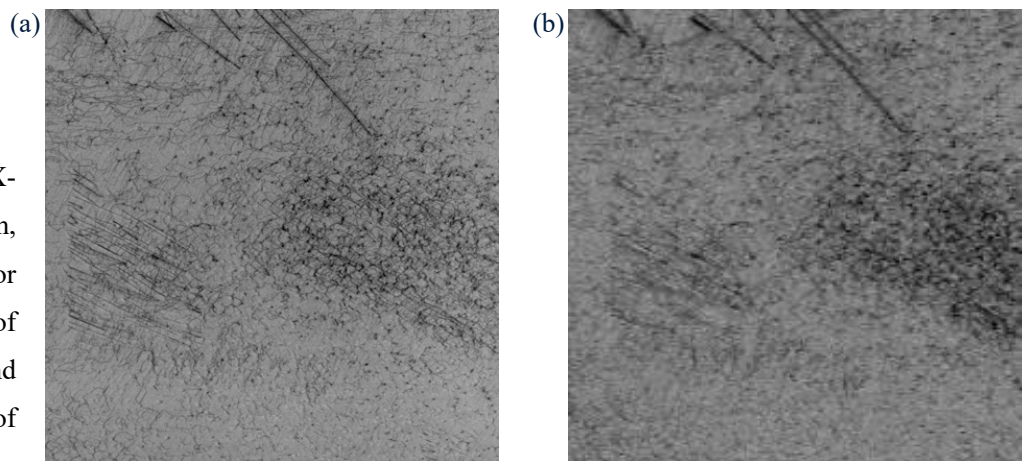
### High-speed mode of the topography

As shown in the previous section, high-resolution topography is suitable for precise investigation for the crystal quality. However, it takes long time for hole wafer scanning, typically one hour for a 300 mm wafer. Then, we have developed high-speed topography for the industry use suited for products control of high-volume manufacturing. For this purpose, we have employed a photon counting pixel detector to maximizing signal to noise ratio. As a results, it is possible to scan the speed of 10 mm/s (600 mm/min) and enable to obtain hole image of 300 mm wafer

within four minutes. Fig.4 shows topography images of 75 mm diameter 4H SiC with Mo  $k\alpha_1$   $11\bar{2}0$  reflection taken by (a) high-resolution and (b) high-speed detectors, those resolutions are 5.4  $\mu\text{m}$  and 100  $\mu\text{m}$  pixel sizes and the acquisition times are 20 min and 1.5 min, respectively. These two images look very similar in this magnification scale, but only high-resolution mode can detect individual dislocations, as shown in Fig. 5. Therefore, high-speed mode is useful for rapid qualification of the crystal and/or to find large size defects. The present hybrid system enables both for fast detection of crystal defects and precise investigation of the detected areas.



**Fig. 4.** Transmission topography for epitaxial 4H SiC with Mo  $K\alpha_1$   $11\bar{2}0$  reflection taken by (a) high-resolution and (b) high-speed detector.



**Fig. 5.** The enlarged images of Fig. 4 (a) and (b).

### Conclusion

We have developed an X-ray topography system, which can be used for both rapid inspection of the product wafers and precise investigation of the individual defects.

It can be useful not

only for precise study of the relation between type of defects with device performances, but also for high-volume manufacturing product control.

### REFERENCES

- [1] H. Tsuchida, I. Kamata, M. Nagano, *J. Crystal Growth*, **306**, 254 (2007).
- [2] K. Omote, *Rigaku Journal*, **29 (1)**, 1 (2013).
- [3] K. Inaba, *Rigaku Journal*, **36 (2)**, 11 (2020).

## A TCAD Simulation Study for a New Technique to Calculate Carrier Recombination Lifetime Based on Open Circuit Voltage Decay Method

Shun Sasaki<sup>1,2\*</sup>, Noritomo Mitsugi<sup>1</sup>, Shuichi Samata<sup>1</sup>, Srikanth Gollapudi<sup>2</sup>, and Ichiro Omura<sup>2</sup>

<sup>1</sup>*SUMCO Corporation, 1-2-1 Shibaura, Minato-ku, Tokyo 105-8634, Japan*

<sup>2</sup>*Kyushu Institute of Technology, 2-4 Hibikino, Wakamatsu-ku, Kitakyushu-shi, 808-0196, Japan*

e-mail: sysasaki@sumcosi.com

### Abstract

A new technique for calculation of correct carrier recombination lifetime in intrinsic layer of silicon PiN diode on the basis of the Open Circuit Voltage Decay method was invented. The new technique can remove the effects of carrier diffusion into p+ and n+ layer from intrinsic layer and carrier injection into intrinsic layer from depletion layer. The comparison of calculation results between the conventional and new technique by employing TCAD simulation indicated that the new technique can calculate more correct recombination lifetime value.

### Introduction

The carrier recombination lifetime is an effective parameter to characterize the purity of semiconductor materials and devices. The Open Circuit Voltage Decay (OCVD) method evaluates the recombination lifetime in the intrinsic layer (i-layer) of PiN diodes. For this advantage, OCVD can be applied to evaluate recombination lifetime in epitaxial layer of silicon epitaxial wafer by employing the epitaxial layer as i-layer of PiN diode [1,2].

In the conventional technique of OCVD, the recombination lifetime values of high and low level injection ( $\tau_{hi}$  and  $\tau_{ll}$ ) [3] are calculated from slope of voltage decay curve which is generated across anode and cathode of a PiN diode after carrier injection, by using equation (1) and (2) [1] :

$$\frac{1}{\tau_{hi}} = -\frac{q}{2kT} \frac{dV}{dt}, \quad (1)$$

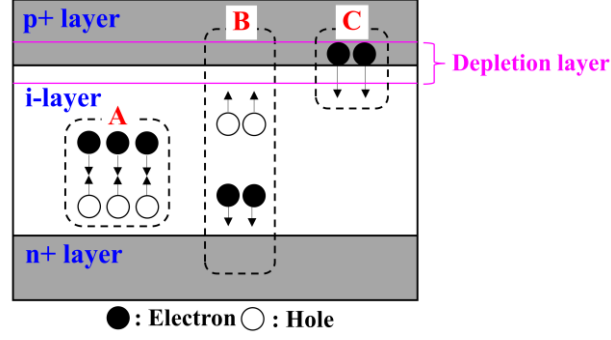
$$\frac{1}{\tau_{ll}} = -\frac{q}{kT} \frac{dV}{dt}, \quad (2)$$

where,  $k$ ,  $T$ ,  $q$ ,  $V$ , and  $t$  are Boltzmann constant, temperature, elementary charge, voltage across anode and cathode of a PiN diode, and time.

However, these equations do not consider the effect of carrier diffusion into p+ and n+ layer from the i-layer and carrier injection into the i-layer from depletion layer of p+ layer that occur during the carrier recombination in the i-layer. In practical, the voltage decay curve contains the effects of the carrier recombination, carrier diffusion, and carrier injection. Figure.1 shows schematic image of the carrier diffusion and injection during carrier recombination. Incidentally, the effect of the carrier diffusion and carrier injection to the voltage decay curve depend on thickness and dopant density of the p+, n+, and i-layer of the PiN diode. For example, the effect of the carrier diffusion and injection becomes strong in a PiN diode which has relatively thinner and lower dopant density of p+ layer. As a results of such effect, the slope of the voltage decay curve of the PiN diode changes in comparison with a PiN diode which has relatively thicker and higher dopant density of p+ layer. Therefore,

calculation results of  $\tau_{hl}$  and  $\tau_{ll}$  by the conventional technique can not compare between two PiN diodes that have different thickness and dopant density of the p+, n+, and i-layer.

To solve this problem, we have invented a new technique for calculation of  $\tau_{hl}$  and  $\tau_{ll}$  which can remove the effects of carrier diffusion and carrier injection. In this study, we simulated the voltage decay curve of the OCVD by employing Technology Computer Aided Design (TCAD) to verify the validity of the new technique.



**Fig. 1.** The schematic image of the carrier diffusion and injection during recombination in i-layer of PiN diode. A: Carrier recombination. B: Carrier diffusion into p+ and n+ layer from i-layer. C: Carrier injection into i-layer from depletion layer.

#### Proposal of the new technique for calculation of recombination lifetime

In the new technique, recombination lifetime values of high and low level injection ( $\tau_{hl}$  and  $\tau_{ll}$ ) [3] are calculated by following equation (3) and (4) :

$$\frac{1}{\tau_{hl}} = -\frac{q}{2kT} \frac{dV}{dt} - \left( \frac{D_p}{L_i N_{n+} L_{n+}} + \frac{D_n}{L_i N_{p+} L_{p+}} \right) n_{s-hl}, \quad (3)$$

$$\frac{1}{\tau_{ll}} = -\frac{q}{kT} \frac{dV}{dt} - \left( \frac{D_p N_i}{L_i N_{n+} L_{n+}} + \frac{D_n N_i}{L_i N_{p+} L_{p+}} \right) + \frac{1}{n_{s-ll} q L_i} \frac{dQ}{dt}, \quad (4)$$

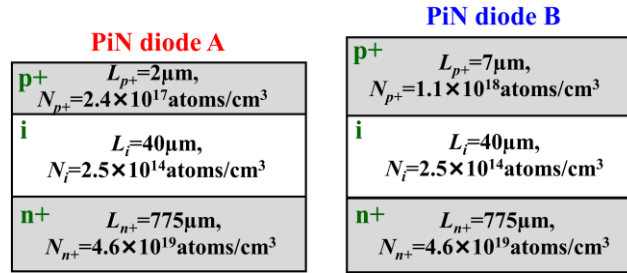
where  $D_p$ ,  $D_n$ ,  $L_i$ ,  $N_i$ ,  $L_{n+}$ ,  $N_{n+}$ ,  $L_{p+}$ ,  $N_{p+}$ ,  $Q$ ,  $n_{s-hl}$ , and  $n_{s-ll}$  are hole diffusion coefficient, electron diffusion coefficient, i-layer thickness, dopant density of i-layer, n+ layer thickness, dopant density of n+ layer, p+ layer thickness, dopant density of p+ layer, area density of injected carrier from depletion region, injected carrier density in high level injection, and injected carrier density in low level injection.

On the right hand of above equations,  $Q$ ,  $n_{s-hl}$ , and  $n_{s-ll}$  can be calculated from ref 1 and 4. As other variables of the right hand of above equations,  $dV/dt$ ,  $L_i$ ,  $N_i$ ,  $L_{n+}$ ,  $N_{n+}$ ,  $L_{p+}$ ,  $N_{p+}$ , and  $T$  can be known from the voltage decay curve, PiN diode structure, and measurement condition.

#### TCAD simulation to verify the validity of the new technique

To verify the validity of the new technique, the voltage decay curves of two silicon PiN diodes that have different thickness and dopant densities of p+ layer were simulated by employing TCAD. Figure.2 shows

schematic cross section of the two silicon PiN diodes structures (PiN diode A and B). The p+ layer of PiN diode A is relatively thinner and lower dopant density than PiN diode B. On the other hand, thicknesses and dopant densities of i-layer and n+ layer are same between PiN diode A and B. Table I shows assumed values of recombination lifetime in i-layer and temperature in the TCAD simulation. Here,  $\tau_n$  and  $\tau_p$  are the recombination lifetime of electron and hole [3]. Incidentally,  $\tau_{hl}$  and  $\tau_{ll}$  are approximated as  $\tau_{hl} \approx \tau_n + \tau_p$  and  $\tau_{ll} \approx \tau_p$  [3]. Thus, same recombination lifetime values of i-layer were assumed to the two PiN diodes in each condition and voltage decay curves were simulated.



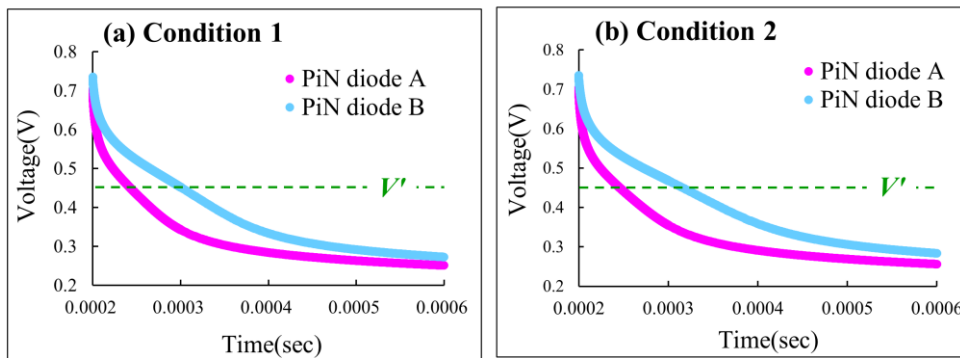
**Fig.2.** The schematic cross section of the two silicon PiN diodes for TCAD simulation.

**Table 1.** The recombination lifetime values of i-layer and temperature for the TCAD simulation.

Condition	Assumed recombination lifetime value of i-layer		Temperature (K)
	$\tau_n$ ( $\mu\text{sec}$ )	$\tau_p$ ( $\mu\text{sec}$ )	
1	55	20	300
2	75	25	300

Figure.3 (a) and (b) show the simulated the voltage decay curves of PiN diode A and B in condition 1 and 2. Apparently, PiN diode A which has relatively thinner and lower dopant density p+ layer shows faster voltage decay due to the effect of carrier diffusion and injection, in spite of same assumed i-layer recombination lifetime values. The  $V'$  which is the boundary of high and low level injection was determined as 0.45V from the change of the slope of voltage decay curves  $dV/dt$  (green dashed line).

The  $\tau_{hl}$  and  $\tau_{ll}$  were calculated from these voltage decay curves by employing the conventional and new technique. Finally, the calculated results of the conventional and new technique were compared to verify the validity of the new technique.



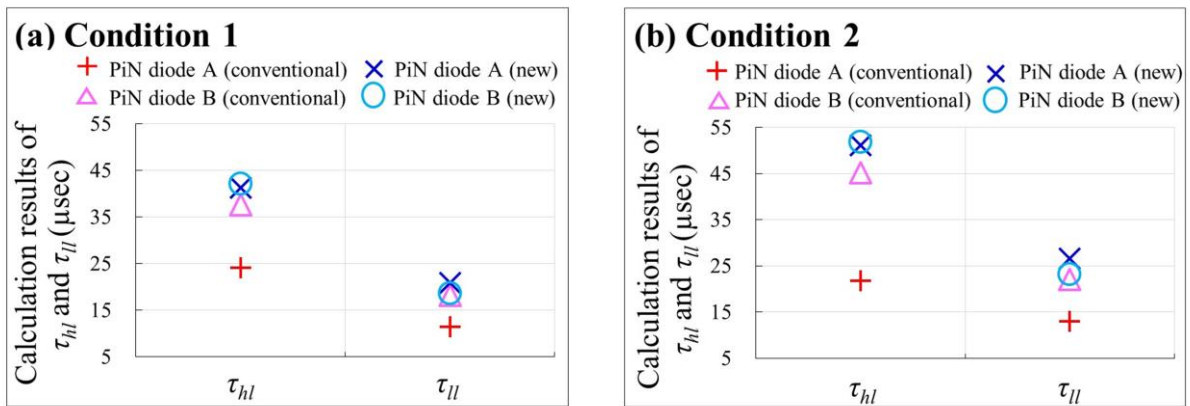
**Fig.3.** The simulation results of voltage decay curve of condition1 (a) and condition 2 (b) in the PiN diode A and B.

## Recombination lifetime calculation and comparison between the conventional and new technique

In the conventional technique, values of  $dV/dt$  were estimated from slope of 0.475-0.45V and 0.45-0.425V in the voltage decay curves of PiN diode A and B, as 0.45V is the boundary of high and low level injection. The values of  $\tau_{hl}$  and  $\tau_{ll}$  by the conventional technique were calculated by substituting the estimated values of  $dV/dt$  into equation (1) and (2). Here, the slope of 0.475-0.45V was substituted into equation (1) and the slope of 0.45-0.425V was substituted into equation (2).

In the new technique, the values of  $dV/dt$  were estimated from same region of the voltage decay with the conventional technique. As mentioned above, the values of  $Q$ ,  $n_{s-hl}$ , and  $n_{s-ll}$  were calculated by employing the equations of ref 1 and 3. The values of  $L_i$ ,  $N_i$ ,  $L_{n+}$ ,  $N_{n+}$ ,  $L_{p+}$ , and  $N_{p+}$  were determined from the structures of PiN diode A and B. The values of  $\tau_{hl}$  and  $\tau_{ll}$  by the new technique were calculated by substituting the these values of into equation (3) and (4).

Figure.4 (a) and (b) are the comparison of the calculation results between conventional and new technique of  $\tau_{hl}$  and  $\tau_{ll}$  in condition 1 and 2. Although same assumed i-layer recombination lifetime values in each condition, the calculation results of the conventional technique are different between the two PiN diodes. This is due to difference of the effect of the carrier diffusion and injection. Thus, the conventional technique can not compare between two PiN diodes that have different thickness and dopant density of the p+, n+, and i-layer, as described in previous section. On the other hand, the calculation results of the new technique are mostly same between the two PiN diodes. This means that the new technique can calculate the correct recombination lifetime of i-layer by removing the effect of the carrier diffusion and injection. Accordingly, it was confirmed that the new technique can calculate more correct recombination lifetime value of i-layer.



**Fig.4.** The calculation results of recombination lifetime by the conventional and new technique in condition 1 and 2.

## Conclusions

A new technique to calculate the carrier recombination lifetime of i-layer of PiN diode on the basis of OCVD method was invented. This technique can calculate recombination lifetime value of i-layer by removing the effect of the carrier diffusion and carrier injection. To verify the validity of this technique, the voltage decay curves of PiN diodes that have same i-layer recombination lifetime and different p+ layer structure were simulated by TCAD. The calculation results of  $\tau_{hl}$  and  $\tau_{ll}$  by employing the new and conventional technique showed that the results of the new technique mostly same values of  $\tau_{hl}$  and  $\tau_{ll}$  in different p+ layer structures of PiN diodes. Therefore, it was confirmed that the new technique can calculate correct recombination lifetime of i-layer.

## REFERENCES

- [1] M. Tapajna, J. Pjenčák, and A. Vrbicky, *Serb. J. Electr. Eng.*, **55**, 239 (2004)
- [2] S. Sasaki, N. Mitsugi, and I. Omura, *Proc. of SSDM*, 727 (2019)
- [3] D.K.Schroder, *IEEE Trans. Electron Devices*, **44**, 16 (1997)
- [4] W. Manabe, *Conference Paper of IEE-SPC*, 7 (2017)



## Analysis of metal gettering in p–n junctions and effect of gettering sites inside Si wafers as starting materials for electronic device processing

Eiji Kamiyama<sup>1,2\*</sup> and Koji Sueoka<sup>2</sup>

<sup>1</sup> Technology, GlobalWafers Japan Co., Ltd., 6-861-5 Higashiko, Seiro, Niigata 957-0197, Japan

<sup>2</sup> Department of Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

e-mail: [Eiji\\_Kamiyama@sas-globalwafers.co.jp](mailto:Eiji_Kamiyama@sas-globalwafers.co.jp) / [ejkamiyama@aol.com](mailto:ejkamiyama@aol.com)

### Abstract

We set a targeted 3d metal atom at specific positions inside a Si cell with a P and/or B atom for ab initio calculation and estimated their binding energies (especially energies in a P/B coexisting cell that describes the depletion layer of p–n junctions). We evaluated the tolerance of each concentration of a contaminated 3d metal atom for generating a leak current, based on their distribution inside p–n junctions. The distribution is determined by using the binding energies with the Hakoniwa method. The tolerances of the Ni/Cu concentrations that contaminated the whole wafer in case of including bulk micro defects inside the wafer as starting material for contamination during device processing are also compared with that in case of p on p<sup>+</sup> epitaxial wafers.

### Introduction

Highly doped parts getter contaminated metal atoms inside Si-based electronic devices during their manufacturing processing. This gettering works particularly well in p<sup>+</sup>–n (or p–n<sup>+</sup>) junctions, which are key parts in various electronic devices. However, few reports have evaluated the effect of gettering based on the highly doped (p<sup>+</sup> or n<sup>+</sup>) parts in a device structure. Therefore, we evaluate this effect and evaluate the tolerance of each concentration of a contaminated 3d metal atom that generate a leak current based on their distribution inside p–n junctions. In addition, the tolerances of Ni/Cu concentrations that contaminated the whole wafer in case of including bulk micro defects (BMDs) inside the wafer as starting material for contamination during device processing are also compared with that in case of p on p<sup>+</sup> epitaxial wafers using the newly reported binding energy values of a Ni/Cu atom near SiO<sub>2</sub>/Si interfaces [1].

### Calculation details

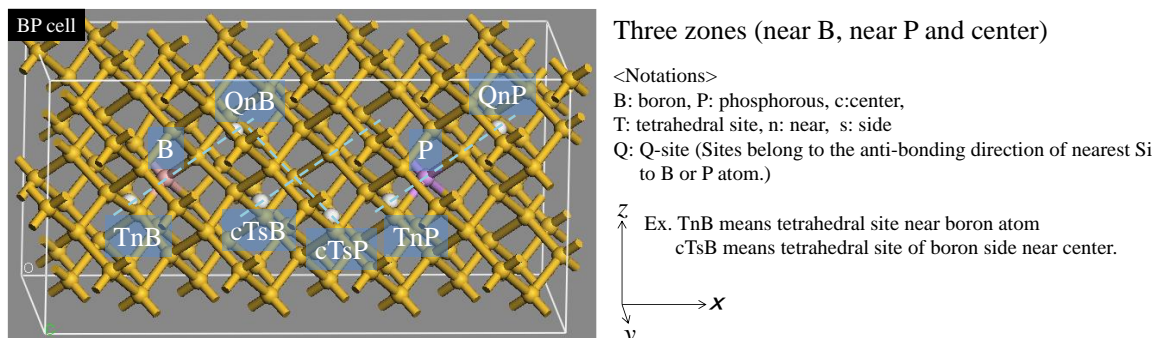
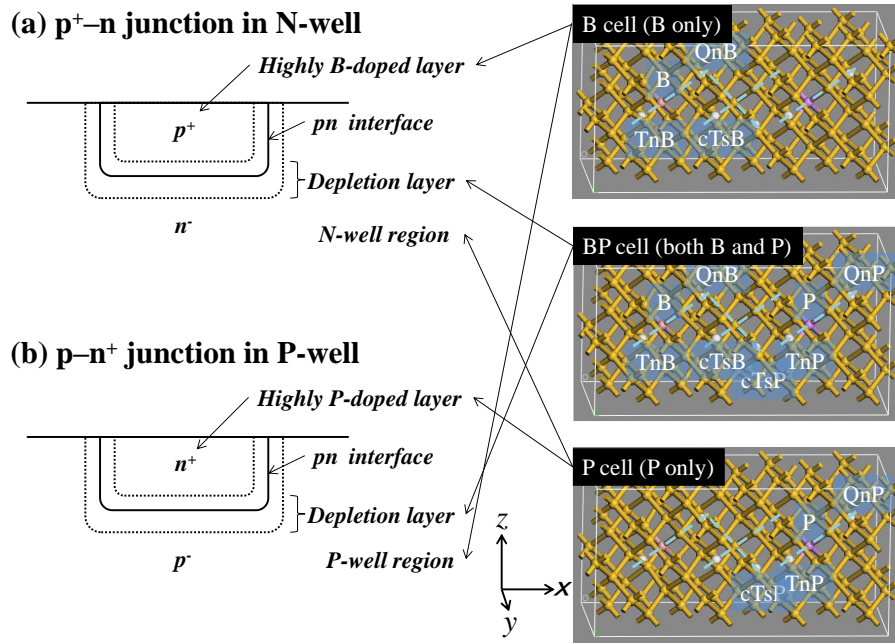


Fig. 1. Models and specific sites for ab initio calculation to describe specific parts of p–n junction [2].

The typical atomistic model (BP cell) used in this study is shown in Fig. 1 to describe depletion layer of a p–n junction in which concentrations of B/P are almost equal [2]. The specific sites for a contaminated metal atom are also shown in Fig. 1. Figure 2 shows that each type of junction is divided into three parts that correspond to atomistic models [2]. We set a targeted 3d metal atom at specific positions and calculate the total energy to estimate binding energies. We evaluate the tolerance of each concentration of a contaminated 3d metal atom for generating a leak current of p–n junctions [2] using the binding energies with the Hakoniwa method [3]. The Hakoniwa method is based on ab initio calculations and thermal statistics and is used to solve many gettering issues [4].

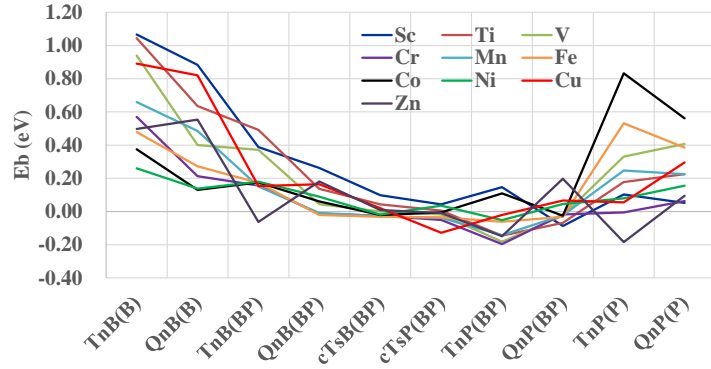


**Fig. 2.** Basic concept of relation between parts of junctions and atomistic models [2].

All calculations by ab initio in this paper were based on the local density approximation [5, 6] using the ultra-soft pseudopotential method [7] and the plane waves as a basis set for efficient structure optimization. The expression proposed by Perdew, et.al. [8] was used for the exchange-correlation energy in the generalized gradient approximation (GGA). The *CASTEP* code was used to solve the Kohn-Sham equation self-consistently with the three-dimensional periodic boundary condition [9]. The density mixing method [10] and *Broyden–Fletcher–Goldfarb–Shanno* (BFGS) geometry optimization method [11] were used to optimize atomic configurations. Only the neutral charge state of the systems was considered in this study. The calculations were performed for the system at a temperature of absolute zero. Additionally, k-point sampling was set at  $1 \times 2 \times 2$  special points of the Monkhorst–Pack grid [12]. The cutoff energy of the plane waves was set to 500 eV.

### Calculated results I. Binding energies

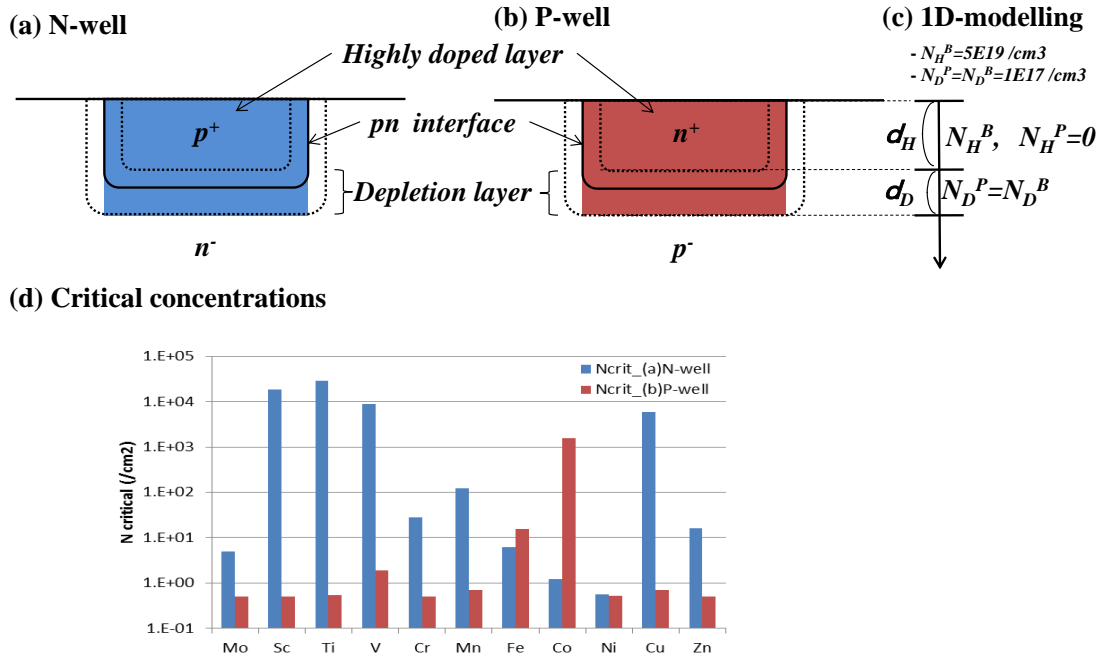
Figure 3 shows the calculated binding energies of each metal atom and each position. Metal atoms in B cells have higher binding energy than that in P cells except some metal atoms (Co and Fe). Metal atoms in BP cells have the lowest binding energy, which is useful for devices with p<sup>+</sup>–n (p–n<sup>+</sup>) junctions. In the next section, we evaluate the relative tolerance for contamination of each 3d metal atom using these binding energies.



**Fig. 3.** Calculated binding energies of each metal atom and each position (also see notations in Fig.1) [2].

### Calculated results II. Critical contamination concentrations of 3d metal atom in p-n junctions

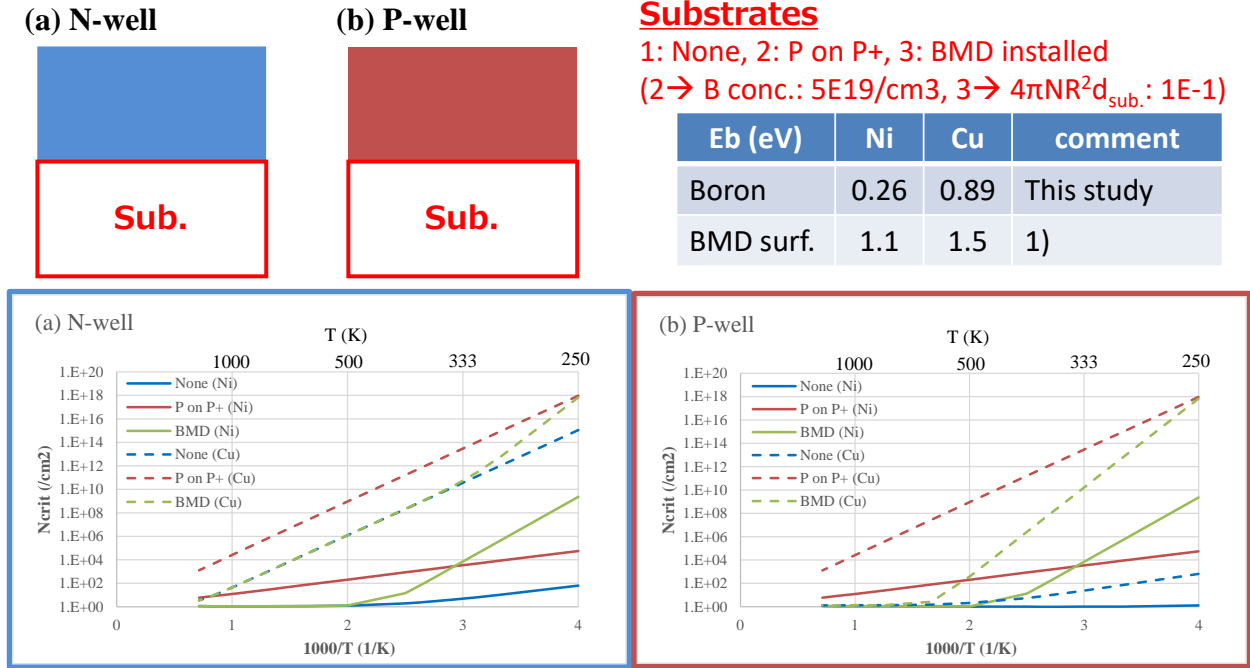
To evaluate the tolerance of the contamination, we estimate the critical contamination concentrations of each 3d metal atom under the following three assumptions. First, contaminating metal atoms only come from the surface. Second, any structures of the well region and underneath it (i.e., any structures of substrates) are ignored except the p-n junction as shown in Fig. 3(a)–(c). Third, the distribution of metal atoms should thermal-statistically obey binding energies. An example of this would be applying the Hakoniwa method [2, 3] and calculating the existence probability of the metal atoms in the depletion layer  $p$ . The critical concentration  $N_{critical}$  is defined by the amount of contaminating metals  $N_{contami}$  (/cm<sup>2</sup>) when the mean number of metal atoms is 0.5 counts/per unit area (1 cm<sup>2</sup>) in the depletion layer (i.e.,  $N_{contami} \times p = 0.5$ ) based on thermal equilibrium. Figure 4(d) is an example of calculated  $N_{critical}$  when  $N_H = 5E19/cm^3$ ,  $N_D^P = N_D^B = 1E17/cm^3$ ,  $d_D = 200$  nm (reverse bias~ 2 V),  $d_H = 800$  nm, and  $T = 700$  K.



**Fig. 4** Schematic cross section of p-n junctions in (a) N-well and (b) P-well. (c) 1D modelling for p-n junctions corresponding to (a) and (b). (d) Example of calculated critical concentrations of contaminated 3d metals [2].

### Calculated results III. Critical contamination concentrations of Ni/Cu atom in whole wafer with BMD or highly doped B atoms installed

We analyze the whole wafer by adding the contribution from the substrate as a gettering zone like in Fig. 5. In Fig. 5, parameters describing doped boron atoms and BMD are also shown, and others are the same as those in Fig. 4(d). Here, the density of gettering sites is assumed to exist one per 1.16 nm<sup>2</sup> of the BMD surface, whose area is cited from the Si/SiO<sub>2</sub> interface area of the 2×2×1 model in the reference [1].



**Fig. 5 Effect of substrate (with BMD or highly doped B atoms) on calculated temperature dependence of critical concentrations of Ni/Cu atoms (used parameters are also included).**

Critical concentrations of Cu atoms with junctions in the N-well are higher due to the highly boron-doped layer (p<sup>+</sup>) inside p–n junctions from the higher temperature. Critical concentrations of Cu atoms with junctions in the P-well and substrates also show moderate values due to the gettering at the substrates. Conversely, critical concentrations of Ni atoms are not as high as that of Cu atoms. However, this value significantly recovers when BMDs are installed into the substrate and the temperature drops below 340 K.

### Summary

We analyzed contaminated metal atom behaviors inside Si wafers, focusing on p–n junctions with highly doped P or B layers. We modeled p–n junctions by dividing them into three parts and used ab initio calculations to evaluate the binding energies of the metal atoms contaminated in corresponding cells. Ab initio calculations showed smaller binding energies in cells corresponding to the depletion layers, which is useful for devices with p<sup>+</sup>–n (p–n<sup>+</sup>) junctions. We estimated critical concentrations of contaminated metal atoms using the Hakoniwa method. We analyzed the whole wafer by adding contributions from the substrate as a gettering zone that has highly doped B atoms or BMD in the same manner. Both gettering zones work well for Cu atoms, but Ni atoms only show a higher critical concentration when BMDs are installed into the substrate and the temperature drops below 340 K.

## Acknowledgements

We thank Dr. Hiroki Nagakura of Sony Semiconductor Manufacturing Corporation for discussions on the behaviors of oxygen and metal atoms near oxidizing Si/SiO<sub>2</sub> interfaces and p–n junctions.

## REFERENCES

- [1] H. Nagakura, K. Sueoka, and E. Kamiyama, *ECS J. Solid State Sci. Technol.*, **10**, 123003 (2021).
- [2] E. Kamiyama, H. Nagakura, and K. Sueoka, *The 81th JSAP Autumn Meeting*, 11p-Z12-13 (2020) [In Japanese].
- [3] E. Kamiyama et al., *Materials Science in Semiconductor Processing*, **43**, 209 (2016); E. Kamiyama and K. Sueoka, *ECS Trans.* **102**, 39 (2021).
- [4] E. Kamiyama et al., *ECS J. Solid State Science and Technology*, **4**, P232 (2015); *ibid.* **5**, X1 (2015); E. Kamiyama et al., *Phys. Status Solidi (c)*, **13**, 746 (2016); A. Yamada and K. Sueoka, *ECS J. Solid State Science and Technology*, **6**, P125 (2017); K. Toyosaki and K. Sueoka, *ECS J. Solid State Science and Technology*, **6**, P326 (2017); K. Tadano and K. Sueoka, *Materials Science in Semiconductor Processing*, **63**, 45 (2017).
- [5] P. Hohenberg and W. Kohn, *Phys. Rev.* **136** (1964) B864.
- [6] W. Kohn and L. Sham, *Phys. Rev.* **140** (1965) A1133.
- [7] D. Vanderbilt, *Phys. Rev. B* **41** (1990) 7892.
- [8] J.P. Perdew et.al. *Phys. Rev. Lett.*, **77**, 3865 (1996).
- [9] The *CASTEP* code is available from *Dassault Systèmes, Biovia Inc.*
- [10] G. Kresse and J. Furthmuller, *Phys. Rev. B* **54** (1996) 11169.
- [11] T. Fischer and J. Almlof, *J. Phys. Chem.* **96** (1992) 9768.
- [12] H. Monkhorst and J. Pack, *Phys. Rev. B* **13** (1976) 5188.

## Properties of a Nickel-Related Electronic Level in Solar-Grade Polysilicon Crystals

Yuito Terada<sup>1\*</sup>, Yoshifumi Yamashita<sup>2</sup>, Hiroo Suzuki<sup>2</sup>, Takeshi Nishikawa<sup>2</sup>, Yasuhiko Hayashi<sup>2</sup>

<sup>1</sup>*Graduate School of Natural Science and Technology, Okayama University, 3-1-1, Tsushima-naka, Kita-ku, Okayama 700-8530, Japan*

<sup>2</sup>*Natural Science and Technology, Institute of Academic and Research, Okayama University, 3-1-1, Tsushima-naka, Kita-ku, Okayama 700-8530, Japan*

E-mail: psp39kuh@s.okayama-u.ac.jp

### Abstract

We investigated the stability of nickel-related levels in polycrystalline silicon for solar cells using isothermal deep-level transient spectroscopy. The level we focused on became unstable and disappeared when a reverse bias voltage was applied to the Schottky electrode below room temperature. By performing isothermal annealing experiments, we found that this phenomenon can be explained by a two-state model, and the energy barrier of annihilation at a bias voltage of  $-2$  V was 0.63 eV.

### Introduction

Polycrystalline silicon is a useful material for solar cells because of its relatively high power-generation efficiency and low production cost. Metallic impurities that accumulate on grain boundaries (GBs) in polycrystalline silicon form gap levels and act as recombination centers for photocarriers, reducing the efficiency of power generation [1]. Copper (Cu) and nickel (Ni) are examples of such materials [2], and studying the properties of these impurity levels on GBs is important for improving the efficiency. We previously reported the disappearance of Cu-related levels on GBs when the Schottky electrode for deep-level transient spectroscopy (DLTS) was reverse biased and recovered with zero bias [3, 4]. We investigated this effect using isothermal DLTS (IT-DLTS), which can be performed at a constant temperature lower than that of DLTS measurement, during which the levels decrease owing to the effect itself. We found that the same effect is also observed for Ni-related levels; however, we were unable to detect them as a single level in many cases, likely because they were located on GBs. In this paper, we report our success in obtaining a near single peak in IT-DLTS from a sample and extracting a single level. Then, we present the quantitative analysis results of the annihilation process of this level under reverse bias via isothermal annealing.

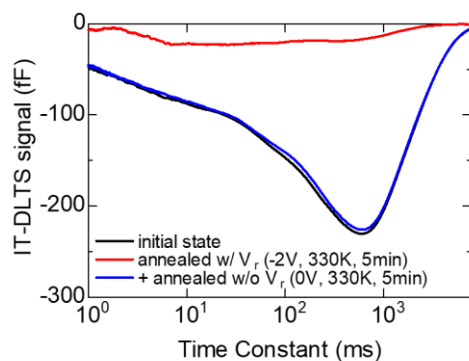
### Experimental

The crystals used were commercially available *p*-type polycrystalline silicon wafers for solar cells (0.5–3  $\Omega\text{cm}$ ), which were cut into several millimeter-square samples. After etching the surface with a mixture of hydrofluoric acid and nitric acid (1:3), an Ni nitrate solution ( $[\text{Ni}] = 300$  ppm) was dropped onto the sample surface and annealed at 600  $^{\circ}\text{C}$  for 1 h to intentionally introduce Ni into the sample. The top surface oxide was then removed with hydrofluoric acid, and titanium was vacuum deposited over several GBs using a transparent mask with a hole in the cover glass to form a Schottky electrode. An ohmic electrode was attached to the back

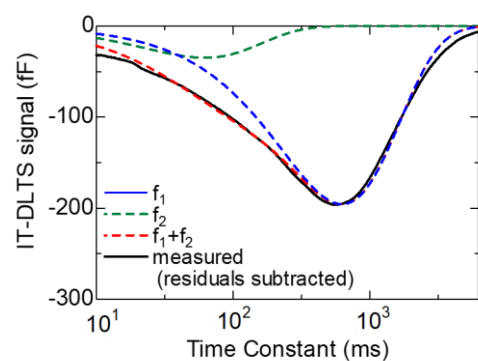
surface of the sample by discharge welding a gallium-doped gold wire, and the sample was evaluated using IT-DLTS measurement [5, 6] with a reverse bias of  $-2$  V at 230 K. As mentioned above, the reverse bias effect restores the level concentration via annealing at approximately room temperature without bias-voltage application, and we confirmed that once the level was annihilated, annealing at 330 K for 5 min without bias voltage restored the peak to almost the same intensity as before annihilation annealing. Therefore, we performed all isothermal annealing experiments using one sample and initialized the peak via zero-bias annealing under the above conditions after annihilating the peak via reverse-bias annealing.

## Results and discussions

The black line in Fig. 1 is an IT-DLTS spectrum of the electronic levels detected in an intentionally Ni-contaminated sample. This peak exhibited the same “reverse bias effect” observed for Cu. The peak disappeared when a reverse bias of  $-2$  V was applied to the Schottky electrode at 330 K (red line in Fig. 1) then recovered to its original intensity when the voltage was removed (blue line in Fig. 1). All results report in this paper relate to this peak. The signal remaining after annihilation annealing at  $-2$  V (red spectrum in Fig. 1) was almost the same whether the temperature was raised to 350 K or the annealing duration was prolonged to 240 min at 330 K. Based on this, we considered this residual signal to be of a different origin from what we were interested in. The black line in Fig. 2 is the spectrum with the residual signal subtracted. Even if we considered the IT-DLTS function to be asymmetric, this spectrum had a slightly large left tail. This spectrum was fitted well by two IT-DLTS peaks ( $f_1$  and  $f_2$  in Fig. 2); therefore, we adopted the following procedure: We subtracted the common residual signal from the measured spectra, separated them into two peaks via fitting, and then focused on the main peak at approximately 700 ms ( $f_1$  in Fig. 2).



**Fig. 1.** IT-DLTS spectra from an Ni-contaminated sample, which exhibits the “reverse bias effect.”

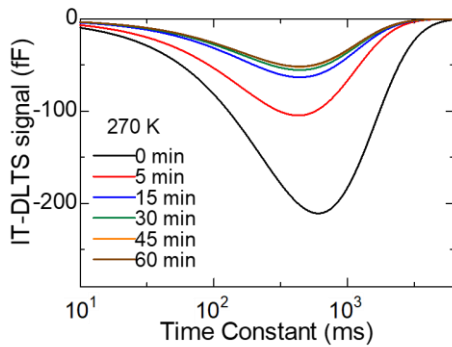


**Fig. 2.** Two-peak fitting of the spectra after subtracting the residual signal by the IT-DLTS function.

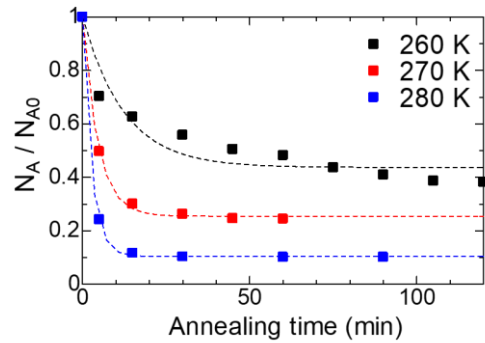
We performed IT-DLTS measurements at different temperatures, plotted the peak time constant against the inverse of the temperature (Arrhenius plot), and determined the position of the electronic level of the peak origin from the slope of the Arrhenius plot. The obtained level was  $E_v + 0.49$  eV, which corresponds to that of an Ni–hydrogen (Ni–H) complex according to literature [7].

Figure 3 shows the main peak of isothermal annealing at 270 K under reverse bias. The peak intensity decreased significantly in the first 15 min and remained almost unchanged after 45 min. After annihilation was completed via 60 min of annealing, the peak intensity was recovered to its initial value using zero-bias annealing

at 330 K for 5 min. Reverse-bias annealing was then repeated at different temperatures. Figure 4 shows the isothermal annealing curves of the main peak at three temperatures. The vertical axis represents the concentration of the Ni-related defect  $N_A$ , which has the electronic level and can be detected as the present main peak, normalized by the initial value  $N_{A0}$ . Because Ni-related defects should be on GBs and are not uniformly distributed over the measurement region of IT-DLTS,  $N_A$  and  $N_{A0}$  are not the defect concentrations but the amounts per unit GB area within the measurement region, which were obtained from the parameter  $\Delta C$  in the IT-DLTS function, corresponding to the main peak intensity. For simplicity, we refer to these amounts as “concentrations” in this paper. This is not a problem because the bias voltage during IT-DLTS measurements was always constant at  $-2$  V. As shown in Fig. 4, the defect concentration decreased rapidly at first for all temperatures before ceasing annihilation at a certain value; this value was smaller at higher temperatures. It should be noted that the IT-DLTS spectra and their intensities (presented in Figs. 3 and 4) have the unknown signal mentioned above already subtracted. Therefore, the result that the annihilation ceased at a certain intensity suggests that an inverse reaction of annihilation, that is, a formation reaction, took place, and equilibrium was reached after a long duration of annealing.



**Fig. 3.** Isothermal annealing results at 270 K for the main peak of Ni-related IT-DLTS spectra.



**Fig. 4.** Isothermal annealing curves of the main peak for 260 K, 270 K, and 280 K. The dashed lines are the fitting curves from Eq. (2).

Therefore, we propose a two-state model for the annihilation of the Ni-related level, as shown in Fig. 5, which is similar to the model used by Vu [8] for the generation and annihilation of boron–oxygen-related defects in CZ silicon solar cells. State A in Fig. 5 is the state in which the peak is detected by IT-DLTS, and state B is that in which the peak is not detected. The energy of A is lower than that of B, and many Ni-related defects are initially in A. Under reverse bias, the energy of A become higher, and defects in state A transfer into state B, which is observed as an exponential decrease in peak intensity. As the transition proceeds and the concentration of B increases, a transition in the opposite direction (B to A) occurs, and eventually the transitions in both directions reach equilibrium. The fact that the peak intensity in equilibrium is smaller at higher annealing temperatures indicates that the energy of A under reverse bias is still lower than that of B. In such a two-state model, the rate equations for the time evolution of the level concentrations in each state  $N_A$  and  $N_B$  are as follows:

$$\frac{dN_A}{dt} = -K_1 N_A + K_2 N_B, \quad \frac{dN_B}{dt} = K_1 N_A - K_2 N_B \quad (1)$$

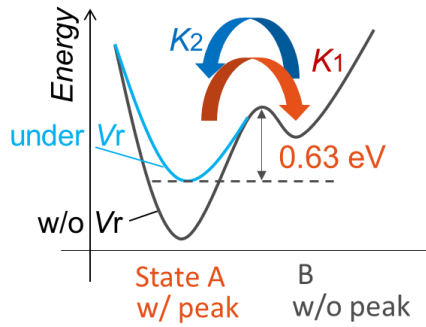
We assumed that all defects were initially in state A, that is,  $N_B = 0$  at  $t = 0$ , because the peak intensity decreased almost exponentially in the early stages of annihilation. As a result, we obtained the following expression for the annihilation curve of the defect:



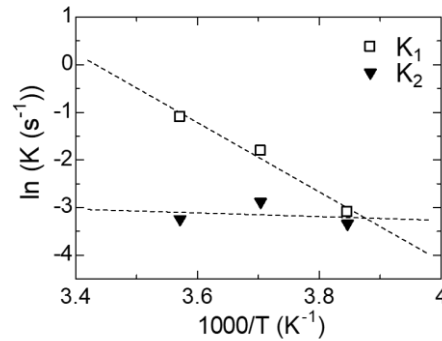
$$\frac{N_A}{N_{A0}} = \frac{K_2}{K_1 + K_2} + \left(1 - \frac{K_2}{K_1 + K_2}\right) \exp(-(K_1 + K_2)t). \quad (2)$$

The rate constants  $K_1$  and  $K_2$  were fitted to the annealing curves in Fig. 4 using Eq. (2), and Arrhenius plots of these parameters are shown in Fig. 6. From the temperature dependence of  $K_1$ , the activation energy of defect annihilation was determined to be 0.63 eV, which is the difference between the energy of state A and the saddle point of the transition, as shown in Fig. 5. The pre-exponential factor for  $K_1$  was  $7 \times 10^{10} \text{ s}^{-1}$ . The energy barrier from state A to B, which should be obtained from the Arrhenius plot of  $K_2$ , was too small to be determined. This fact is consistent with the assumption that almost all defects in the initialized state were in state A. With respect to the physical picture of states A and B, we now presume that the Ni–H complex on a GB has two stable states that can be transferred by an atomic jump. The annihilation of Ni-related defects under reverse bias has also been reported in single crystalline silicon [9]. However, it took several hundreds of hours at 298 K to reduce the Ni-related DLTS peak in that study. Therefore, we believe that the phenomena we observed are different from those previously reported.

In summary, we investigated the annihilation of an Ni-related state on the GBs of multi-crystalline silicon under reverse bias and explained it in terms of the two-state model. We obtained a value of 0.63 eV for the activation energy of the annihilation process, which might be the energy barrier height for Ni–H to transfer from the site with a gap level to that without a gap level.



**Fig. 5.** Two-state model used to explain reverse bias effects.



**Fig. 6.** Arrhenius plots for the rate constants  $K_1$  and  $K_2$ .

## REFERENCES

- [1] J. Chen and T. Sekiguchi, *Jpn. J. Appl. Phys.* **46**, 6489 (2007).
- [2] Z. Xi, D. Yang, J. Chen, and T. Sekiguchi, *Mater. Sci. Semicond. Proc.* **9**, 304 (2006).
- [3] Y. Yamashita, M. Ochi, H. Yoshinaga, Y. Kamiura, and T. Ishiyama, *Physica B* **404**, 5071 (2009).
- [4] M. Yabuki, Y. Yamashita, T. Tokura, T. Nishikawa, and Y. Hayashi, *Proc. The Forum on the Science and Technology of Silicon Materials 2014*, 209 (2014).
- [5] Y. Tokuda, N. Shimizu, and A. Usami, *Jpn. J. Appl. Phys.* **18**, 309 (1979).
- [6] H. Shiraki, Y. Tokuda, and K. Sassa, *J. Appl. Phys.* **84**, 3167 (1998).
- [7] L. Scheffler, V. I. Kolkovskiy, and J. Weber, *J. Appl. Phys.* **116**, 173704 (2014)
- [8] T. K. Vu, Y. Ohshita, K. Araki, and M. Yamaguchi, *J. Appl. Phys.* **91**, 4853 (2002).
- [9] S. J. Pearton and A. J. Tavendale, *J. Appl. Phys.* **54**, 1375 (1983).

## Effect of thermal treatment on bulk lifetime of CZ silicon wafer of solar cell

Katsuto Tanahashi<sup>1\*</sup> and Hidetaka Takato<sup>1</sup>

<sup>1</sup> Renewable Energy Research Center, National Institute of Advanced Industrial Science and Technology (AIST), 2-2-9, Machiikedai, Koriyama, Fukushima 963-0298, JAPAN

e-mail: tanahashi.katsuto@aist.go.jp

### Abstract

We report on the lifetime improvement in Czochralski (CZ) silicon wafers of solar cells by pre-rapid thermal oxidation (RTO). The *n*-type CZ silicon wafers with the thickness of 160  $\mu\text{m}$  were subjected to RTO followed by the three-step thermal annealing, which corresponded to the typical processes of a fully ion-implanted passivated emitters, rear totally diffused silicon solar cell. We investigated the effect of RTO conditions on the minority carrier lifetime of CZ silicon wafer. We also discuss the effect of surface morphology on the change in lifetime of wafer by the thermal oxidation.

### Introduction

Many types of silicon solar cells have been researched and commercialized: a homogeneous emitter cell, passivated emitter and rear (PERC) cell, passivated emitters, rear totally diffused (PERT) cell, interdigitated back-contact (IBC) cell and so on. A common issue of the silicon solar cell is the degradation of bulk lifetime. It is well known that the thermal treatment during the fabrication process of Czochralski (CZ) silicon solar cells causes the degradation of bulk lifetime due to oxygen precipitation. One of the solutions to suppress the oxygen precipitation during thermal treatment is tabula rasa treatment [1], which is a pre-thermal treatment prior to the fabrication of CZ silicon solar cells.

Sopori *et al.* reported that the oxygen precipitate nuclei of CZ silicon wafers for solar cell can be dissolved using a flash-annealing at temperature between 1150 and 1250 °C for a short time. This process improves the minority carrier lifetime of as-grown silicon wafers used in their study [2]. Kissinger *et al.* investigated the oxygen precipitation of CZ silicon wafers subjected to pre-rapid thermal annealing at 1100-1250 °C for 30 sec and flash lamp annealing followed by 780 °C for 3 hours + 1000 °C for 16 hours anneals [3]. They developed a model of intrinsic point defect generation during these two types of pre-thermal treatment to understand the oxygen precipitation during subsequent annealing. Walter *et al.* performed pre-thermal treatment within a conventional belt-firing furnace at a peak temperature of 1000 °C [4]. This treatment leads to a reduction of lifetime degradation during subsequent high-temperature processing. Thus, tabula rasa treatment has various parameters such as temperature, duration time, ramping rate, cooling rate, atmosphere and so on.

In tabula rasa treatment, point defect generation at wafer surface has an important role. In oxidation, excess silicon atoms are created at the interface between silicon and oxide layer [5]. They diffuse into the bulk and become self-interstitials. Generally, the mirror-polished (100) oriented silicon wafers have been used in the fabrication of ultra-large-scale integrated circuits, whereas the crystalline silicon solar cell has a textured surface, which is composed of upright tetrahedral pyramids with four (111) planes. The rate of thermal oxidation of silicon depends on surface orientation [6]. However, the effect of surface morphology on tabula rasa treatment has not yet fully investigated.

In this paper, we investigate the lifetime improvement in CZ silicon wafers of solar cell by pre-rapid thermal oxidation (RTO) followed by the thermal annealing, which corresponds to the fabrication processes of a fully ion-implanted PERT silicon solar cell. Moreover, we investigate the change in lifetime of silicon with textured surface or alkaline-etched surface subjected to thermal oxidation. We discuss the effect of surface morphology on the change in lifetime of wafer by the thermal oxidation.

## Experimental

The commercially available *n*-type (phosphorus doping) CZ silicon wafers with the size of 156 mm × 156 mm, thickness of 160 μm were used in this study. First, the surface damage due to wafer slice was removed by chemical etching. Following the wafer texturing on the front and rear surface, wafer cleaning was performed with SC-1 and SC-2. An oxide layer on the silicon wafer was removed by dipping in hydrofluoric acid.

As tabula rasa treatment, a rapid thermal annealing in an oxygen atmosphere (RTO) was performed; 800 °C for 30 sec, 900 °C for 30 sec, and 1050 °C for 30 sec. Subsequently, we performed the following three-step thermal annealing to the silicon wafer: the first was oxidation at 900 °C for 60 min, the second was isothermal annealing at 1050 °C for 30 min in a nitrogen atmosphere, and the third was oxidation at 900 °C for 10 min. These correspond to the typical processes of a fully ion-implanted PERT silicon solar cell [7]. The effective minority carrier lifetime was characterized by micro-wave photoconductive decay method using Semilab PV-2000 system. In the carrier lifetime measurement and imaging, an oxide layer of silicon wafer was removed by dipping in hydrofluoric acid, and wafer surface was passivated with quinhydrone/ethanol solution. A detailed experimental condition is given in Refs. [8].

Silicon wafer with texturing was also dipped in potassium hydroxide (KOH) solution to etch off pyramidal configurations. Silicon wafers with the textured surface and alkaline-etched surface were subjected to thermal oxidation at 900 °C for 30 min or 1000 °C for 30 min by using the quartz tube furnace. The oxide layer on silicon wafer was removed by dipping in hydrofluoric acid, and some wafers with texturing were subsequently dipped in KOH solution to make surface smooth after oxidation. And then, silicon wafers with textured surface and alkaline-etched surface were passivated with plasma enhanced chemical vapor deposition silicon nitride layer (PECVD SiN). Minority carrier lifetime was characterized by using Sinton Instruments WCT-120.

## Results and discussion

Figure 1 shows the Lifetime mapping of silicon wafer subjected to (a) the three-step annealing, (b) RTO at 900 °C followed by the three-step annealing and (c) RTO at 1050 °C followed by the three-step annealing, respectively. Figure 2 shows the distribution of lifetime data of silicon wafers with and without RTO followed by three-step annealing. Silicon wafer with donor killer annealing (black, DK-ANL) is not subjected to three-step annealing. Table 1 is the average implied  $V_{oc}$  of the whole wafer calculated from the data of lifetime. The three-step annealing decreases the lifetime of wafer. This is due to the oxygen precipitation during three-step annealing, although the ring-like pattern or striation is not observed in Fig. 1.

The lifetime distribution of silicon wafer subjected to RTO followed by three-step annealing shift to high values, comparing with that of w/o RTO. Thus, RTO is effective to suppress the lifetime degradation during three-step annealing, i.e., oxygen precipitation. Silicon wafer subjected to RTO at 800 °C for 30 sec shows the high lifetime distribution with the range of oxidation temperature between 800 °C and 1050 °C. We previously investigated on

the impact of pre-rapid thermal processing (RTP) on the lifetime of silicon wafers subjected to the three-step annealing [8]. RTP conditions for suppression of lifetime degradation strongly depend on the growth conditions of CZ silicon crystals. RTO conditions used in this study may not dissolve but grow as-grown nuclei of oxygen precipitate, resulting in the lifetime degradation due to the growth of oxygen precipitates during three-step annealing.

Self-interstitials created by oxidation have a role of suppression of oxygen precipitate growth. Concentration of self-interstitial created by thermal oxidation depends on the thickness of oxide layer. The thickness of oxide layer depends on the orientation of wafer surface as well as oxidation temperature. Therefore, we investigated the effect of surface morphology on the change in lifetime of wafer by thermal oxidation. Figure 3 shows the laser microscope images of (a) textured surface and (b) alkaline-etched surface. The variation in the height of the alkaline-etched surface is approximately a half of that of textured surface. Figure 4 shows the lifetime of wafer with textured surface and alkaline-etched surface after thermal oxidation at 900 °C for 30 min or 1000 °C for 30 min. Some wafers with textured surface (green squares) were dipped in KOH solution after thermal oxidation at 900 °C for 30 min. They indicate approximately same values as that of textured surface (green squares). The rates of thermal oxidation are in the order (111) > (100) of surface orientation [6]. The difference of the lifetime of wafer between textured surface and alkaline-etched surface is due to the self-interstitials created by thermal oxidation, which has intrinsic energy level and become the carrier recombination center [9].

## Summary

We investigated the lifetime of silicon wafers subjected to RTO at temperature range of 800 °C to 1050 °C followed by the three-step thermal annealing with. RTO is effective to suppress the lifetime degradation during three-step annealing. However, the lifetime of wafer subjected to RTO at 800 °C for 30 sec shows the high values in the distribution of lifetime data with the range of oxidation temperature between 800 °C and 1050 °C. We also investigated the effect of surface morphology on the lifetime of wafer subjected to oxidation. Following thermal oxidation, the lifetime of wafer with textured surface is lower than that of alkaline-etched surface.

## REFERENCES

- [1] R. Falster, M. Cornara, D. Gambaro, M. Olmo, and M. Pagani, *Solid State Phenomena* **57/58**, 123-128 (1997)
- [2] B. Sopori, P. Basnyat, S. Devayajanam, T. Tan, A. Upadhyaya, K. Tate, A. Rohatgi, and H. Xu, *IEEE J. Photovolt.* **7**(1), 97-103 (2017).
- [3] G. Kissinger, D. Kot, and W. von Ammon, *ECS J. Solid State Sci. Tech.* **1**, 269-275 (2012).
- [4] D. Walter, B. Lim, R. Falster, J. Binns, and J. Schmidt, in *Proc. 28th European Photovoltaic Specialist Conf. and Exhibition (EuPVSC) 2012*, pp. 699–702.
- [5] H. kageshima, K. Shiraishi, and M. Uematsu, *Jpn. J. Appl. Phys.* **38**, L971-L974 (1999).
- [6] E. A. Irene, H. Z. Massoud, and E. Tierney, *J. Electrochem. Soc.* **133**, 1253-1256 (1986).
- [7] K. Tanahashi, T. Tachibana, K. Sueoka, M. Moriya, Y. Kida, S. Utsunomiya, K. Shirasawa, and H. Takato, *ECS J. Solid State Sci. Technol.* **8**, 596-601 (2019).
- [8] K. Tanahashi, T. Fukuda, K. Shirasawa, and H. Takato, *AIP Conference Proceedings* **1999**, 130018 (2018).
- [9] T. Hasegawa and S. Matsumoto, *Jpn. J. Appl. Phys.* **27**, 1906-1909 (1988).

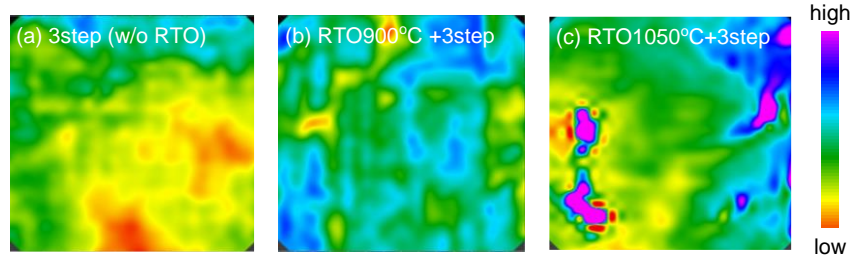


Fig. 1. Lifetime mapping of silicon wafer subjected to (a) the three-step annealing, (b) RTO at 900 °C followed by the three-step annealing and (c) RTO at 1050 °C followed by the three-step annealing.

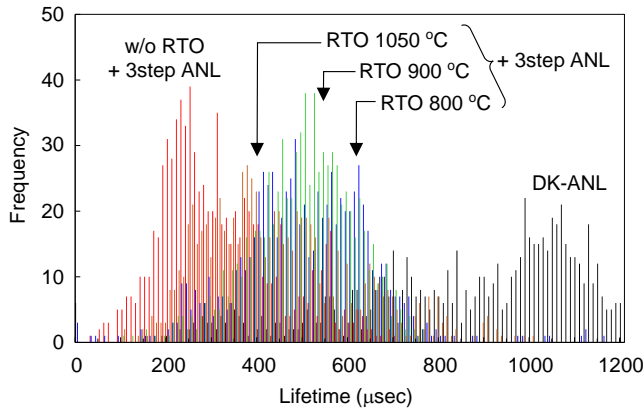


Fig. 2. Lifetime distribution of silicon wafer with and w/o RTO followed by 3step annealing. RTO conditions are as follows; 800 °C for 30 sec (blue), 900 °C for 30 sec (green), 1050 °C for 30 sec (brown), and w/o RTO (red).

Table 1 Implied  $V_{oc}$  of silicon wafer with and w/o RTO followed by 3step annealing.

Condition	$iV_{oc}$ (V)
DK annealing	0.688
w/o RTO + 3step	0.644
RTO 800 °C +3step	0.677
RTO 900 °C +3step	0.664
RTO 1050 °C +3step	0.661

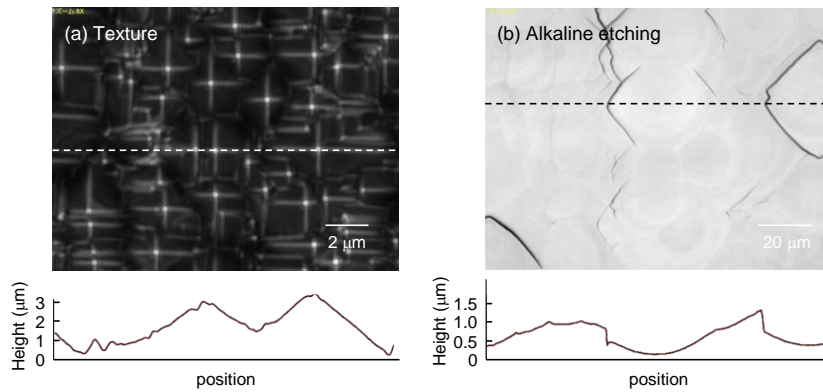


Fig. 3. Laser microscope images of (a) textured surface and (b) alkaline-etched surface.

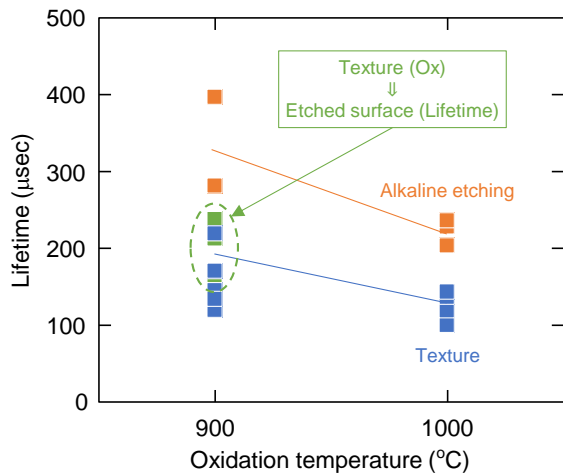


Fig. 4. Lifetime of wafer with texture (blue) and alkaline-etched surface (orange) after oxidation at 900 °C for 30 min or 1000 °C for 30 min. Some wafers with textured surface were dipped in KOH solution after thermal oxidation at 900 °C for 30 min (green).

## Fabrication of Tensile-strained Single-crystalline GeSn Wires on Amorphous Quartz Substrates by Local Liquid-phase Crystallization

Takayoshi Shimura<sup>1\*</sup>, Hiroshi Oka<sup>1†</sup>, Takuji Hosoi<sup>2</sup>, Yasuhiko Imai<sup>3</sup>, Shigeru Kimura<sup>3</sup>, and Heiji Watanabe<sup>1</sup>

<sup>1</sup>Graduate School of Engineering, Osaka University, 2-1 Yamadaoka, Suita, Osaka 565-0871, Japan

<sup>2</sup>School of Engineering, Kwansei Gakuin University, Sanda, Hyogo, Japan

<sup>3</sup>Japan Synchrotron Radiation Research Institute (JASRI), Kouto, Sayo-cho, Sayo-gun, Hyogo 679-5198, Japan

e-mail: shimura@prec.eng.osaka-u.ac.jp

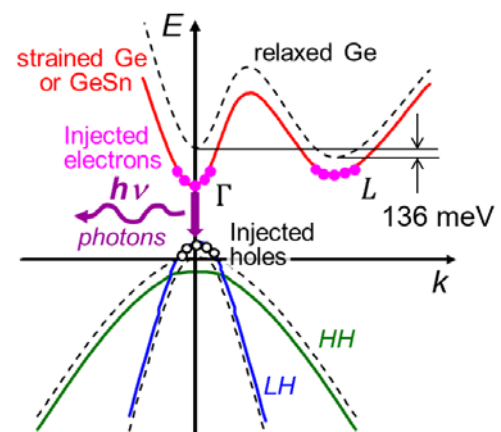
### Abstract

We demonstrate the fabrication of tensile-strained single-crystalline GeSn wires on amorphous quartz substrates by local liquid-phase crystallization (LLPC). In this method, amorphous GeSn wires on a quartz substrate are partially annealed at temperatures above the melting point of the GeSn wire. The LLPC begins at the interface with the unmelted GeSn wire. Transmission electron microscope (TEM) observations showed a high-quality dislocation-free single-crystalline structure of the GeSn wires. We also confirmed significant intensity enhancements and red-shift in the photoluminescence (PL) peaks. These results originated from the 2.6% incorporation of Sn and the 0.5% tensile strain induced by the difference in the thermal expansion coefficients between the GeSn wires and quartz substrate.

### Introduction

Electronic–photonic integration is a solution for fast data processing and data transfer [1]. Although Si is the most common semiconductor material in use currently, it has an indirect bandgap and is difficult to use as a light emitting material. Light sources made of group III–V materials are realistic solutions, but require a costly bonding process. Therefore, Ge, which is in the same group IV materials as Si, has drawn attention. Although it also has an indirect bandgap structure, the difference in the conduction band bottoms between the  $\Gamma$  and L valleys is only 136 meV (Fig. 1) [2]. Therefore, considerable research has been devoted to enhancing the optical properties of Ge. Theory predicts that biaxial tensile strains greater than 1.8% enable indirect-to-direct bandgap transitions. GeSn alloys containing over 6.5% are expected to have direct bandgaps [3].

However, there are many issues to address in the growth of a GeSn single crystal layer. Because Ge and Si crystals have a lattice mismatch of 4%, the two-step growth process is commonly used with a low temperature growth at the initial stage to suppress crystal defects. Although the threading dislocations can be significantly reduced, the density is still approximately  $10^6/\text{cm}^2$ , and crosshatch patterns are observed on the growth surface even after the formation of the 2.5  $\mu\text{m}$  thick Ge layer [4]. Adding Sn atoms causes more difficulties. Because a lattice mismatch also occurs on the relaxed Ge substrates, compressive strain is applied, and the effect of adding Sn is



**Fig. 1.** Band structure modulation of Ge by incorporating Sn atoms and inducing tensile strain.

<sup>†</sup>Present address: National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki 305-8568, Japan.

reduced. Furthermore, because the solid solubility of Sn atoms in Ge is as low as approximately 1%, low-temperature non-equilibrium growth at several hundred degrees Celsius is inevitable for growing GeSn films with Sn fractions exceeding the solid solubility. This causes significantly poor optical properties due to the point defects.

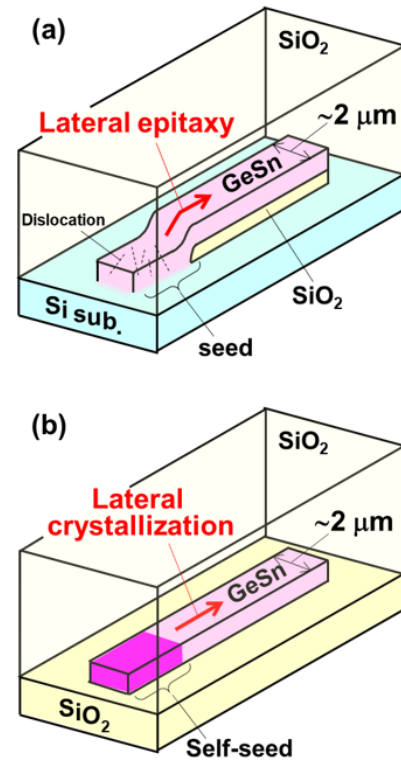
However, we have been fabricating high-quality single-crystal GeSn wires with tensile strain by lateral liquid phase epitaxy (LLPE) (Fig. 2a) [5,6]. In this method, amorphous GeSn wires connected to the seed area of an Si substrate are annealed at temperatures above the melting point of the GeSn wires, leading to LLPE growth from the seed along the GeSn wires during cooling. Crystalline defects caused by the lattice mismatch between Si and GeSn are generated in the seed but quickly move out of the thin wires, similar to necking in the Czochralski crystal growth process [7].

This method has the advantage of inducing tensile strain owing to the difference in the thermal expansion coefficients of the GeSn wires and Si substrate. We confirmed approximately 0.3% tensile strain in the GeSn wires fabricated by this method [5,6]. It should be noted that the tensile strain induced by this method is independent of the Sn fraction in the GeSn wires, which allows GeSn wires with a high Sn fraction and high tensile strain.

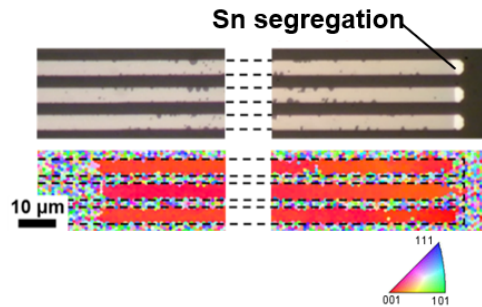
In this study, we demonstrate the fabrication of tensile-strained single-crystalline GeSn wires on amorphous quartz substrates by local liquid-phase crystallization (LLPC) (Fig. 2b) [8-10]. In this method, amorphous GeSn wires on a quartz substrate without the Si seed are partially annealed at temperatures above the melting point of the GeSn wires. The LLPC starts from the interface with the unmelted GeSn wire during cooling (Fig. 1b). We expect two additional advantages compared with LLPE. One is a higher tensile strain because the thermal expansion coefficient of the quartz substrate is  $5 \times 10^{-7}/^\circ\text{C}$ , which is one order of magnitude smaller than  $4 \times 10^{-6}/^\circ\text{C}$  of Si. A tensile strain of approximately 0.6% is expected for the LLPC. We also expect the elimination of Si impurities diffused from the Si seeds. Si atoms diffuse for over 200  $\mu\text{m}$  from the Si seed along the GeSn wires during LLPE [6]. This causes the degradation of the optical properties of the GeSn wires.

### Experimental methods

We used a commercially available quartz substrate as the starting substrate. A 100-nm-thick amorphous GeSn layer was deposited using a molecular beam deposition system and patterned into wires with a width of 3  $\mu\text{m}$  and length of 300  $\mu\text{m}$ . The Sn content inside the amorphous GeSn layer was estimated to be approximately 2% by



**Fig. 2.** (a) Lateral liquid phase epitaxy (LLPE). (b) Local liquid phase crystallization (LLPC).



**Fig. 3.** Optical image and crystal orientation map of GeSn wires fabricated by LLPC.

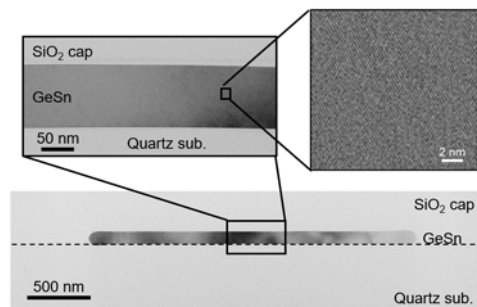
XPS measurement. It should be noted that Sn surface segregation was observed on the as-deposited GeSn layers owing to the low solid solubility of Sn in Ge. After SiO<sub>2</sub> capping of 1 μm thickness by RF sputtering to prevent the agglomeration of the GeSn wires, rapid thermal annealing (RTA) was performed in nitrogen (N<sub>2</sub>) ambient above the melting point of the GeSn wires for 1 s. During RTA, the samples were placed on the edge of a carbon susceptor for the partial melting of the amorphous GeSn wires.

## Results and discussion

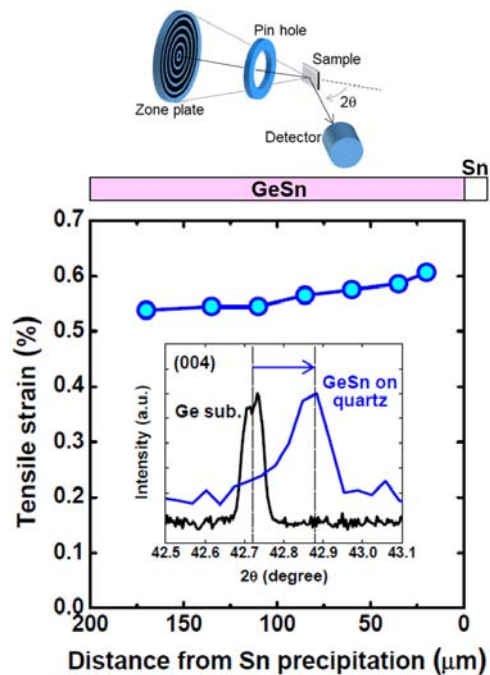
Figure 3 shows the optical image and crystal orientation map obtained by electron back scatter diffraction (EBSD) of the GeSn wires fabricated by LLPC. We observe bright ends in the wires in the optical image. These indicate the Sn precipitates exhibiting crystallization along the wires, as observed in the LLPE wires [6]. The EBSD image clearly shows that the GeSn wires has a single crystal structure and (100) orientation in the direction normal to the surface. In LLPC, single crystal seeds are not employed at the initial stage of crystallization. Therefore, this preferential orientation of the GeSn wires is determined by an interface energy between the GeSn wires and quartz substrate.

Figure 4 shows the transmission electron microscope (TEM) images of single-crystalline GeSn wires at 100 μm, far from the Sn precipitate. We observed that a dislocation-free single-crystalline GeSn layer was grown on the quartz substrate. The average Sn content along the depth direction was estimated to be 2.6% by energy dispersive X-ray spectroscopy (EDX), which exceeds the solid solubility limit of Sn in Ge. The Sn content in the single-crystalline GeSn layer was higher than the initial Sn content inside the amorphous GeSn layer (2%). This can be attributed to the diffusion of Sn, which was segregated at the surface of the as-deposited GeSn layer. We also confirmed by Raman spectroscopy that the Sn content along the wire was almost constant except near the Sn precipitate (data not shown).

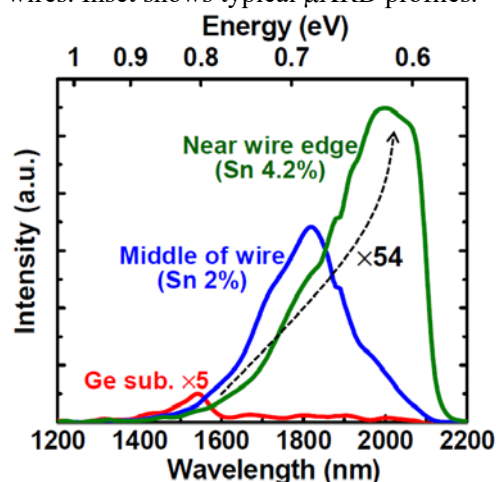
Further, we evaluated the tensile strain in the GeSn wires by synchrotron microbeam X-ray diffraction (μXRD) with a beam size of 700×200 nm<sup>2</sup>, which was performed at BL13XU of SPring-8. The inset in Fig. 5 shows a typical diffraction profile of 004reflection of a single crystalline GeSn wire, which is



**Fig. 4.** TEM images of the GeSn wire fabricated by LLPC.



**Fig. 5.** Schematic of μXRD and the distribution of tensile strain along the GeSn wires. Inset shows typical μXRD profiles.



**Fig. 6.** PL spectra at the middle and near the Sn precipitate of the single-crystalline GeSn wire on the quartz substrate.



observed at a higher  $2\theta$  angle compared to the Ge substrate, indicating a decrease in the (004) lattice spacing. From the diffraction peak position of the GeSn wire, the in-plane strain was estimated using Vegard's law and Poisson's ratio. Figure 5 shows the tensile strain evaluated from the  $\mu$ XRD results as a function of the distance from the Sn precipitation. We observed that over 0.5% of the tensile strain was applied in the GeSn wire. This tensile strain is in good agreement with the calculation based on the difference in the thermal expansion coefficient between the GeSn wires and quartz substrates. From these results, we confirmed that a highly tensile-strained single-crystalline GeSn layer with Sn content exceeding solid solubility was grown on quartz substrates.

Figure 6 shows the photoluminescence (PL) spectra at the middle and near the Sn precipitate of the single-crystalline GeSn wire on the quartz substrate. The PL spectrum from the middle of the GeSn wire shows direct bandgap emission at a peak wavelength of 1800 nm, which is red-shifted from 1550 nm of the bulk Ge peak, corresponding to a bandgap shrinkage of 0.1 eV. This shrinkage is caused by incorporating Sn atoms and inducing biaxial tensile strain. Moreover, an enhanced direct bandgap emission 34 times higher than that from the Ge substrate was observed, indicating an excellent crystalline quality of the single-crystalline GeSn wire. The PL spectrum near the edge of the GeSn wire exhibited a significantly enhanced luminescence, 54 times higher than that from the bulk Ge peak, which was observed with a peak wavelength of approximately 2000 nm (0.62 eV), originating from the increase in the Sn content. The GeSn wire still has the indirect bandgap structure, but the energy difference between the  $\Gamma$  and L valley of the conduction band bottom is only 30 meV, approximately the same as thermal energy at room temperature [11].

### Acknowledgments

This work was partly supported by JSPS KAKENHI (Grant Numbers 20H02620, 21K04880, and 22H01528). The synchrotron radiation experiments were performed at the BL13XU of SPring-8 with the approval of the Japan Synchrotron Radiation Research Institute (JASRI) (Proposal No. 2015B1226).

### REFERENCES

- [1] D. J. Lockwood, and L. Pavesi, *Silicon Photonics IV: Innovative Frontiers* (Switzerland: Springer) (2021).
- [2] J. Michel, J. Liu, and L. C. Kimmerling, *Nat. Photonics* **4**, 527 (2010).
- [3] D. Rainko, Z. Ikonik, A. Elbaz, *et al.*, *Sci. Rep.* **9**, 259 (2019).
- [4] J. M. Hartmann, J.-F. Damlencourt, Y. Bogumilowicz, P. Holliger, G. Rolland, and T. Billon: *J. Cryst. Growth* **274**, 90 (2005).
- [5] M. Matsue, Y. Yasutake, S. Fukatsu, T. Hosoi, T. Shimura, and H. Watanabe, *Appl. Phys. Lett.* **104**, 031106 (2014).
- [6] T. Shimura, M. Matsue, K. Tominaga, K. Kajimura, T. Amamoto, T. Hosoi, and H. Watanabe, *Appl. Phys. Lett.* **107**, 221109 (2015).
- [7] W. C. Dash, *J. Appl. Phys.* **30**, 459 (1959).
- [8] H. Oka, M. Koyama, T. Tomita, T. Amamoto, K. Tominaga, S. Tanaka, T. Hosoi, T. Shimura, and H. Watanabe, 2016 IEEE International Electron Devices Meeting (IEDM), 2016, pp. 22.1.1–22.1.4.
- [9] H. Oka, T. Amamoto, M. Koyama, Y. Imai, S. Kimura, T. Hosoi, T. Shimura, and H. Watanabe, *Appl. Phys. Lett.* **110**, 032104 (2017).
- [10] H. Oka, M. Koyama, T. Hosoi, T. Shimura, and H. Watanabe, 2017 Symposium on VLSI Technology, 2017, pp. T58–T59.
- [11] D. Rainko, Z. Ikonik, A. Elbaz, N. von den Driesch, D. Stange, E. Herth, P. Boucaud, M. El Kurdi, D. Grützmacher & D. Buca, *Sci. Rep.* **9**, 259 (2019).

## Electron spin resonance study of Si dangling bond defects in stacks of LPCVD SiN film on H<sub>2</sub> or N<sub>2</sub> Annealed Si(001) substrate

Hayato Miyagawa<sup>1\*</sup>, Kosuke Bunya<sup>1</sup>, Hisatsugu Kurita<sup>2</sup>, Masataka Nakamura<sup>2</sup>, and Yoshiaki Kamigaki<sup>3</sup>

<sup>1</sup>*Faculty of Engineering and Design, Kagawa University, 2217-20 Hayashi-cho, Takamatsu, 761-0396, Japan*

<sup>2</sup>*Manufacturing Division, ROHM Hamamatsu Co., Ltd., 10 Sanwa-Cho, Minami-Ku, Hamamatsu, 435-0038, Japan*

<sup>3</sup>*Electron and Bio Research Laboratory (EBL), 2-16-16 Nerima, Nerima-Ward, Tokyo, 176-0001, Japan*

e-mail: miyagawa.hayato@kagawa-u.ac.jp

### Abstract

In this study, the interface state between silicon nitride (SiN) and Si underlayer for SiN film made by low pressure chemical vapor deposition on Si(001) substrate was investigated. For this, the Si surface before SiN deposition were microscopically observed, and the electron spin resonance (ESR) measurements after SiN deposition were conducted. H<sub>2</sub> annealing of Si(001) substrate contributed to the atomic flattening of Si surface, while N<sub>2</sub> annealing with high temperature over 1000°C increased surface roughness. ESR fitting analysis revealed that dangling bond defects of Si with one or more oxygen backbonds were found to be increased with the increase in the H<sub>2</sub> annealing temperature.

### Introduction

Silicon nitride (SiN) films have high durability and high dielectric properties, owing to which they have wide applications such as charge trap layer in memory device, gate insulator film and passivation film in electric circuit. When the SiN film is under a certain field applied by voltage or accumulated charges, electrical breakdown occurs, resulting in undesirable current flows. The frequency of this charge breakdown is strongly influenced by the condition before, during, and after the growth process of SiN film. In our previous reports [1][2], the frequency of Time Dependent Dielectric Breakdown (TDDB) of low pressure chemical vapor deposition (LPCVD) SiN films in poly-Si/SiN/poly-Si (MIM) capacitors depends on N<sub>2</sub> annealing temperature after SiN deposition. We also found that the TDDB frequencies exhibit two behaviors. Regarding the first behavior type, a local maximum appeared at the N<sub>2</sub> annealing temperature of 900°C, while regarding the second behavior type, a monotonical increment appeared when the annealing temperature was over 1000°C. These two increasing trends of TDDB frequency showed good agreement with the increase in defect densities near the interface of SiN, which were estimated from Electron Spin Resonance (ESR) method for SiN films on Si(001) substrate processed under the same N<sub>2</sub> annealing conditions. This similarity between two different structures and test methods implies the early-stage breakdown of SiN dielectric films may be related to the state of interface between SiN film and under Si layer, as well as the state of silicon oxide (SiO) layer that exists natively at the interface.

Yanase et al. investigated the variation in the surface morphology of Si substrate under different temperatures of H<sub>2</sub> annealing [3], and found numerous pits on the surface when the H<sub>2</sub> annealing temperature was 900°C. ~~Kuroda~~ It is reported that the concentration of H<sub>2</sub>O and/or O<sub>2</sub> affected the surface roughness of Ar annealed Si wafer, and that the most flattened surface of Si layer was obtained with a small dose of H<sub>2</sub>O and/or O<sub>2</sub> concentration and at annealing temperature of 850°C [4][5]. At comparably small annealing temperature of 850°C–900°C, under certain given other conditions, Si reconstruction and flattened surface can be obtained. Therefore, the local

maximum of Si-DB densities observed in ESR of our SiN samples at the N<sub>2</sub> annealing temperature of 900°C for SiN might be due to interface roughness or atomic movements near the interface. In the present study, we investigate the state of Si-DB by means of ESR measurements for SiN samples of SiN/Si(001), which is fabricated on the Si(001) substrate preprocessed by annealing using H<sub>2</sub> or N<sub>2</sub> gas. We also examine the annealing effects on surface morphology of both Si(001) substrate and poly-Si by using Atomic Force Microscopy (AFM) and Scanning Electron Microscopy (SEM). In addition, we discuss about the changes in the interface of SiN films in various annealing conditions and the relationship between the interface state and the charge breakdown.

## Experiments

First, the poly-Si samples and Si(001) substrates were subjected to annealing using H<sub>2</sub> gas or N<sub>2</sub>. The poly-Si samples have a structure of poly-Si/SiO/Si(001) substrate, where the thickness of poly-Si layer was designed to be 400 nm. For Si(001) substrates, wafer misorientation angle was less than 0.034° toward the [001] direction. The annealing processes of H<sub>2</sub> and N<sub>2</sub> were carried out for 10 min and 60 min, respectively, at the temperatures of 900°C, 1000°C, and 1150°C. AFM measurements were done by contact mode using Si cantilever (NSC-36) with the curvature of 10 nm.

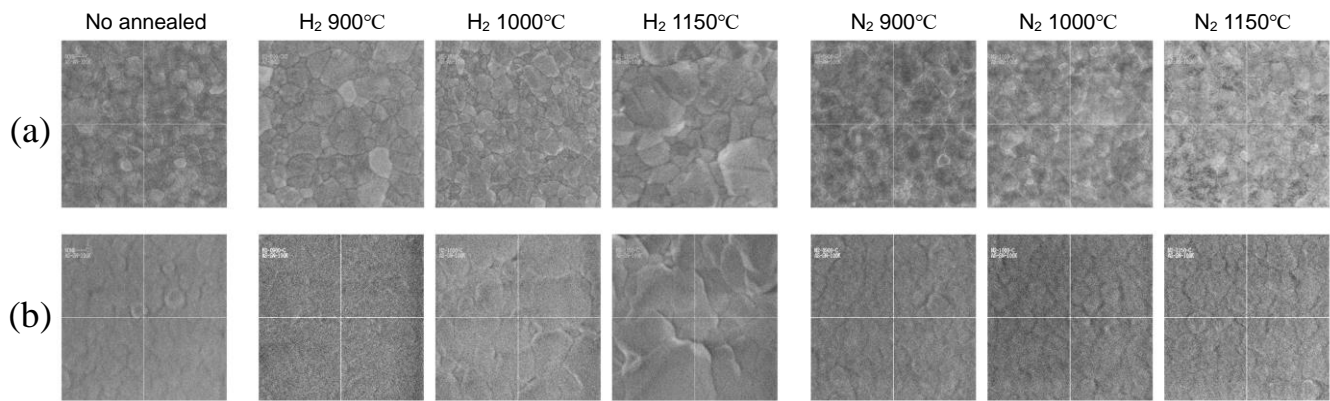
ESR measurements were carried out to investigate point defects of SiN film on Si(001) substrate and to obtain information on the variation and density of each Si-DB. For measuring ESR, we used the Si(001) substrate which was already subjected to the same annealing as mentioned above. ESR spectra were measured at room temperature using JEOL RE2X, under the conditions of 9.4 GHz microwave frequency, 0.4 mW microwave power, 15mT field range, and 337.5 mT center field. We accumulated over 256 cycles of 16 min scanning to reduce noise to signal ratio and obtain high statistical precision.

The TDDB test was done for MIM capacitors having poly-Si/SiN/poly-Si structure, where SiN film was deposited at 700°C with the mixed gas of dichlorosilane (DSC) and ammonia (NH<sub>3</sub>) flowing on the poly-Si surface, which were annealed in H<sub>2</sub> or N<sub>2</sub> atmosphere under the same conditions as mentioned above. The gas mixing ratio of DSC/NH<sub>3</sub> were set to be 0.1, and the SiN thickness were designed to be 54 nm. In the TDDB test, a constant current of 1.33 A/cm<sup>2</sup> was applied for 30 sec, and the breakdown was judged in the case of over 10% voltage change. We tested 99 chips per wafer for each MIM capacitor.

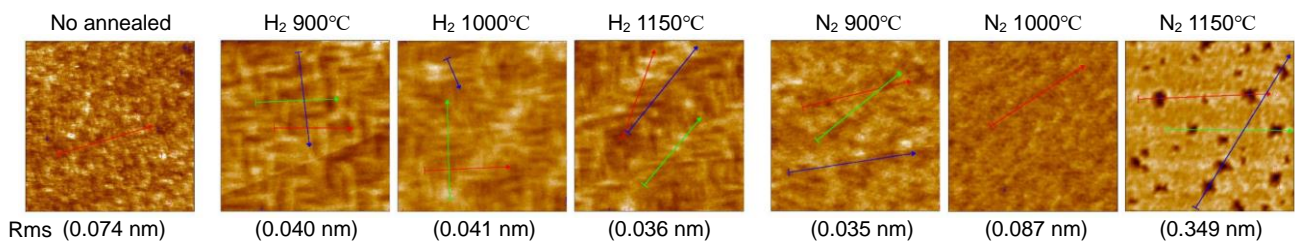
## Results and Discussions

Fig.1(a) shows SEM images of poly-Si surface annealed in H<sub>2</sub> or N<sub>2</sub> gas, and that of no-annealed sample. The area of all SEM images was 1.3 μm × 1.3 μm. As shown in Fig.1(a), there were the facets on all poly-Si surfaces annealed at different temperatures. In the case of H<sub>2</sub> annealing, the facet size increased with the increase in annealing temperature. In the case of N<sub>2</sub> annealing, no increase in facet size was observed with the increase in annealing temperature, and the size of the facets remained as small as the no-annealed sample. After the deposition of SiN, the surface of SiN film became smoother. as observed in Fig.1(b), however, the roughness from the poly-Si facets under SiN layer can still be recognized on the surface. Fig.1(b) shows the images of the SiN surface deposited on the annealed poly-Si.

Fig.2 shows AFM surface images of Si(001) substrate that had been annealed in H<sub>2</sub> or N<sub>2</sub> gas as well as the no-annealed sample. All images in Fig.2 were taken within the area of 1 μm × 1 μm. The number below each



**Fig. 1.** SEM images ( $1.3 \times 1.3 \mu\text{m}^2$ ) of (a) poly-Si surface annealed in H<sub>2</sub> or N<sub>2</sub>, and (b) surface of SiN (54 nm thickness) deposited on the annealed poly-Si.

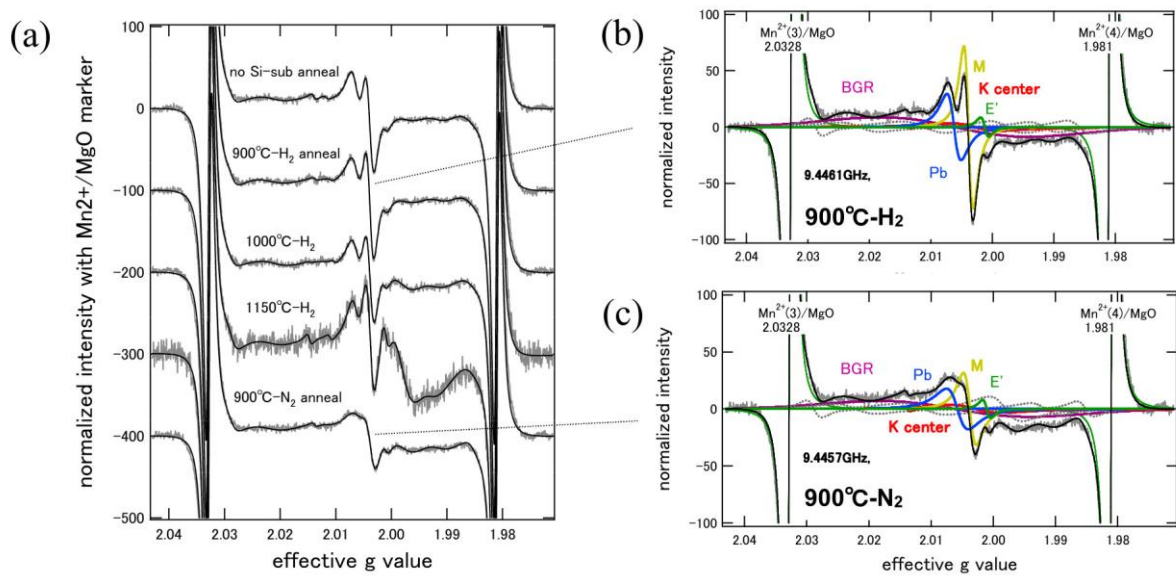


**Fig. 2.** AFM images ( $1 \times 1 \mu\text{m}^2$ ) of Si(001) substrates annealed in H<sub>2</sub> or N<sub>2</sub>, and their respective roughness(RMS).

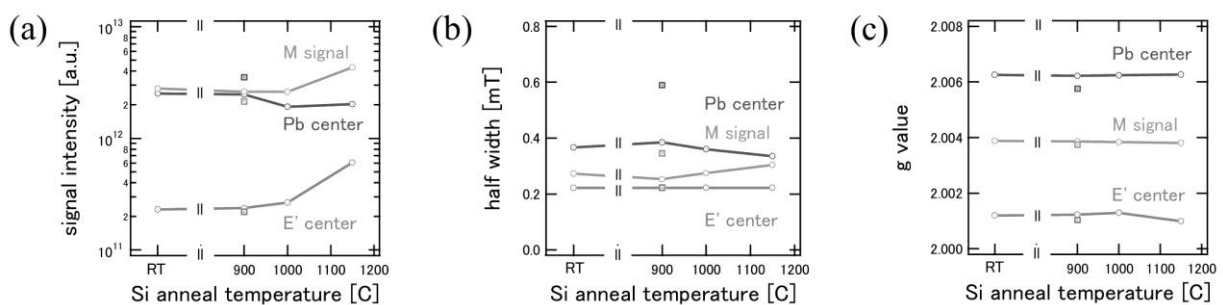
image indicates the RMS value. In the case of H<sub>2</sub> annealed samples, many bisect stripes with right angles were observed, indicating the existence of Si-Si dimer structure in the surface. In addition, we also observed the terrace-step structure [6][7][8] in wide range images more than  $5 \mu\text{m} \times 5 \mu\text{m}$ . H<sub>2</sub> annealing truly contributes to the atomic flattening on the Si surface. In the case of N<sub>2</sub> annealing, the RMS dropped down for samples annealed at 900°C. When the annealing temperature increased over 1000°C, the surface became rough. Further increase in annealing temperature to more than 1150°C resulted in many pits on the surface that had depths of 3–5 nm. This transition of surface morphology of N<sub>2</sub> annealed samples were not fully identified. However, the findings indicated that the annealing temperature of 900°C caused atomic movement on the surface of Si substrate, resulting in reduced surface roughness. On further increase in annealing temperature over 1000°C, the atom movement on the surface of the substrate becomes more active and random, reacting with N<sub>2</sub> and/or residual H<sub>2</sub>O or O<sub>2</sub> in the atmosphere outside the sample, resulting in rough surface. The many pits observed on the sample annealed at 1150°C might be due to differences of etching rate at the inhomogeneous surface that were caused due to certain nitrogen complex.

ESR spectra obtained for SiN/Si(001) samples are shown in Fig.3(a), and the spectra with fitting curves of those with Si substrate annealed at 900 °C in (a) H<sub>2</sub> gas and (b) N<sub>2</sub> gas are shown in Fig.3(b) and (c), respectively. The results of the fitting analysis for each ESR spectrum showed the defects of K center[9][10], which is the Si dangling bond (Si-DB) with three backbonds contact to nitrogen (abbreviated as  $\cdot \text{Si}=\text{N}_3$ ) and comes from inside SiN films; E' center[11], which is Si-DB with three oxygen backbonds ( $\cdot \text{Si}=\text{O}_3$ ) and comes from the interface between SiN and Si underlayer; and Pb center[12], which has three silicon backbonds ( $\cdot \text{Si}=\text{Si}_3$ ) coming from the topmost of Si substrate. We also extracted the M signal which is so far unspecified, and the g-value of M signal

located at 2.004, which is between E' center (2.001) and Pb center (2.006). Therefore, the M signal is expected to be the Si-DB with partially oxidized backbonds ( $\cdot\text{Si}=\text{Si}_2\text{O}$ ) [13][14]. As shown in Fig.3(a), the different annealing temperature of  $\text{H}_2$  annealed samples did not show any significant difference, indicating that the states of all ESR-sensitive defects were not changed even when the annealing temperature for Si underlayer in  $\text{H}_2$  atmosphere were changed. With respect to  $\text{N}_2$  atmosphere, drastic changes were observed when the annealing temperature was  $900^\circ\text{C}$ . However, no key findings were observed for  $\text{N}_2$  annealed sample over the temperature of  $1000^\circ\text{C}$  because the microwave resonance could not be tuned in ESR cavity and the power loss of microwave could not be kept within the acceptable range. This power loss indicates that  $\text{N}_2$  annealing at high temperature decreases substrate resistivity due to carrier diffusion inside Si substrate.



**Fig. 3.** ESR spectra of SiN/Si(001) samples with various annealing conditions on Si underlayer. All spectra were fitted with 16 peaks including two Mn markers. (b) Fitted results for  $900^\circ\text{C}$   $\text{H}_2$  annealed sample, and (c)  $900^\circ\text{C}$   $\text{N}_2$  annealed sample

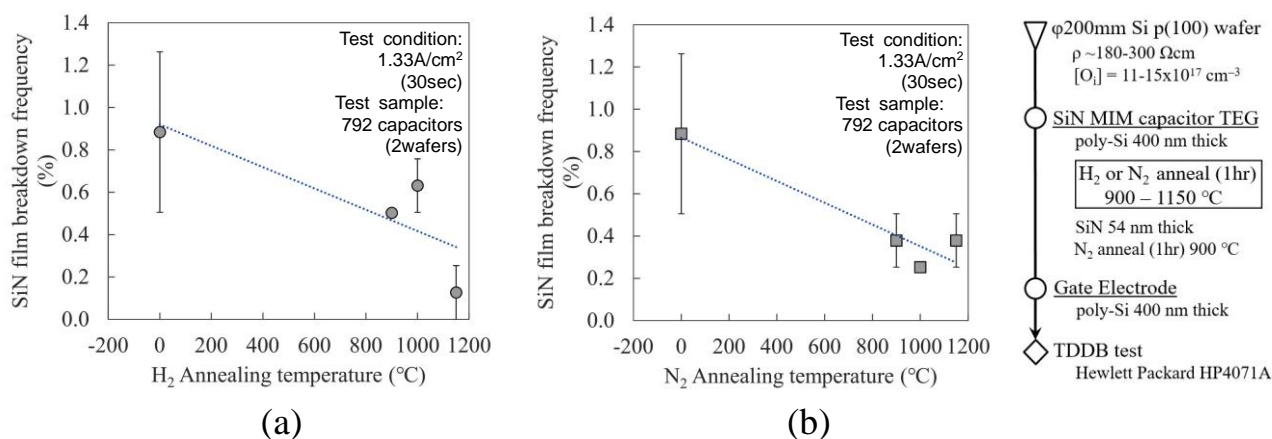


**Fig. 4.** (a) Signal intensity, (b) half width, and (c) g-values of each ESR peak signal from fitting analysis of ESR spectra of SiN/Si(001) samples with various annealing condition on Si underlayer.

The results of the fitting analysis revealed the parameters of each peak such as (a) signal intensity, (b) peak width and (c) g value as the center position of peak, as shown in Fig.4. The lines in Fig.4 indicate the dependency of  $\text{H}_2$  anneal temperature, and the marks at only  $900^\circ\text{C}$  indicate the values obtained by  $\text{N}_2$  annealing. As shown in Fig.4(a), the peak intensities of E' center and M signal increase with the increase in temperature over  $1000^\circ\text{C}$ ,

while that of Pb center decreases. This increment in E' center and M signal indicate the atom movements of both Si and O at the interface between SiN and Si substrate became active with the increase in temperature. This also resulted in the rearrangement at the backbond sites of Si-DB, prompting backbond oxidization and formation of the partially oxidized state (M signal) or the fully oxidized state (E' center). The results of N<sub>2</sub> annealing and H<sub>2</sub> annealing at 900°C did not reveal any significant difference in signal intensities of each peak. The width and g-values are found to be different, especially for Pb center, suggesting the atomic arrangement at the topmost of Si substrate. However, we need more data to verify this supposition.

Fig.5 show the frequencies of charge breakdown obtained from TDDDB test for poly-Si/SiN/poly-Si MIM capacitors with different annealing conditions of poly-Si underlayer. Fig.5(a) shows the dependency of annealing temperature of H<sub>2</sub> gas, and (b) N<sub>2</sub> gas. As shown in Fig.5(a) and (b), H<sub>2</sub> and N<sub>2</sub> annealing at a temperature over 900°C reduced the breakdown frequency effectively. The TDDDB results of annealing effect on breakdown suppression suggests the possibility that the atomically flattening of the interface under SiN film is one of the factors leading to breakdown mechanism [15][16].



**Fig. 5.** Breakdown frequencies of poly-Si/SiN/poly-Si MIM capacitor. With underlayer poly-Si annealed in (a) H<sub>2</sub> and (b) N<sub>2</sub>. The flowchart of sample preparation is shown at the right side.

## Summary

In this study, we investigated the pre-annealing effects before SiN deposition on the interface state between SiN film and Si underlayer by means of AFM, SEM observations, and ESR measurements. H<sub>2</sub> annealing to the Si(001) surface contributes to the reconstruction of the surface and the atomically flattening of the surface with RMS less than 0.05 nm. In the case of N<sub>2</sub> annealing, the surface roughness decreased at around 900°C and increased with further increase in annealing temperature at more than 1000°C. The surface of N<sub>2</sub> annealing at 1150°C exhibited numerous pits that were 3–5 nm in depth. The fitting analysis of ESR spectra revealed that the Si-DBs with one or more oxygen backbonds, E' center and M signal, increased with the increase in H<sub>2</sub> annealing temperature of over 1000°C. In comparison, Si-DB at the Si substrate surface with three Si backbonds, Pb center, decreased with the increase in N<sub>2</sub> annealing temperature. Both the interface morphologies within atomic scale observed at underlayer Si surface and the state variation of ESR defects possibly contribute to the charge breakdown of SiN films.

## REFERENCES

[1] H. Kurita, M. Nakamura, H. Miyagawa, Y. Kamigaki, ECS Transactions **108**, 69 (2022)

- [2] H. Miyagawa, Y. Kamigaki, H. Kurita, M. Nakamura, ECS Transactions **108**, 85 (2022)
- [3] Y. Yanase, H. Horie, Y. Oka, M. Sano, S. Sumino, and T. Shigematsu, J. Electrochem. Soc. **141** 3259 (1994)
- [4] X. Li, A. Teramoto, T. Suwa, R. Kuroda, S. Sugawa, T. Ohmi, Microelectronic Engineering **88**, 3133 (2011)
- [5] T. Goto, R. Kuroda, N. Akagawa, T. Suwa, A. Teramoto, X. Li, T. Obara, D. Kimoto, S. Sugawa, T. Ohmi, Y. Kamata, Y. Kumagai, K. Shibusawa, Jpn. J. Appl. Phys. **54**, 04DA04 (2015)
- [6] L. Zhong, A. Hojo, Y. Matsushita, Y. Aiba, K. Hayashi, R. Takeda, H. Shirai, H. Saito, J. Matsushita, and J. Yoshikawa, Phys. Rev. B **54**, 4 2304 (1996).
- [7] K. Izunome, Y. Saito, H. Kubota, Jpn. J. Appl. Phys. **31**, L1277 (1992)
- [8] H. Kurita, K. Izunome, H. Nagahama, T. Ino, J. Yamabe, N. Hayamizu and N. Sakurai, ECS Proceedings 2002-20, p.155 (2002).
- [9] W. L. Warren, J. Kanicki, J. Robertson, E. H. Poindexter, and P. J. McWhorter, J. Appl. Phys. **74**, 4034 (1993)
- [10] A. Toki, N. Shinohara, Y. Kamigaki, M. Nakano, A. Shibata, T. Okumine, T. Shiomi, K. Sugimoto, T. Negishi, Fu. Yoshioka, and H. Hotaki, Jpn. J. Appl. Phys. **47**, 2684 (2008)
- [11] P. M. Lenahan and P. V. Dressendorfer, J. Appl. Phys. **55**, 3495 (1984)
- [12] E. H. Poindexter, P. J. Caplan, B. E. Deal, and R. R. Razouk, J. Appl. Phys. **52**, 879 (1981)
- [13] F. J. Grunthaner, P. J. Grunthaner, and J. Maserjian, IEEE Trans. Nucl. Sci. **NS-29**, 1462 (1982)
- [14] S. K. Lai, J. Appl. Phys. **54**, 2540 (1983)
- [15] R. Hasunuma, Y. Hayashi, M. Ota, and K. Yamabe, Jpn. J. Appl. Phys. **52**, 031301 (2013)
- [16] S. Kudou, S. Ohmi, IEICE Trans. Electron. E99-C, 504 (2016)

## Effect of contact angle between SiC and metal solvents on growth surface morphology in solution growth of SiC

Tomoya Iwai<sup>1\*</sup>, Katsuya Ozeki<sup>1</sup>, Gouki Nakashima<sup>1</sup>, Toshinori Taishi<sup>1</sup>

<sup>1</sup>Faculty of Engineering, Shinshu University, Wakasato, Nagano, 380-8553, Japan

e-mail: 21w2007j@shinshu-u.ac.jp, taishi@shinshu-u.ac.jp

### Abstract

In the top-seeded solution growth (TSSG) of SiC, it has been reported that the addition of Co or Al to the Si-Cr solvent can obtain a smooth growth surface. The suppression of roughening caused by two-dimensional (2D) nucleation, and a larger contact angle between SiC and the solvent is related to the smoothing of the growth surface. On the other hand, from the viewpoint of long SiC crystal growth, we had proposed a unique solution growth method for SiC using SiC ceramics as a solute and a metal solvent without Si. We achieved smoothing of the growth surface by adding Al to the Cr solvent in SiC solution growth. In this study, the contact angles between SiC and metal solvents were measured to investigate the effect of addition of Co and Al to the Cr solvent on the morphology of the SiC crystal growth surface. The contact angles between the 4H-SiC substrate and the metal solvents at 1800°C were measured, and it was found that they were different as a result of changing the metallic species on the SiC substrate; the angle of Co- or Al-added Cr solvent was larger than that of Cr alone. When crystals were grown in Cr solvent with the addition of Co and Al, the growth surface became smoother than that of crystals grown in Cr alone. This suggests that the addition of Co and Al to the Cr solvent may contribute to the suppression of 2D nucleation and smoothing of the growth surface.

### 1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor material with excellent physical properties and is expected to be applied to high-performance electronic devices [1]. Many studies have been conducted on solvents for top-seeded solution growth (TSSG), and solvents containing Si and metals such as Cr enable high growth rates and large crystal sizes [2-4]. It is often reported that SiC crystals grown by the TSSG method from such solvents have smooth surfaces with low carbon supersaturation [5-8]. It has also been reported that the addition of Co [9], Al or Sn to Si<sub>0.6</sub>Cr<sub>0.4</sub> solvent [10] suppresses the formation of large macrosteps with step bunching while also suppressing the roughening of the crystal surface on the macroscale. The contact angle and solvent surface energy values were used to examine the frequency of 2D nucleation ( $\Delta G_{\text{two-dimensional}}$ ) considering the interfacial energy between the SiC crystal and the solvent, and it was found that the higher the interfacial energy between the SiC crystal and the solvent, the higher the frequency of 2D nucleation. [11].  $\Delta G_{\text{two-dimensional}}$  is expressed as

$$\Delta G_{\text{two-dimensional}} = -\pi \frac{r^3}{V} \Delta\mu + 2\pi r^2 \gamma_{\text{solid/liquid}} \quad (1)$$

where  $r$  and  $V$  are the radius and volume of the 2D nucleus and  $\Delta\mu$  is the change in chemical potential.  $\gamma_{\text{solid/liquid}}$  is the interfacial energy between solid and liquid and is expressed by Young's equation as eq. (2).



$$\gamma_{\text{solid/liquid}} = \gamma_{\text{solid}} - \cos\theta \cdot \gamma_{\text{liquid}} \quad (2)$$

Eq. (1) shows that as  $\gamma_{\text{solid/liquid}}$  decreases, the frequency of 2D nucleation increases. In contrast, as  $\gamma_{\text{solid/liquid}}$  increases, the frequency of 2D nucleation decreases.

We have also investigated SiC solution growth using high-density SiC ceramics as a SiC solute source without molten Si metal solvents [12]. In this method, Si and carbon are dissolved from SiC ceramics in a metallic solvent, and SiC seed crystals are brought into contact with the solution in a crucible. The SiC crystal is then recrystallized just below the SiC seed crystal. It was confirmed that SiC crystals with a thickness of several tens of micrometers can be obtained by using Cr as the metallic solvent dissolving Si and C [12]. SiC crystals are then grown in the crucible. However, severe surface roughness leading to the formation of parasitic polycrystals is a problem in this system, limiting the growth process. Both 2D nucleation and parasitic polytypes were observed on the surface of crystals grown by this technique. This feature is attributed to the high surface energy of the Cr solvent. The surface energy of pure metals and alloys is related to viscosity, and the surface energy tends to decrease with decreasing viscosity. In a previous study, a SiC crystal with a smoother surface was obtained from Cr with Al added to the solvent [13]. In this study, we added Co or Al at different compositions to the Cr solvent, measured the contact angle between SiC and the solvent metal, and evaluated the effect on the surface morphology of crystals grown by the present solution growth method from Cr solvent with 4 mol% Co or Al. The step heights of the crystals were examined to evaluate the benefits of addition of Co and Al. We also estimated the viscosity of each solvent and discussed the effect of these parameters on the frequency of 2D nucleation.

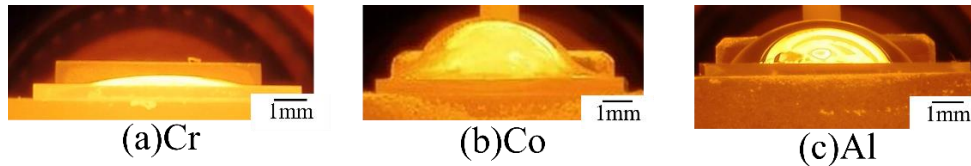
## 2. Experimental procedure

Contact angles between SiC and metal solvents were measured by placing Cr and  $\text{Cr}_{1-x}\text{M}_x$  ( $\text{M}=\text{Co}, \text{Al}, x=0, 0.02$  and  $0.04$ ) on a 4H-SiC substrate (C-face,  $8 \times 7.5 \text{ mm}^2$  in size) in an infrared lamp furnace at  $1800 \text{ }^\circ\text{C}$  in an Ar atmosphere at 1atm. Photographs of droplets on the SiC substrate were taken through an observation window and the contact angles were estimated from the photographs.

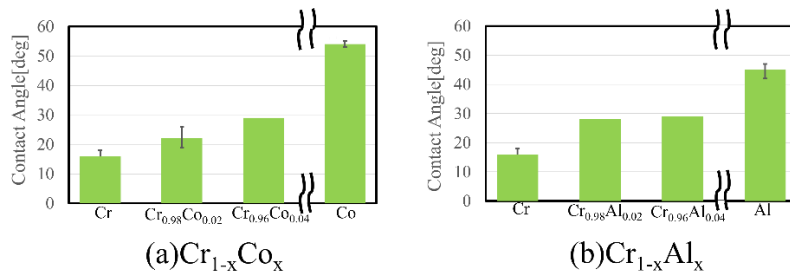
For the growth experiments, granular Cr and Co or Al were placed on a ceramic SiC feed placed at the bottom of the carbon crucible. The Co and Al compositions in the solvent were 0 and 4 mol%. The concave ceramic SiC feed had a density of  $3.14 \text{ g cm}^{-3}$  (fabricated by ASUZAC Inc., Japan), a height of 12 mm, inner diameter of 22-23 mm, outer diameter of 33-34 mm, and depth of 6 mm. The inner diameter of the carbon crucible was 34 mm. The carbon crucible was placed in a resistance heating furnace. A 4H-SiC substrate (C-face,  $8 \times 7.5 \text{ mm}^2$  in area and 330-360  $\mu\text{m}$  thick) was used as a seed crystal. The inside of the furnace was heated to the desired growth temperature under an Ar atmosphere at 1atm and the temperature was maintained for 1 or 2 h, after which the seed crystal was brought into contact with the solvent. The seed crystal was then placed on the molten metal surface to initiate crystal growth. The growth temperature was measured with thermocouples placed under the bottom of the crucible. Both the seed crystal and the crucible were rotated in opposite directions at 2 rpm during the 2 h growth period. After growth, the resulting crystal was detached from the solution and cooled to room temperature in the furnace. The liquid height, defined as the distance between the flat surface of the molten metal and the bottom surface, was constant at 3 mm for all solvents. The crystal surfaces were observed with an optical microscope (VHX-900F, Keyence Co., Japan), and step height was evaluated with a laser microscope (VK-9510, Keyence Co.).

### 3. Results and discussion

Fig. 1 shows the photographs of Cr, Co, and Al droplets taken through the observation window. It is clear that contact angles changed very markedly as a result of changing the solvent species; for example, it was small for Cr while it was large for Al and Co. The results of contact angle measurement between Cr solvent and SiC substrate with 0, 0.02, and 0.04 of Co or Al added to Cr are shown in Figs. 2 (a) and (b), respectively. The contact angle of the Cr solvent was about 15°, and it increased in spite of adding small amounts of Co or Al to the solvent.

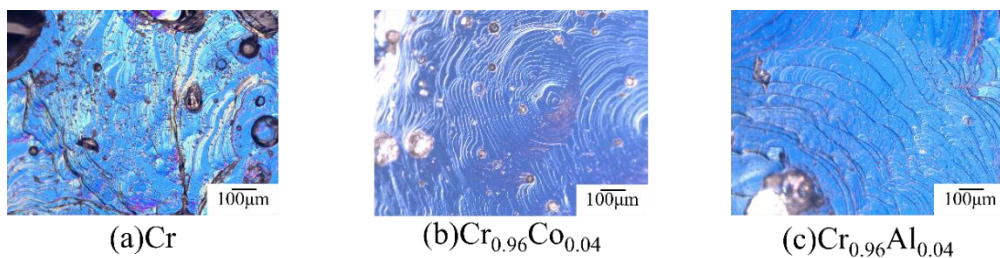


**Fig. 1.** Photographs of (a) Cr, (b) Co, (c) Al droplets on SiC substrate at 1800 °C under an Ar atmosphere at 1atm.



**Fig. 2.** Measured contact angles between solvent of Cr<sub>1-x</sub>M<sub>x</sub> (x=0, 0.02, 0.04, 1) and SiC substrate.

Figs. 3 (a), (b) and (c) show microscopic images of SiC grown crystal surfaces in Cr, Cr<sub>0.96</sub>Co<sub>0.04</sub> and Cr<sub>0.96</sub>Al<sub>0.04</sub> solvents, respectively. The crystal grown in Cr solvent showed noticeable surface roughness including solvent adhesion, whereas grown surface crystals with less solvent adhesion were obtained in Co- or Al-added solvents compared to Cr solvent. Table 2 summarizes the growth thickness, growth rate, and step height of the grown surface. It was found that smoother crystal surfaces were obtained in both Co- and Al-added solvents than in Cr solvent alone.



**Fig. 3.** Optical micrographs of grown crystals in (a) Cr, (b) Cr<sub>0.96</sub>Co<sub>0.04</sub>, (c) Cr<sub>0.96</sub>Al<sub>0.04</sub> solvents.

**Table 1.** Thickness, growth rate and average step height of grown crystals.

	Cr	Cr <sub>0.96</sub> Co <sub>0.04</sub>	Cr <sub>0.96</sub> Al <sub>0.04</sub>
Thickness[ $\mu\text{m}$ ]	187	148	146
Growth rate [ $\mu\text{m}/\text{h}$ ]	187	74	73
Average step height[ $\mu\text{m}$ ]	4.0	1.9	1.0

The obtained experimental results are discussed from the viewpoint of the frequency of 2D nucleation. The results appear to indicate that the addition of Co or Al, with a large contact angle against SiC, to Cr solvent increased the interfacial energy,  $\gamma_{\text{solid/liquid}}$ , in eq. (2), then increased the 2D nucleation energy,  $\Delta G_{\text{two-dimensional}}$ , in eq. (1) and finally led to a decrease in the frequency of 2D nucleation and smoothed the crystal surface. That is, these results suggest that the addition of Co or Al to Cr solvent is an effective technique for SiC crystal growth from metal solvents in terms of surface morphology stability.

#### 4. Conclusion

In this study, the contact angles between SiC and metal solvents were measured to investigate the effect of Co and Al addition to Cr solvent on the morphology of the SiC crystal growth surface. Contact angles of Co and Al on a SiC substrate were large in comparison with that of Cr, and the SiC crystal surfaces grown in Co- or Al-added Cr solvent were smoother than those grown in Cr solvent alone. These results suggest that the addition of Co or Al to Cr solvent is an effective technique for SiC crystal growth from metal solvents in terms of surface morphology stability.

#### Acknowledgement

This work was supported in part by Grant-in-Aid for Scientific Research B (20H02637).

#### REFERENCES

- [1] H. Matsunami and T. Kimoto, *Mater. Sci. eng. R* 20 (1997) 125.
- [2] S. Harada et al., *Acta Mater.* 81, (2014) 284.
- [3] T. Narumi et al., *J. Cryst. Growth* 408, (2014) 25.
- [4] H. Daikoku et al., *Cryst Growth Des.* 16, (2016) 1256.
- [5] K. Seki, et al., *J. Cryst Growth* 360, (2012) 176.
- [6] N. Komatsu et al., *Mater. Sci. Forum* 740-742, (2013) 23.
- [7] W. K. Burton et al., *Philos. Trans. R. Soc. Lond., Ser. A* 243, (1951) 299.
- [8] D. Elwell and H.J. Scheel, *Crystal from High-Temperature Solutions* (Academic, New York, 1975).
- [9] K. Hyun et al., *Applied Surface Science* 513 (2020) 145798.
- [10] T. Mitani et al., *J. Cryst. Growth* 423 (2015) 45.
- [11] N. Komatsu et al., *J. Cryst. Growth* 458 (2017) 37.
- [12] K. Suzuki, et al., *Mater. Sci. Forum* 924, (2018) 35.
- [13] K. Suzuki et al., *Jpn. J. Appl. Phys* 59 (2020) 025504.

## Evaluation of Thermal Conductivity Characteristics near Insulator/SOI Interface by Raman Spectroscopy

K. Sahara<sup>1\*</sup>, R. Yokogawa<sup>1,2</sup>, M. Tomita<sup>3</sup>, T. Watanabe<sup>3</sup>, and A. Ogura<sup>1,2</sup>

1. School of Science and Technology, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa 214-8571, Japan

2. Meiji Renewable Energy Laboratory, Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, Kanagawa 214-8571, Japan

3. Faculty of Science and Engineering, Waseda University, Shinjuku, Tokyo 169-8555, Japan

e-mail: ce211027@meiji.ac.jp

### Abstract

We evaluated thermal conductivity characteristics near the insulator/SOI (Silicon on Insulator) interfaces with various insulators ( $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{MgO}$ , and  $\text{HfO}_2$ ) on SOI by Raman spectroscopy. It was confirmed thermal conductivity characteristics near insulator/SOI interfaces have rare influence on the thermal conductivity of insulator. Interface properties seem to play more significant role for the thermal conductivity.  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$  may be attractive materials that will greatly contribute to achieving even lower thermal conductivity in insulator/Si nanowires since  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$ /SOI samples show lower thermal conductivity properties than  $\text{SiO}_2$ /SOI. The results are important findings for the realization of next-generation thermoelectric devices.

### Introduction

Silicon nanowires (Si NWs) are attractive thermoelectric materials owing to their significantly lower thermal conductivity than bulk silicon [1-3]. In order to obtain high thermoelectric conversion efficiency, high dimensionless performance index ( $ZT = S^2\sigma T/\kappa$ ) is desired, where  $S$  is the Seebeck coefficient,  $\sigma$  is the electric conductivity, and  $T$  is the absolute temperature. Therefore, it is necessary to reduce the thermal conductivity of Si NWs further for the next-generation thermoelectric devices.

The strain states in Si NWs affects both the carrier mobility and thermal conductivity [4, 5]. In addition, it has been shown by molecular dynamics (MD) simulation that the thermal conductivity of Si NWs covered with oxide films are further reduced due to the disorder vibrations near  $\text{SiO}_2$ /Si interface [6-8]. However, the relationship between the interface state and the thermal conductivity characteristics near insulator/Si interface other than oxide films have not been investigated yet. For further reduction of the thermal conductivity of Si NWs, immediate clarification is required. In this study, we evaluated the thermal conductivity characteristics and the interface state near the insulator/SOI (Silicon on Insulator) interface with various insulators on SOI by Raman spectroscopy.

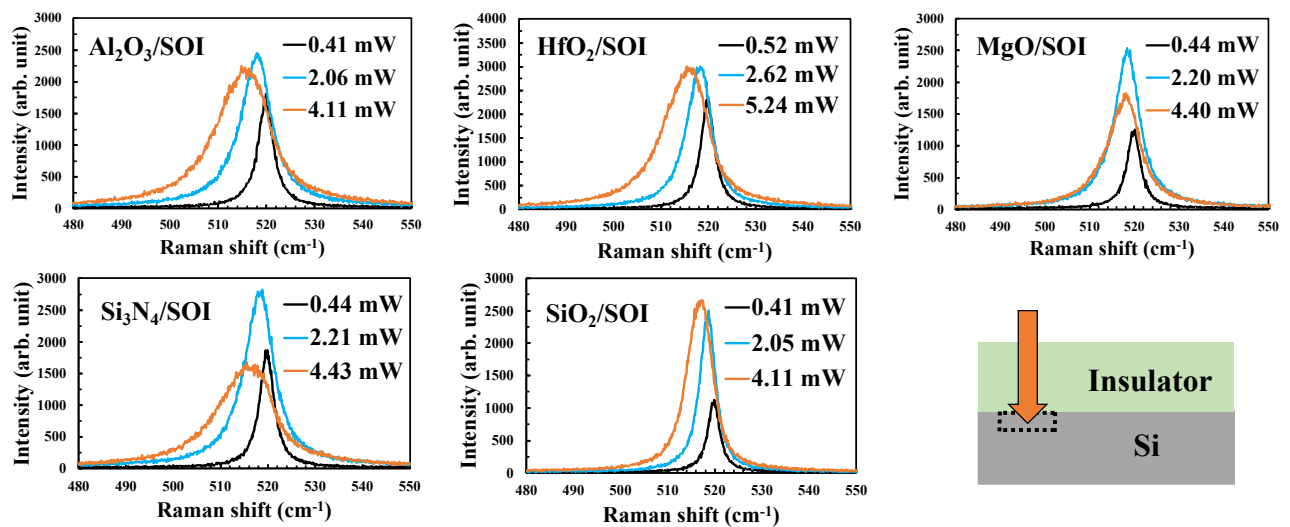
### Experimental methods

Various 30 nm thick insulator films ( $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{MgO}$ , and  $\text{HfO}_2$ ) were deposited by sputtering on a (001)-oriented SOI substrate (SOI thickness: 70 nm and buried oxide thickness: 145 nm). The focal length of the Raman spectrometer, the number of grating, and the wavenumber resolution were 2000 mm,  $3600 \text{ mm}^{-1}$ , and  $0.1 \text{ cm}^{-1}$ , respectively. The excitation source was a ultra violet ( $\lambda = 355 \text{ nm}$ ) laser with a penetration depth in the bulk Si of approximately 5 nm under the backscattering geometry. For the thermal conductivity measurement, the laser

power was controlled by a variable neutral density filter in the incident light path [9]. The exposure time of the UV excitation light was 30s. Finally, the laser powers were calibrated in consideration of the reflectance from each sample.

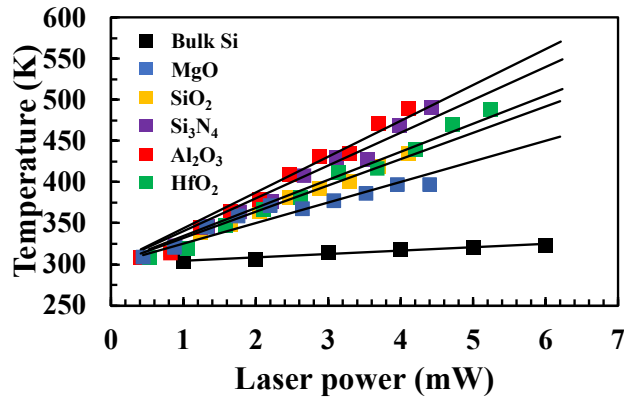
## Results and discussion

Figure 1 shows the laser power dependence of Raman spectra derived from Si-Si vibration mode from insulator/SOI samples. From Fig. 1, it was confirmed the Raman spectrum for Si-Si mode tends to shift toward a lower wavenumber with increasing laser power. It has been reported there is a close relationship between the Raman spectra and the lattice vibration that contributes to thermal transport. Therefore, Si atoms which were thermally expanded by the laser-excited heat contribute to the decrease in the vibrational frequency. In addition, we analyzed thermal conductivity characteristics by peak fitting of the Raman spectra with the Lorentz function



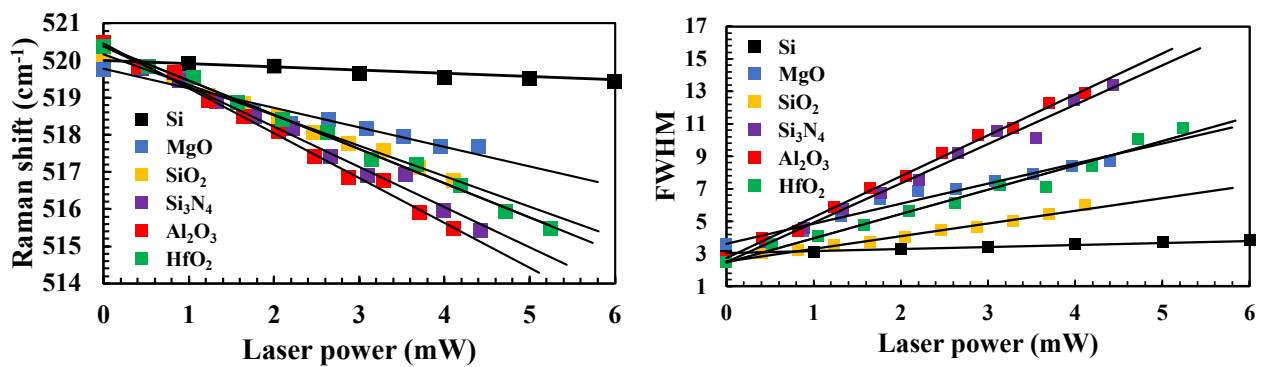
**Fig. 1.** Laser power dependence of Raman spectra derived from Si-Si vibration mode for insulator/SOI samples.

Figure 2 shows the laser power dependence of temperature in the SOI layer of the samples estimated by the relationship between Raman shift  $\omega$  of Si and temperature  $T$  ( $d\omega/dT = -0.024$  [cm<sup>-1</sup>/K]) [10]. Since there is a close relationship between the thermal diffusion and the increase in temperature, the steeper the slope shows the lower the thermal conductivity characteristics. From Fig. 2, it is clarified each sample has different thermal conductivity characteristics near the insulator/SOI interface. This result shows thermal conductivity characteristics near the insulator/SOI interface have rare influence on the thermal conductivity of the insulator. Our group have previously reported SiO<sub>2</sub>/Si NWs fabricated by different oxidation processes using Raman spectroscopy [11]. It is clarified that the poor interface state caused by strains or defects has an impact on thermal conductivity characteristics. From the above, we attempted to evaluate the interface state at the insulator/SOI interface in order to clarify the cause of different thermal conductivity characteristics.



**Fig. 2.** Laser power dependence of temperature for top Si layer of SOI samples.

Figure 3 shows the laser power dependence of Raman shift and FWHM for insulator/SOI samples. In Fig. 3, the zero-power intercept shows Raman shift and FWHM which were not affected by local laser heating. We summarized the results in Table 1. From Table 1, The FWHMs of Raman spectra in  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$ , and  $\text{HfO}_2$ /SOI samples have almost equivalent to that of pure-Si. However, in  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$ , and  $\text{HfO}_2$ /SOI samples, the Raman peak shows a higher wavenumber than that of pure-Si. These results indicated  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2$ , and  $\text{HfO}_2$ /SOI samples have compressive strain [12]. Hence, it can be considered that the thermal conductivity characteristics in these samples are further reduced due to the disorder vibrations near the insulator/SOI interface caused by the compressive strain. From the above,  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$ /SOI samples show lower thermal conductivity characteristics compared to  $\text{SiO}_2$ /SOI despite the fact that these samples show almost equivalent interface states. Therefore,  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$  may be attractive materials that will greatly contribute to achieve even lower thermal conductivity in Si NWs. The results are important findings for the realization of the next-generation electric and thermoelectric devices.



**Fig. 3.** Laser power dependent Raman shift and FWHM for insulator/SOI samples.

**Table 1** Raman shift and FWHM for insulator/SOI samples at zero-power intercept.

	MgO	$\text{Al}_2\text{O}_3$	$\text{Si}_3\text{N}_4$	$\text{HfO}_2$	$\text{SiO}_2$	Si
FWHM	3.6	2.7	2.5	2.5	2.5	2.6
Raman shift ( $\text{cm}^{-1}$ )	519.8	520.5	520.4	520.4	520.2	520.0

## Conclusions

We evaluated thermal conductivity characteristics near the insulator/SOI (Silicon on Insulator) interface with various insulators ( $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{MgO}$ , and  $\text{HfO}_2$ ) on SOI by Raman spectroscopy. It was confirmed thermal conductivity characteristics near the insulator/SOI interface have rare influence on the thermal conductivity of the insulator. In addition, we evaluated the interface states of insulator/SOI samples in order to clarify the cause of different thermal conductivity characteristics. As a result,  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$ /SOI samples show lower thermal conductivity characteristics compared to  $\text{SiO}_2$ /SOI. It can be considered the thermal conductivity characteristics in these samples are further reduced due to the disorder vibrations caused by the compressive strain near the insulator/SOI interface. Therefore,  $\text{Al}_2\text{O}_3$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{HfO}_2$  may be attractive materials that will greatly contribute to achieving even lower thermal conductivity in Si NWs. The results are important findings for the realization of next-generation thermoelectric devices.

## Acknowledgments

This work was partly supported by JST-CREST(JPMJCR19Q5).

## Reference

1. M. Kazan, G. Guisbiers, S. Pereira, M. R. Correia, P. Masri, A. Bruyant, S. Volz, and P. Royer, *J. Appl. Phys.* **107**, 083503 (2010).
2. K. Kukita, I. N. Adisusilo, and Y. Kamakura, *Jpn. J. Appl. Phys.* **53**, 015001 (2014).
3. Y. Zhou and M. Hu, *Nano Lett.*, **16**, 6178 (2016).
4. A. Seike, T. Tange, Y. Sugita, I. Tsuchida, H. Ohta, T. Watanabe, D. Kosemura, A. Ogura, and I. Ohdomari, *Jpn. J. Appl. Phys.* **91**, 202117 (2007).
5. D. Fan, H. Sigg, R. Spolenak, and Y. Ekinci, *Phys. Rev. B* **96**, 115307 (2017).
6. T. Zushi, K. Shimura, M. Tomita, K. Ohdomari, K. Yamada, and T. Watanabe, *ECS J. Solid State Sci. Technol.* **3**, P149 (2014).
7. T. Zushi, K. Ohdomari, K. Yamada, and T. Watanabe, *Phys. Rev. B* **91**, 115308 (2015).
8. T. Watanabe, T. Zushi, M. Tomita, R. Kuriyama, N. Aoki, and T. Kamioka, *ECS Trans.* **50** [9], 673 (2013).
9. H. Takeuchi, R. Yokogawa, K. Takahashi, K. Komori, T. Morimoto, Y. Yamashita, N. Sawamoto, and A. Ogura, *Jpn. J. Appl. Phys.* **59**, 075501 (2020).
10. H. H. Burke and I. P. Herman, *Phys. Rev. B* **48**, 15016 (1993).
11. R. Yokogawa, S. Hashimoto, S. Asada, M. Tomita, T. Watanabe, and A. Ogura, *Jpn. J. Appl. Phys.* **56**, 06GG10 (2017).
12. A. Ogura, D. Kosemura, M. Takei, H. Uchida, N. Hattori, M. Yoshimaru, S. Mayuzumi, and H. Wakabayashi, *Mater. Sci. Eng. B* **159**, 206 (2009).

## PL spectra analyses of strain-free GeSn with high Sn fraction

Yuta Ito<sup>1\*</sup>, Shizuru Matsunaga<sup>1</sup>, Ryo Yokogawa<sup>1,2</sup>, Naomi Sawamoto<sup>2</sup>, Yosuke Shimura<sup>3,4</sup>, Roger Loo<sup>4</sup>, Anurag Vohra<sup>4,5</sup>, and Atsushi Ogura<sup>1,2</sup>

<sup>1</sup> School of Sci.&Tech., Meiji University, 1-1-1 Higashimita, Tama-ku, Kawasaki, 214-8571, Japan

<sup>2</sup> Meiji Renewable Energy Laboratory, 1-1-1 Higashimita, Tama-ku, Kawasaki, 214-8571, Japan

<sup>3</sup> Shizuoka University, Research Institute of Electrons, 3-5-1 Johoku Naka-ku, Hamamatsu, 432-8011, Japan

<sup>4</sup> Imec, Kapeldreef 75, 3001 Leuven, Belgium

<sup>5</sup> K. U. Leuven, Dept of Physics, Celestijnenlaan 200D, 3001 Leuven, Belgium

e-mail: ce221012@meiji.ac.jp

### Abstract

We performed Photoluminescence (PL) measurements for the GeSn film with Sn fraction of 9% on the Ge buffer layer/Si substrate. We found that the PL spectrum at 50 K has two peaks at approximately 0.61 eV and 0.59 eV (hereinafter referred to as Peak 1 and Peak 2). Peak 1 and Peak 2 are in good agreement with the Maxwell-Boltzmann and the Gaussian distribution function by PL spectrum fitting, respectively. As a second analysis, we measured the PL intensity dependence on the excitation light intensity to investigate the origins of Peak 1 and Peak 2 in detail. The relationship between PL intensity  $I_{PL}$  and excitation light intensity  $I_{ex}$  can be described as  $I_{PL} \propto I_{ex}^n$ , where the power exponent  $n$  indicates the PL intensity dependence on excitation light intensity. From this analysis, Peak 1 and Peak 2 have a quadratic dependence and a linear dependence, respectively. Therefore, Peak 1 can be regarded as the band-to-band luminescence while Peak 2 should be the impurity or defect level luminescence from the viewpoints of peak shape and excitation intensity dependence. In this paper, we have revealed the PL peaks origin and showed the experimental data and analysis of the strain-free GeSn.

### Introduction

In recent years, the amount of information handled in the world is increasing enormously, and the silicon (Si) photonics is attracting attention as a technology for the high-speed communications [1]. Si is not suitable for the material used for the optical component in the waveguides of Si photonics since Si has poor luminescence efficiency, and the best materials are explored [2]. Some III-V semiconductor materials have excellent luminescence efficiency, therefore the possibility to apply to the Si photonics has been studied [3,4]. However, these materials are not suitable for applying Si photonics devices because of the poor compatibility with Si process [5-8]. It is reported that high-density dislocations as well as the other defects are formed during the III-V material growths on Si [5]. For this reason, modulating to the direct transition type for group IV materials has been focused on, and especially germanium (Ge) has been researched for light emitting devices [9] since the energy difference of the conduction band energy  $\Gamma$ -valley and L-valley is only 0.136 eV [4]. Strain-free Ge is an indirect transition type, but it can be modulated to a direct transition type by applying tensile strain or tin (Sn) doping [7-9]. There are many previous studies of GeSn [10-18], but the effects of doping Sn and strain are unclear experimentally, and accurate Sn fraction of crossover point to direct type is unknown. Similar research was performed in the poly SiSn, but it is reported that it needs much higher Sn fraction approximately 30-50% [19-21]. In contrast, GeSn needs Sn fraction of approximately 9-11% [10-16], and it has been already applied for infrared



laser since it is easy to modulate to direct transition type [22]. Therefore, the evaluation of strain-free GeSn can be an important reference for the research of Si photonics with GeSn. In this study, we evaluated strain-free and high crystal quality GeSn by Photoluminescence (PL) spectroscopy.

## Experiments

We prepared strain-free GeSn with 9% Sn fraction. The GeSn film (thickness: 870 nm) was epitaxially grown on the Ge buffer layer (thickness: 1  $\mu\text{m}$ )/Si substrate (thickness: 0.7 mm) by a low-pressure chemical vapor deposition (CVD) method. The Sn fraction was confirmed by Rutherford backscattering spectroscopy (RBS) and X-ray diffraction (XRD), and the strain state was confirmed by XRD [23].

We have used the PL spectrometer with the extended InGaAs diode array detector, which has sensitivity from 0.9 to 2.2  $\mu\text{m}$ . This spectrometer can control the stage temperature from 4-300 K with a helium compressor and a heater device. The excitation source is a diode pumped solid-state (DPSS) laser with wavelength: 532 nm. We selected the wide slit to obtain the higher PL intensity, and the wavelength resolution is approximately 41 nm.

## Results and Discussion

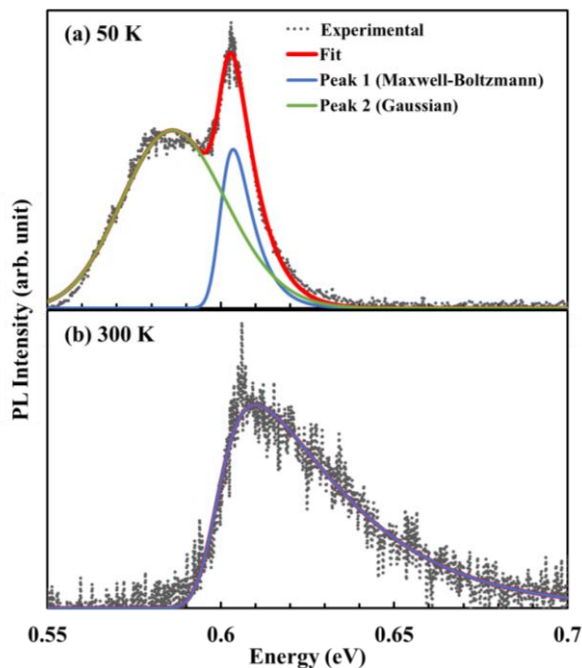


Fig. 1. PL spectra and fit to experimental data at (a) 50 K and (b) 300 K of strain-free GeSn (Sn 9%).

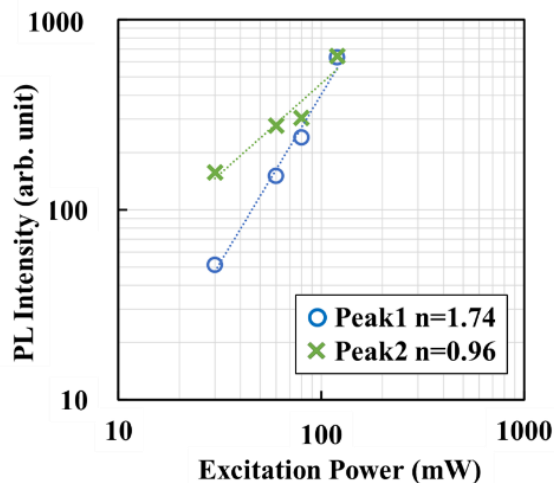


Fig. 2. PL peak intensity dependence on excitation power at 65 K.

It has been reported that a PL spectrum derived from band-to-band luminescence is in good agreement with the Maxwell-Boltzmann distribution function since it is related to carrier density in theory [24]. On the other hand, a PL spectrum derived from defects and impurity-related luminescence reflects a certain level under the effects of the wavefunction, the lattice vibration, and the resolution of the spectrometer. Therefore, the PL spectrum shape derived from a localized level is in mostly good agreement with the Gaussian distribution function. In previous studies, the Gaussian distribution function was mostly used in the spectra fitting for localized level luminescence [25,26]. In this study, we used both the Maxwell-Boltzmann distribution and Gaussian distribution for PL spectra fitting. Figure 1 (a) and (b) shows the PL spectra of strain-free GeSn at 50 K and 300 K, respectively. We found the PL

spectrum at 300 K has peak at approximately 0.61 eV. This peak does not derive from the Ge buffer since the energy level does not fit to any luminescence from bulk Ge [27]. Furthermore, the penetration depth of the 532 nm laser is approximately 21 nm in GeSn with Sn fraction of 9% [28], and it is no problem to discuss the PL spectrum obtained from this experiment as PL from the GeSn film. In addition, we found the PL spectrum at 50 K has two peaks at approximately 0.61 and 0.59 eV (hereinafter referred to as Peak 1 and Peak 2). As a result of our fitting, Peak 1 and Peak 2 are good agreement with the Maxwell-Boltzmann distribution and Gaussian distribution, respectively at each temperature. Therefore, we consider that Peak 1 and Peak 2 are derived from band-to-band luminescence and defect and impurity-related luminescence, respectively, for strain-free GeSn film. In addition, full-width-at-half-maximum (FWHM) of Peak 1 becomes broader with increasing temperature in the principle of band-to-band luminescence [24]. In general, defects and impurity-related luminescence has a sharp shape spectrum since it is the emission from a localized energy level. However, Peak 2 has too wide FWHM as localized level luminescence. There is a possibility that Peak 2 is the high-dope-impurity-related luminescence [29].

Figure 2 shows the PL peak intensity dependence on the excitation power of the strain-free GeSn sample. The relationship between PL intensity  $I_{PL}$  and excitation intensity  $I_{ex}$  can be described as  $I_{PL} \propto I_{ex}^n$  where  $I_{PL}$  is the PL intensity, and  $I_{ex}$  is the the excitation laser radiation power. In the case of band-to-band luminescence, the relation should show a quadratic dependence, and the exponent  $n$  is between 1 and 2. While in the case of defects and impurity-related luminescence, the dependence shows a liner dependence, and the exponent  $n$  is close to 1 or less [30-33]. As shown in Figure 2, the exponents  $n$  for Peak 1 and Peak 2 are 1.74 and 0.96, respectively. For these reasons, we consider that there is a possibility that Peak 1 is band-to-band luminescence and the Peak 2 is defects or impurity-related luminescence.

## Conclusions

In this paper, we have discussed the origin of PL spectra of strain-free GeSn with Sn fraction of 9%. Two peaks were observed at 50 K in the PL experimental spectra data (the lower energy peak is 0.59 eV, and the higher energy peak is 0.61 eV). We have revealed that the lower energy peak and the higher energy peak are good agreement with the Gaussian and the Maxwell-Boltzmann distribution function by the PL spectrum fitting. For the investigation of PL intensity dependence on excitation laser power, the integral intensity of the lower energy peak has a quadratic dependence, and the higher energy peak has a liner dependence. From these analyses, we consider the lower energy peak is high-dope-impurity-related luminescence, and the higher energy peak is band-to-band luminescence.

## REFERENCES

- [1] S. Y. Siew, B. Li, F. Gao, H. Y. Zheng, W. Zhang, P. Guo, S. W. Xie, A. Song, B. Dong, L. W. Luo, C. Li, X. Luo, Senior Member, IEEE, and G. -Q. Lo, J. Light. Technol. **39**, 4374 (2021).
- [2] R. Geiger, T. Zabel, and H. Sigg, Front. Mater. **2**, 1 (2015).
- [3] J. P. Reithmaier, and M. Benyoucef, ECS Trans. **72**, 171 (2016).
- [4] W. Xie, C. Xiang, L. Chang, W. Jin, J. Peters, and J. E. Bowers, Photonics Res. **10**, 535 (2022).
- [5] J. Liu, Photonics **1**, 162 (2014).
- [6] Y. Miao, G. Wang, Z. Kong, B. Xu, X. Zhao, X. Luo, H. Lin, Y. Dong, B. Lu, L. Dong, J. Zhao, J. Liu, and H. H. Radamson, Nanomaterials **11**, 2556 (2021).

- [7] S. Zaima, *Jpn. J. Appl. Phys.* **52**, 1 (2013).
- [8] J. Michel, J. Liu, and L. C. Kimerling, *Nat. Photonics* **4**, 527 (2010).
- [9] P. H. Lim, S. Park, Y. Ishikawa, and K. Wada, *Opt. Express* **17**, 16538 (2009).
- [10] S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonik, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grützmacher, *Nat. Photonics* **9**, 88 (2015).
- [11] R. Chen, H. Lin, Y. Huo, C. Hitzman, T. I. Kamins, and J. S. Harris, *Appl. Phys. Lett.* **99**, 181125 (2011).
- [12] S. A. Ghetmiri, W. Du, B. R. Conley, A. Mosleh, A. Nazzal, G. Sun, R. A. Soref, J. Margetis, J. Tolle, H. A. Naseem, and S. -Q. Yu, *J. Vac. Sci. Technol. B* **32**, 060601 (2014).
- [13] T. R. Harris, M. -Y. Ryu, Y. K. Yeo, B. Wang, C. L. Senaratne, and J. Kouvetakis, *J. Appl. Phys.* **120**, 085706 (2016).
- [14] V. R. D'Costa, C. S. Cook, A. G. Birdwell, C. L. Littler, M. Canonico, S. Zollner, J. Kouvetakis, and J. Menendez, *Phys. Rev. B* **73**, 125207 (2006).
- [15] S. A. Ghetmiri, W. Du, J. Margetis, A. Mosleh, L. Cousar, B. R. Conley, L. Domulevicz, A. Nazzal, G. Sun, R. A. Soref, J. Tolle, B. Li, H. A. Naseem, and S. -Q. Yu, *Appl. Phys. Lett.* **105**, 151109 (2014).
- [16] K. L. Low, Y. Yang, H. Han, W. Fan, and Y. -C. Yeo, *J. Appl. Phys.* **112**, 103715 (2012).
- [17] W. Huang, B. Cheng, C. Xue, and Z. Liu, *J. Appl. Phys.* **118**, 165704 (2015).
- [18] E. Kasper, M. Kittler, M. Oehme, and T. Arguirov, *Photonic Res.* **1**, 69 (2013).
- [19] J. Tolle, A. V. G. Chizmeshya, Y. -Y. Fang, J. Kouvetakis, V. R. D'Costa, C. -W. Hu, J. Menéndez, and I. S. T. Tsong, *Appl. Phys. Lett.* **89**, 231924 (2006).
- [20] Y. Nagae, M. Kurosawa, S. Shibayama, M. Araida, M. Sakashita, O. Nakatsuka, K. Shiraishi, and S. Zaima, *Jpn. J. Appl. Phys.* **55**, 08PE04 (2016).
- [21] R. Soref, *Opt. Mater. Express* **4**, 836 (2014).
- [22] R. Soref, *Nat. Photonics* **4**, 495 (2010).
- [23] R. Loo, Y. Shimura, S. Ike, A. Vohra, T. Stoica, D. Stange, D. Buca, D. Kohen, J. Margetis, and J. Tolle, *Semicond. Sci. Technol.* **33**, 1 (2018).
- [24] Pelant, J. Dian, J. Matousková, J. Hála, M. Ambroz, M. Vácha, and V. Kohlová, *J. Appl. Phys.* **73**, 3472 (1993).
- [25] E. Abdoli, and H. Haratizadeh, *Phys. Status Solidi B* **247**, 170 (2010).
- [26] D. Denzler, M. Olschewski, and K. Sattler, *J. Appl. Phys.* **84**, 2841 (1998).
- [27] P. R. Lieten, K. Bustillo, T. Smets, E. Simoen, J. W. Ager III, E. E. Haller, and J. -P. Locquet, *Phys. Rev. B* **86**, 035204 (2012).
- [28] P. C. Grant, J. Margetis, W. Du, Y. Zhou, W. Dou, G. Abernathy, A. Kuchuk, B. Li, J. Tolle, J. Liu, G. Sum, R. A. Soref, M. Mortazavi, and S. -Q. Yu, *Nanotechnology* **29**, 465201 (2018).
- [29] H. T. Nguyen, and D. Macdonald, *J. Lumin.* **181**, 223 (2017).
- [30] Y. Kawamura, K. C. Huang, S. V. Thombare, S. Hu, M. Gunji, T. Ishikawa, M. L. Brongersma, K. M. Itoh, and P. C. McIntyre, *Phys. Rev. B* **86**, 035306 (2012).
- [31] S. Asahara, M. Tajima, Y. Satake, and A. Ogura, *Jpn. J. Appl. Phys.* **59**, 106502 (2020).
- [32] T. Taguchi, J. Shirafuji, and Y. Inuishi, *Phys. Status Solidi B* **68**, 727 (1975).
- [33] H. J. Hovel, IEEE Member, and D. Guigotti, *IEEE Trans. Electron Devices* **32**, 2331 (1985).

# A Linear-Regression Machine-Learning Model for Predicting Total Energies of Silicon Crystal Structures

Yusuke Noda<sup>1\*</sup>, Eiji Kamiyama<sup>1,2</sup>, Koji Sueoka<sup>1</sup>

<sup>1</sup>*Department of Information and Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan*

<sup>2</sup>*Technology, GlobalWafers Japan Co., Ltd., 6-861-5 Higashiko, Seiro, Niigata 957-0197, Japan*

e-mail: noda@c.oka-pu.ac.jp

## Abstract

We proposed a novel method of machine-learning model based on partial least squares (PLS) regression for predicting total energies of crystal structures evaluated from density functional theory (DFT) calculations. In this study, three different atomic descriptors: radial distribution function (RDF), angular distribution function (ADF), and two-dimensional histogram (2DH) of atomic distance vs. atomic angle as explanatory variables of our PLS models were considered. We confirmed that our PLS model with RDF + ADF descriptors exhibits better performance of total energy prediction for various silicon structures.

## 1. Introduction

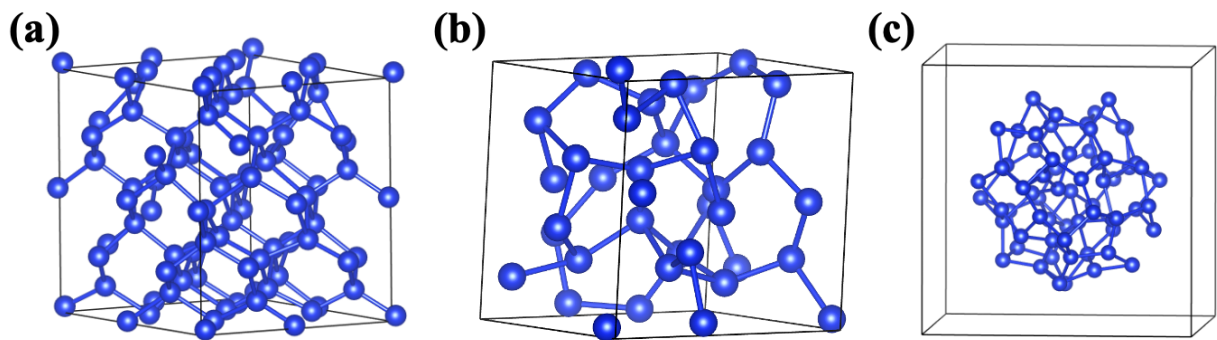
In the field of computational materials science, density functional theory (DFT) calculations have become mainstream as electronic-state calculations on atomic and molecular scales. DFT calculations can solve electronic states based on the basic principles of quantum mechanics, and thus are used in a wide range of research fields. However, since the computational cost of DFT calculations is generally proportional to the cube of the number of atoms, it is hard to handle large-scale crystal structures with several hundreds and thousands of atoms or more in DFT calculations unless sufficient computational resources are available.

To overcome this problem, in recent years, large-scale materials simulations using interatomic potentials have attracted much attention. Such interatomic potentials are often constructed by machine-learning methods with training data obtained from DFT calculations [1]. An artificial neural network (ANN)-based interatomic potential [2-4] and Gaussian approximation potential (GAP) [5,6] method based on Bayesian inference (Gaussian process regression) have been developed as representative machine-learning interatomic potentials. Both algorithms can construct machine-learning models that predict the total energies of crystal structures and interatomic forces with high accuracy through a regression using more complex functions. However, in the ANN interatomic potential, it is very difficult to appropriately determine the hyperparameters (the number of hidden layers and the number of hidden nodes, etc.) that affect the accuracy of the ANN model, and therefore the computational cost of machine learning to optimize the ANN model becomes higher. Similarly, in the GAP method, many of the training data are called every time a physical quantity such as the total energy for an unknown crystal structure is predicted. Therefore, it has the disadvantage that it takes a huge time to construct the interatomic potential.

To solve the above-mentioned problems in the existing methods, we aim to develop interatomic potentials by applying a machine-learning method that are different from previous research. As the first step, we verify the accuracy of our machine-learning model based on a linear-regression analysis method on the total energy prediction of silicon (Si) crystal structures in this study.

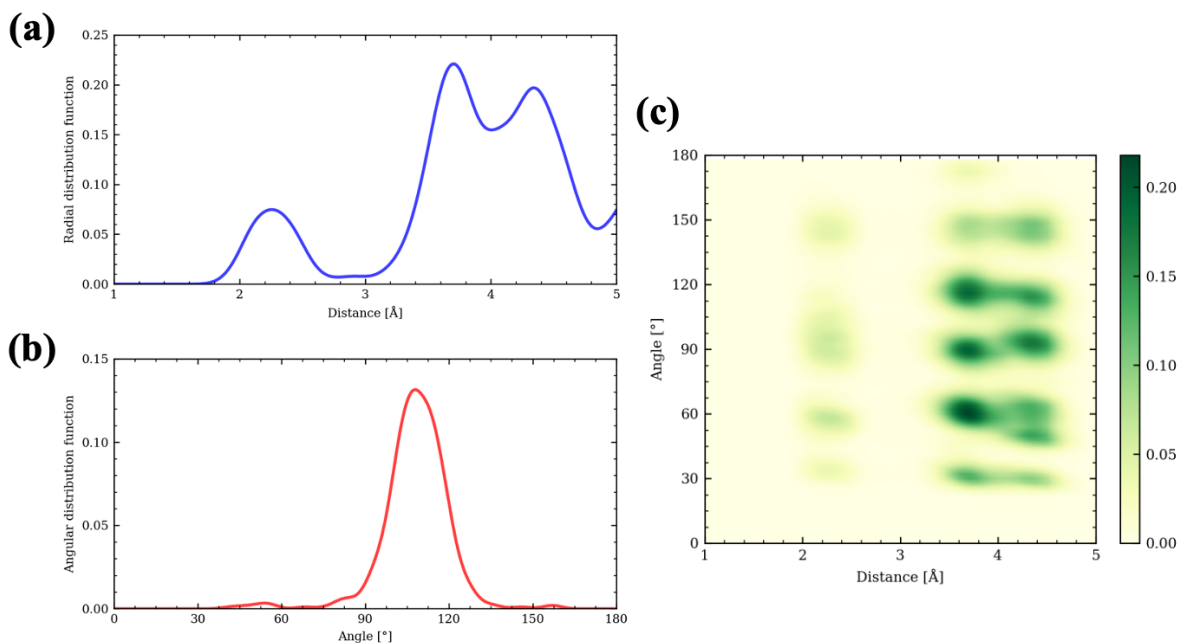
## 2. Methodology

At first, we performed DFT calculations in advance for various morphologies of Si structures (diamond-type crystal structures, amorphous structures, and atomic clusters; see Figure 1), and calculated descriptors representing the atomic environment of each atom in each structure and the total energy of crystal structures. In this study, the radial distribution function (RDF) with a range of 1.0–5.0 [Å] and a width of 0.01 [Å] (i.e. 400 values), angular distribution function (ADF) with a range of 0–180 [°] and the width of 1 [°] (i.e. 180 values), and two-dimensional histogram (2DH) of atomic distance with the range of 1.0–5.0 [Å] and the width of 0.01 [Å] vs. atomic angle with the range of 0–180 [°] and the width of 2 [°] (i.e. 400×90 = 36,000 values) were calculated. Figure 2 shows examples of those atomic descriptors for a diamond-type Si crystal structure. We generated 30,730 training data of various Si structures in total.



**Fig. 1.** Si structure models for the training dataset.

(a) a diamond-type crystal structure, (b) an amorphous structure, and (c) an atomic cluster.



**Fig. 2.** Examples of atomic descriptors for a diamond-type Si crystal structure.

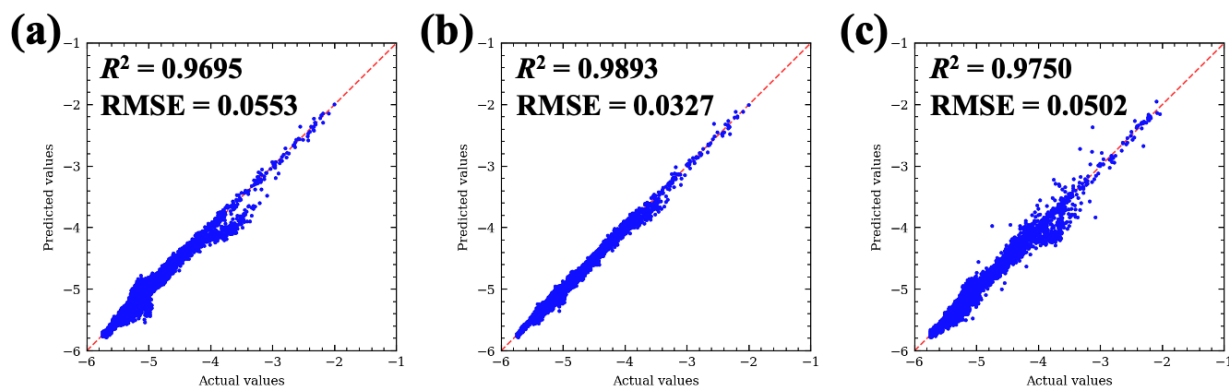
(a) RDF, (b) ADF, and (c) 2DH of atomic distance vs. atomic angle.

Next, we constructed prediction models for learning the training data of all DFT energies using partial least squares (PLS) [7], which has been well known as one of the multivariate regression analysis methods. The PLS is one of the regression models based on a linear function, and machine learning can be performed at a low cost since the PLS handles only simple arithmetic operations such as sums and multiplications of vectors and matrices. We constructed three types of PLS models with different atomic descriptors: RDF, RDF + ADF, and 2DH of atomic distance vs. atomic angle. A 5-fold cross-validation scheme was adopted for constructing those PLS models.

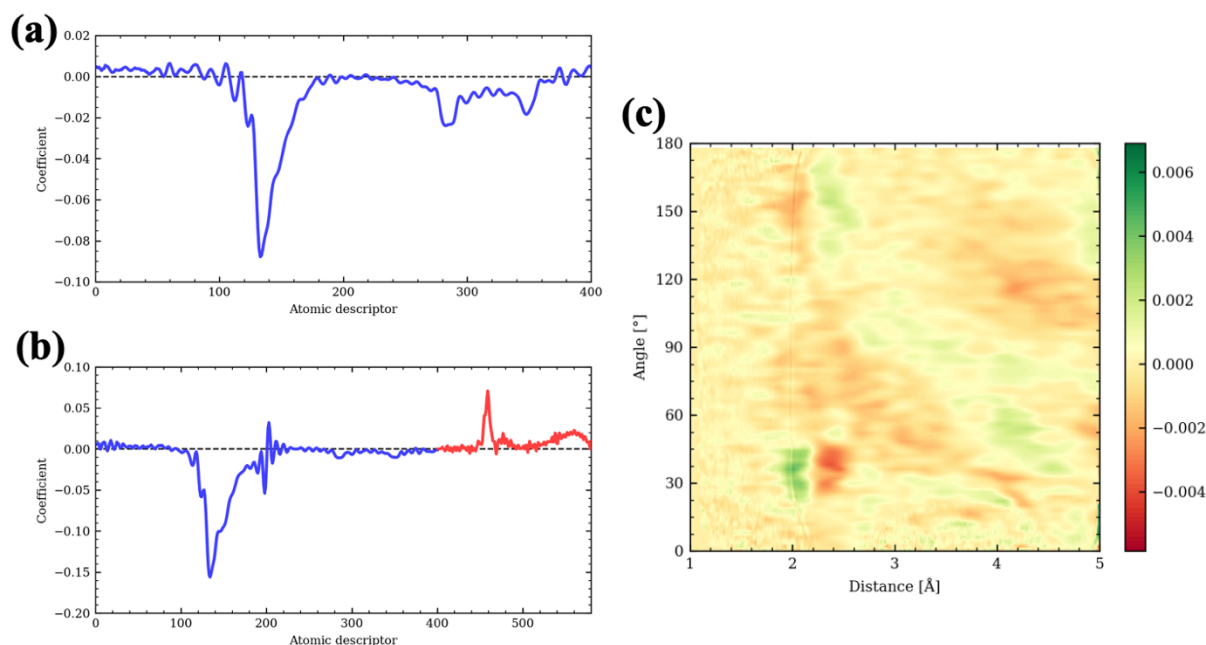
### 3. Results and discussion

Figure 3 shows the prediction accuracy of the total energies of training data evaluated by our PLS model, which exhibits fairly good accuracy for predicting the total energies of Si crystal structures. The prediction performance of the PLS model with RDF + ADF descriptors (coefficient of determination  $R^2 = 0.9893$  and root-mean-square error (RMSE) = 0.0327) is better than that of the other PLS models. However, the PLS model does not exhibit better performance than machine-learning interatomic potentials proposed by previous studies [4,6]. To make matters worse, the prediction accuracy of the PLS model with the 2DH descriptors turned out worse ( $R^2 = 0.9750$  and RMSE = 0.0502) although the 2DH descriptors have more detailed information to represent atomic environments than RDF and ADF descriptors. These results indicate that we should select more informative descriptors to improve the prediction models.

The PLS models are constructed based on a multivariate linear function, and therefore, coefficient values for each descriptor in the PLS models can be evaluated as the importance of each descriptor to the objective variable. Figure 4 shows coefficient values in three different PLS models. In the PLS model with the RDF descriptors, coefficient values for around 130th descriptors (corresponding with around 2.3 [Å]) were relatively low (see Fig. 4(a)), which agrees to the Si–Si bond length in a perfect diamond-type Si ( $\sim 2.35$  [Å]). Similar to this, coefficient values for around 130th descriptors (corresponding with around 2.3 [Å]) were also low in the PLS model with the RDF and ADF descriptors (see Fig. 4(b)). However, as can be seen in Figs. 4(a) and 4(b), there was a slight difference between coefficient values for the RDF descriptors (blue lines) in both cases because the ADF descriptors were also used for the latter case. In the PLS model with the 2DH descriptors, the higher and lower coefficient values (colored green and red, respectively) appear according to the atomic distance and atomic angle (see Fig. 4(c)).



**Fig. 3.** Diagnostic plot of total energy prediction for training data by PLS models with (a) RDF, (b) RDF + ADF, and (c) 2DH of atomic distance vs. atomic angle.



**Fig. 4.** Coefficient values for three different PLS models with (a) RDF (1.0–5.0 [Å]), (b) RDF (1.0–5.0 [Å], a blue line) + ADF (0–180 [°], a red line), and (c) 2DH of atomic distance vs. atomic angle.

However, it is difficult to reveal a cause of the relationship between the prediction performance for total energies and the 2DH descriptors at present.

#### 4. Conclusion

In this study, we propose a new method to construct a machine-learning interatomic potential based on the PLS linear regression model. Prediction accuracies of the PLS models predicting the total energies of various Si structures evaluated by DFT calculations are measured. We can construct the PLS-based interatomic potential with low computational cost in this method, and therefore, our proposed model has the potential to be used as a machine-learning interatomic potential for large-sized atomic-scale simulations. However, we should improve the prediction model by selecting more suitable descriptors.

#### Acknowledgment

The computation in this study was carried out using General Projects on the supercomputer “Flow” at the Information Technology Center, Nagoya University.

#### References

- [1] Y. Mishin, *Acta Mater.* **214**, 116980 (2021).
- [2] J. Behler and M. Parrinello, *Phys. Rev. Lett.* **98**, 146401 (2007).
- [3] J. Behler, *J. Chem. Phys.* **134**, 074106 (2011).
- [4] J. Behler, *Int. J. Quantum Chem.* **115**, 1032 (2015).
- [5] A. P. Bartók, M. C. Payne, R. Kondor, and G. Csányi, *Phys. Rev. Lett.* **104**, 136403 (2010).
- [6] A. P. Bartók, J. Kermode, N. Bernstein, and G. Csányi, *Phys. Rev. X* **8**, 041048 (2018).
- [7] S. Wold, M. Sjöstöm, and L. Eriksson, *Chemom. Intell. Lab. Syst.* **58**, 109 (2001).

## Development of ANN Potential for Si(100) Surface and Validation of Calculation Accuracy

Masayoshi Sato<sup>1\*</sup>, Tatsuya Yokoi<sup>2</sup>, Yusuke Noda<sup>3</sup>, Eiji Kamiyama<sup>3</sup>, Koji Sueoka<sup>3</sup>

<sup>1</sup>Graduate School of Computer Science and Systems Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

<sup>2</sup>Department of Materials Physics, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, Aichi 464-8603, Japan

<sup>3</sup>Department of Information and Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

E-mail: satopu0112@gmail.com

### Abstract

An artificial-neural-network (ANN) potential for Si(100) surfaces trained with data from density functional theory (DFT) calculations is developed. Performance validation of the ANN potential was performed to verify the predictive performance of energetic stabilities of the Si(100) surface models. No significant differences between models optimized by the ANN potential and the DFT calculation was found. Our ANN potential showed a good performance to predict total energies of the Si(100) surface models. We also demonstrated the geometrical optimization of a large-scale Si(100) surface model with more than 130,000 atoms, and discussed the accuracy of the ANN potential.

### Introduction

As large-scale integration (LSI) circuits continue to get smaller and more powerful, it is important to understand point defects and their clusters near the Si(100) surface, which is the manufacturing domain. First-principles calculations based on density functional theory (DFT) are widely used to solve such problems. However, the computational cost of DFT calculations is high, and we need crystal structure models containing a large number of atoms to perform DFT calculations of point-defect clusters with surface structures.

In recent years, atomistic simulations using artificial-neural-network (ANN) potentials [1], which are tuned to reproduce the results of DFT calculations as accurately as possible, have attracted much attention. In our previous study, an ANN potential for perfect crystal and grain boundary models of Si with high accuracy and short computation time was proposed [2]. ANN potentials are expected to be applied for simulating large-scale Si(100) surface models to evaluate their physical properties accurately.

In this study, we constructed an ANN potential for Si(100) surfaces to discuss energetic stability of point-defect clusters near Si(100) surfaces. Especially, we compared the DFT and ANN results for various structures of Si(100) surface with asymmetric Si dimers. We also demonstrated geometrical optimization of a large-scale Si(100) surface structure using our ANN potential.

### Methodology

In this study, training data including atomic coordinates, total energies and atomic forces for the ANN machine learning were generated using a CASTEP software based on DFT calculations with the Vanderbilt ultrasoft



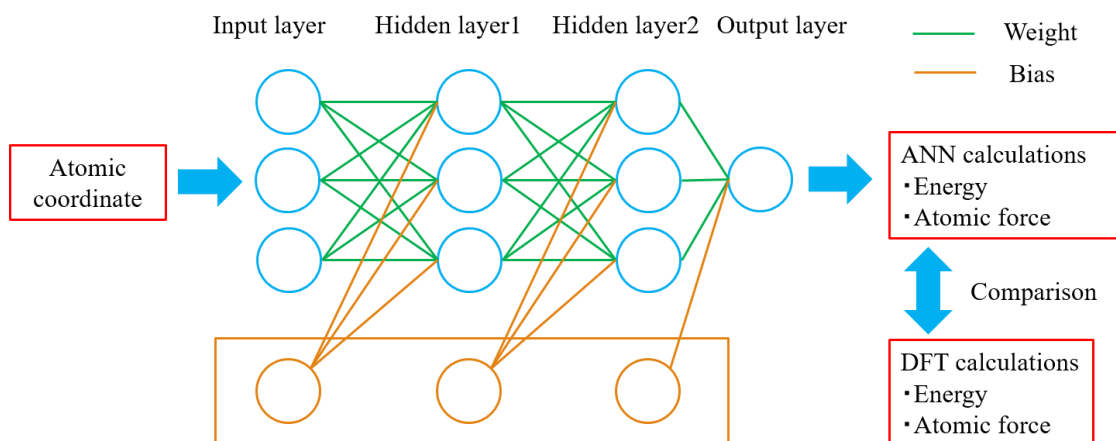
pseudopotential scheme. The cutoff energy of the plane wave was set to 500 eV. Self-consistent-field (SCF) tolerance was set to  $5.0 \times 10^{-7}$  eV/atom, and maximum SCF cycles was set to 500. A generalized gradient approximation (GGA)-based exchange-correlation functional proposed by Perdew, Burke, and Ernzerhof (PBE) was adopted. Different  $k$ -point sampling schemes were adopted according to the size of structure models (see Table 1).

**Table 1.** Different  $k$ -point sampling schemes for each model

Structure model	$k$ -point sampling grid
Bulk Si single crystal (8 atoms), Si(100) surface (8 atoms)	$8 \times 8 \times 8$
Bulk Si single crystal (16 atoms)	$4 \times 8 \times 8$
Bulk Si single crystal (64 atoms)	$4 \times 4 \times 4$
Si(100) surface (64 atoms)	$2 \times 4 \times 4$
Si(100) surface (128 atoms)	$2 \times 4 \times 2$

Bulk Si and Si(100) surface models were used to generate different structure models as training data. The number of atoms in the models ranged from 8 to 128 atoms. Geometrical optimization with 10–20 steps was performed for bulk Si models. Snapshots of DFT-based first-principles molecular dynamics simulations at the temperature range of 200–2,000 K were included in the training dataset. All snapshots of geometrical optimization for the Si(100) surface models were also included in the training dataset. All atomic positions and lattice parameters for each model were randomly displaced (in the range of 0.0–0.2 Å for atomic positions and in the range of  $\pm 20$  % for lattice parameters). Consequently, 5,706 total energies and 154,128 atomic forces were included in the training dataset.

Figure 1 shows the structure of an ANN potential used in this study. It consists of an input layer (32 nodes), two hidden layers (54 nodes for each layer), and an output layer (1 node). Atomic coordinate of each atom as input of the ANN potential, total energy and atomic force for each structure as outputs of the ANN potential were obtained from DFT calculations. Weights and biases as fitting parameters of the ANN potential were tuned so as to reduce total-energy and atomic-force errors between DFT and ANN results.

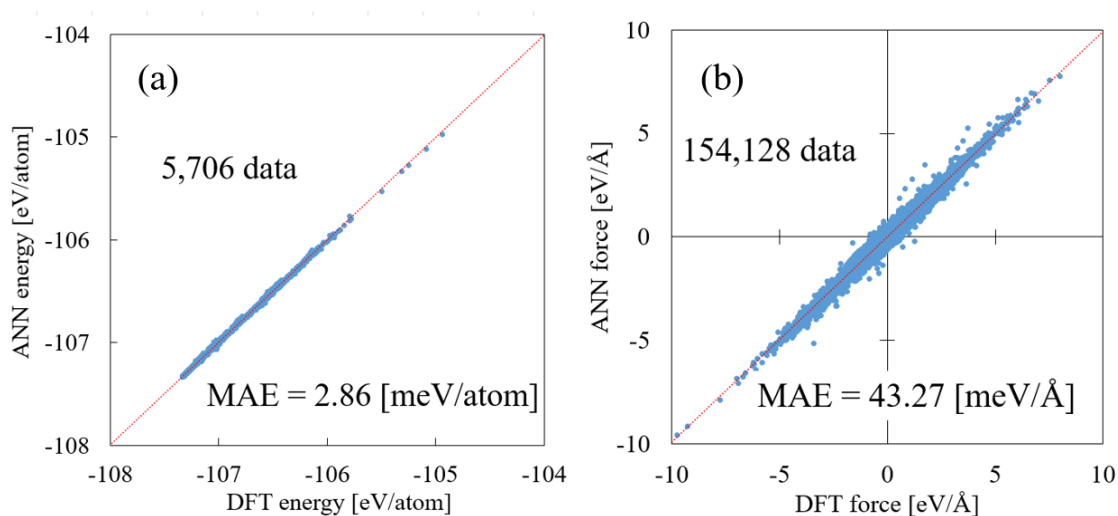


**Fig. 1.** Structure of the ANN potential.

We prepared  $p(2\times 1)$ ,  $p(2\times 2)$ , and  $c(4\times 2)$ -type Si(100) surface models with asymmetric Si dimers to validate the predictive accuracy of the constructed ANN potential. A Si(100) surface model including more than 130,000 atoms was also prepared for a test of large-scale atomistic simulation using the constructed ANN potential.

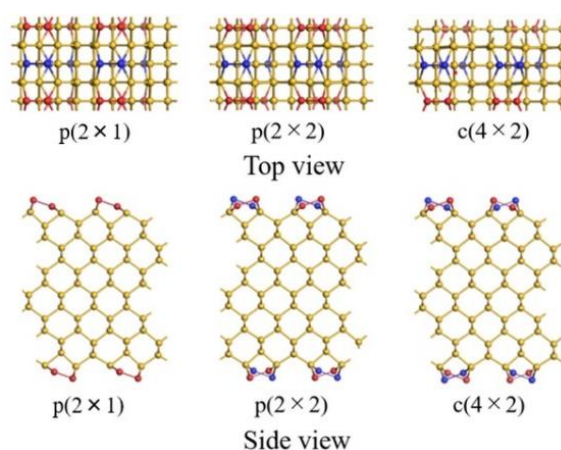
## Results and discussion

Figure 2 shows correlations between ANN-predicted and DFT-calculated values of total energies and atomic forces for the training data, as well as the mean absolute errors (MAEs). In both cases, all data points are distributed along the diagonal line, and there are almost no significant deviations. This indicates that our ANN potential predicts total energies and atomic forces of DFT calculations accurately. And, we confirmed that mean absolute errors (MAEs) for total energies (2.86 meV/atom) and atomic forces (43.27 meV/Å) were comparable to ANN potentials reported in previous studies [3,4].



**Fig. 2.** Correlations between the ANN and DFT results of (a) total energies and (b) atomic forces for the training data.

Figure 3 shows schematic views of Si(100) surfaces with the  $p(2\times 1)$ ,  $p(2\times 2)$ , and  $c(4\times 2)$  reconstructed structures optimized by the ANN potential. We confirmed that all the reconstructed surface models were kept stable with their dimer structures as well as those by DFT calculations. Table 2 shows total energies of their reconstructed surfaces per dimer evaluated by DFT calculation and ANN potential, and an energy difference between their total energies evaluated by DFT and ANN. In both DFT calculations and ANN potential, the orders of energetic stability of their three



**Fig. 3.** Si(100) reconstructed surfaces optimized by the ANN potential.

Si(100) surface models were the same, and the  $c(4 \times 2)$  surface model was the most stable. Prediction error of the total energies evaluated by the ANN potential was less than 5 meV/dimer, indicating a high calculation accuracy in terms of atomistic simulations.

We also performed the ANN simulation for a large-scale Si(100) surface model to verify accuracy and transferability of the ANN potential.

The large-scale model includes more than 130,000 Si atoms and  $c(4 \times 2)$  dimer structures. Schematic views of the large-scale Si(100) surface model are shown in Fig. 4. We confirmed that the large-scale surface model kept the  $c(4 \times 2)$  structure, indicating that the ANN potential can be used to simulate large-scale structure model including a large number of atoms.

## Conclusion

In this study, we developed an ANN potential to simulate various Si(100) surface models. We confirmed that all the reconstructed surface models optimized by the ANN potential were kept stable with their dimer structures as well as those optimized by DFT calculations. Energetic stabilities of the Si(100) surface models were

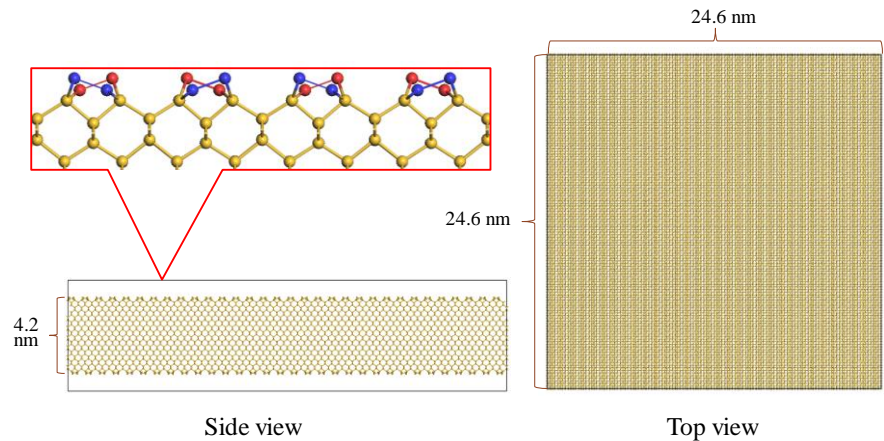
evaluated by both ANN potentials and first-principles DFT calculations and were compared with each other. The maximum difference between DFT and ANN energies is less than 5 meV/dimer, and therefore the ANN potential showed a good agreement with DFT calculations. We were able to perform the ANN potential simulation for the large-scale Si(100) surface model with the  $c(4 \times 2)$  dimer structure with almost the same precision as DFT calculations.

## References

- [1] J. Behler, *Int. J. Quantum Chem.* **115** (2015) 1032.
- [2] T. Yokoi, Y. Noda, A. Nakamura, and K. Matsunaga. *Phys. Rev. Mater.* **4** (2020) 014605.
- [3] T. Ushiro, T. Yokoi, Y. Noda, E. Kamiyama, M. Ohbitsu, H. Nagakura, K. Sueoka, and K. Matsunaga. *J. Phys. Chem. C* **125** (2021) 26869.
- [4] M. Ohbitsu, T. Yokoi, Y. Noda, E. Kamiyama, T. Ushiro, H. Nagakura, K. Sueoka, and K. Matsunaga. *Scripta Materialia* **214** (2022) 114650.

**Table 2.** Energy comparison of Si(100) reconstructed surface models.

	DFT [eV/dimer]	ANN [eV/dimer]	Energy difference [meV/dimer]
$p(2 \times 1)$	-1714.940	-1714.935	5
$p(2 \times 2)$	-1715.027	-1715.026	1
$c(4 \times 2)$	-1715.028	-1715.027	1



**Fig. 4.** The reconstructed Si(100) surface model with more than 130,000 atoms optimized by the ANN potential.

## Artificial Neural Network Potential Analysis on Self-Interstitial Atoms in Si

Kazuki Yamanaka<sup>1\*</sup>, Tatsuya Yokoi<sup>2</sup>, Eiji Kamiyama<sup>3</sup>, Yusuke Noda<sup>3</sup>, Koji Sueoka<sup>3</sup>

<sup>1</sup>Graduate School of Computer Science and Systems Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

<sup>2</sup>Department of Materials Physics, Nagoya University, Furo-cho, Chikusa-ku, Nagoya, Aichi 464-8630, Japan

<sup>3</sup>Department of Information and Communication Engineering, Okayama Prefectural University, 111 Kuboki, Soja, Okayama 719-1197, Japan

e-mail: OPU.Yamanaka@gmail.com

### Abstract

In this study, we focused on self-interstitial (*I*) point defects in Si single crystals and analyzed the distance between two *I* defects using an artificial-neural-network (ANN) interatomic potential. Ten different configurations of the two *I* defects were considered in our simulations. Geometrical optimization and molecular dynamics (MD) simulations based on the ANN potential were performed to evaluate binding energies and distance between the two *I* defects for each configuration. From our simulations, we found that the formation of an *I*<sub>2</sub> cluster and the binding energy do not depend on the distance between the two *I* defects at the initial state of the simulations.

### Introduction

The semiconductor Si crystals that form the basis for miniaturization and performance enhancement of LSIs require very high integrity at the atomic level. Point defects and clusters in Si crystals aggregate to form secondary defects. The secondary defects affect device performance and lead to increasing dopant diffusion, electrical inactivation, and leakage current. Then, many studies on point defects and clusters have been done to overcome these problems.

First-principles calculation based on density functional theory (DFT) is one of widely used theoretical methods to reveal atomic-level phenomena in target materials. DFT calculation can demonstrate atomistic simulation accurately according to the basic principles of quantum mechanics. However, it requires huge computational cost, and thus the size of crystal structure models which can be handled in DFT calculations is limited [1,2]. Whereas, the utility of artificial-neural-network (ANN) potential has recently been reported, and the ANN potential is often constructed so as to predict physical properties with comparable accuracy to and much lower cost than DFT calculations [3-5].

In this study, we perform atomistic simulations based on the ANN potential to reveal the dynamics of self-interstitial atoms (*I*) in Si single crystals. And, we discuss the dynamics of *I* defects based on results of binding energy and distance between two *I* defects.

### Calculation details

We used an ANN potential constructed by Ohbitsu *et al.* [6] for atomistic simulations of Si structures with *I* defects in this study. Geometrical optimization based on DFT calculations for various Si structure models were performed to generate the training data of machine learning for constructing the ANN potential, and the results of geometrical optimization at each step (atomic coordinates, total energies, and atomic forces) were used as the

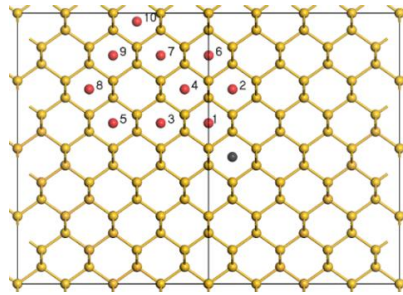
training data. A generalized gradient approximation (GGA)-based exchange-correlation functional proposed by Perdew, Burke, and Ernzerhof (PBE), and an ultrasoft pseudopotential were adopted in the DFT calculations. The plane wave cutoff energy was set to 500 eV, and a  $8 \times 8 \times 8$   $k$ -point sampling scheme was used. The structure of the ANN potential consists of an input layer with 32 nodes (as same as the number of symmetry functions), two hidden layers with 52 nodes for each layer, and an output layer with 1 node. This ANN potential was implemented based on previous research [7]. The predictive performance of the ANN potential was reported in our previous study [6]. The mean absolute errors (MAEs) of total energies and atomic forces for the training data were 4.04 [meV/atom] and 79.41 [meV/Å], respectively. The mean absolute errors (MAEs) of total energies and atomic forces for the validation data were 8.74 [meV/atom] and 77.40 [meV/Å], respectively. These results indicate that the ANN potential has good accuracy to predict total energies and atomic forces in various Si structures obtained from DFT calculations.

We performed ANN-potential-based molecular dynamics (MD) simulations of Si single crystal with two  $I$  defects. The Si single crystal model consisting of 512 Si atoms (also known as a  $4 \times 4 \times 4$  supercell model) was employed. In the MD simulations, ten configurations of two  $I$  defects in each hexagonal (H)-site were considered (see Figure 1), and annealing temperature was set to from 1,500 to 500 [K] during 10 [ps]. Four runs of MD simulations for each configuration of two  $I$  defects were performed, and summary statistics (average, maximum, and minimum) of the distance between two  $I$  defects were measured.

We also performed ANN-potential-based geometrical optimization for the 512-atom Si single crystal model with two  $I$  defects. After the geometrical optimization, binding energy  $E_b$  can be calculated using the following equation,

$$E_b = 2E_{\text{tot}}[\text{Si}_{512}I] - \{E_{\text{tot}}[\text{Si}_{512}I_2] + E_{\text{tot}}[\text{Si}_{512}]\} \quad (1)$$

where  $E_{\text{tot}}[\text{Si}_{512}]$ ,  $E_{\text{tot}}[\text{Si}_{512}I]$ , and  $E_{\text{tot}}[\text{Si}_{512}I_2]$  are the total energies of 512-atom Si single crystal with no defect, single  $I$  defect, and two  $I$  defects, respectively.

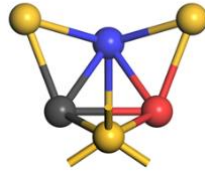


**Fig. 1.** Arrangement of self-interstitial ( $I$ ) atoms in Si single crystal.

## Results and discussion

Table 1 shows summarized results of MD simulations for ten different configurations. It can be seen that the minimum distance between two  $I$  defects after the MD simulation is 2.40 Å. The structure of two  $I$  defects in this case is shown in Figure 2. The Si atom colored black shows introduced to the central atoms and colored red shows numbered atoms in Fig. 1. The blue Si atom shows pushed by red atom and black atom. This structure has been well known as the most stable structure of  $I_2$  cluster. where the two  $I$  defects form a dumbbell structure[6]. The maximum and minimum distances between two  $I$  defects in cases of configuration 1, 3, and 6 are 2.40 Å. In other words, two

$I$  defects form the dumbbell-like  $I_2$  cluster at all the four runs in those cases. Our results show that two  $I$  defects finally form the  $I_2$  cluster at least once in most cases. However, two  $I$  defects have never formed the  $I_2$  cluster in cases of configuration 5 and 9 because the minimum distance is longer than 2.40 Å.



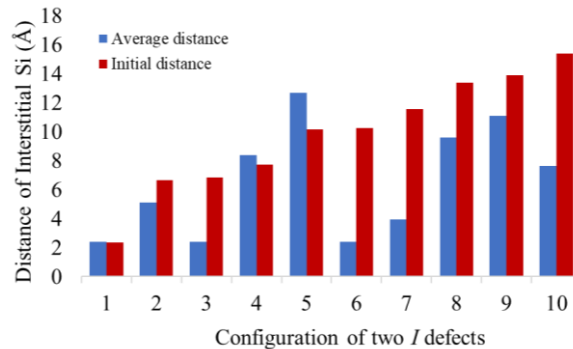
**Fig. 2.** The structure of an  $I_2$  cluster.

Figure 3 shows average distances between two  $I$  defects in four runs of MD simulations for each configuration. For example, two  $I$  defects finally form the dumbbell-like  $I_2$  cluster in case of configuration 6 (because the average distance is 2.40 Å) but have never formed the  $I_2$  cluster in case of configuration 5 (because the average distance is 12.66 Å), although initial distances between the two  $I$  defects in both cases are very close to each other. It indicates that the  $I_2$  cluster formation does not depend on the initial distance between two  $I$  defects.

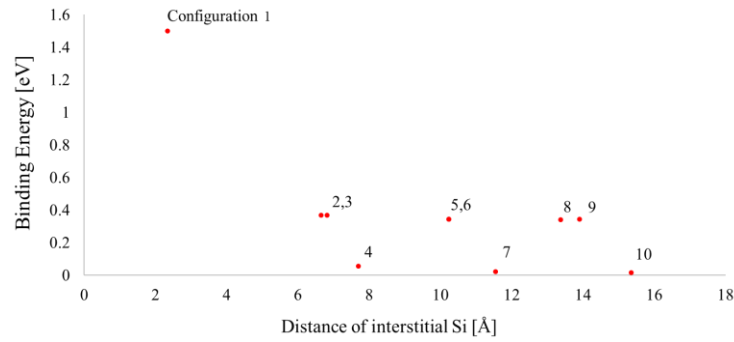
Figure 4 shows the relationship between binding energy and distance between two  $I$  defects for the ten configurations. The highest binding energy is 1.49 [eV] for the configuration 1, in which the structure is similar to the dumbbell-like  $I_2$  cluster (see Figure 5). Binding energies for configurations 4, 7, and 10 are almost zero, and those for the other configurations are about 0.40 [eV]. We found that the binding energy does not strongly depend on the initial distance between two  $I$  defects.

**Table 1.** Initial and final distances between two  $I$  defects in ANN-MD simulations.

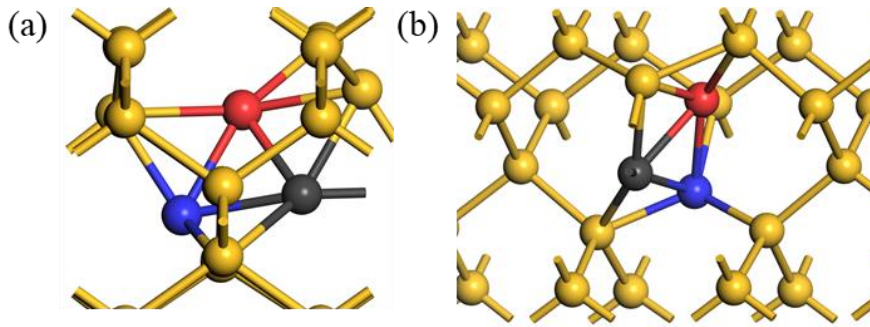
Structure	Initial distance (Å)	Final distance	
		Maximum distance (Å)	Minimum distance (Å)
1	2.34	2.40	2.40
2	6.65	8.18	2.40
3	6.82	2.40	2.40
4	7.70	15.58	2.40
5	10.16	13.46	8.43
6	10.24	2.40	2.40
7	11.54	8.64	2.40
8	13.37	16.29	2.40
9	13.9	15.55	6.61
10	15.36	14.52	2.40



**Fig. 3.** Average and initial distances between two  $I$  defects for each configuration in ANN-MD simulations.



**Fig. 4.** Binding energy and distance between two  $I$  defects for each configuration.



**Fig. 5.** (a) Top view and (b) side view of  $I_2$  defect after MD simulation in case of configuration 1.

## Conclusion

In this study, we demonstrate MD simulations of Si single crystal with two  $I$  defects using the ANN potential. We calculated summary statistics of the distance between two  $I$  defects at the final step of the MD simulations. These results show that the  $I_2$  cluster formation does not depend on distance between two  $I$  defects at the initial step of the MD simulations. It was also found that the binding energy of two  $I$  defects does not strongly depend on the initial distance between the two  $I$  defects. We should investigate what significant is for the binding energy of two  $I$  defects in Si single crystals accordingly.

## REFERENCES

- [1] A. F. Wright, *Phys. Rev. B* **74**, 165116 (2006).
- [2] K. Sueoka, E. Kamiyama, and J. Vanhellemont, *J. Appl. Phys.* **114**, 153510 (2013).
- [3] J. Behler, *Int. J. Quantum Chem.* **115**, 1032 (2015).
- [4] T. Yokoi, Y. Noda, A. Nakamura, and K. Matsunaga, *Phys. Rev. Mater.* **4**, 014605 (2020).
- [5] T. Ushiro, T. Yokoi, Y. Noda, E. Kamiyama, M. Ohbitsu, H. Nagakura, K. Sueoka, and K. Matsunaga, *J. Phys. Chem. C* **125**, 26869 (2021).
- [6] M. Ohbitsu, T. Yokoi, Y. Noda, E. Kamiyama, T. Ushiro, H. Nagakura, K. Sueoka, and K. Matsunaga, *Scr. Mater.* **214**, 114650 (2022).
- [7] J. Behler and M. Parrinello, *Phys. Rev. Lett.* **98**, 146401 (2007).

## Extension of Zeller's Silicon Power Device SEB Failure Rate Calculation method to Aviation Altitude

Srikanth Gollapudi<sup>1\*</sup>, Ichiro Omura<sup>1</sup>

<sup>1</sup>*Kyushu Institute of Technology, 2-4 Hibikino, Wakamatsu-ku, Kitakyushu, 808-0196, Japan*

e-mail: gollapudi.srikanth432@mail.kyutech.jp

### Abstract

Power semiconductor devices are susceptible to catastrophic failures when exposed to energetic particles present in cosmic radiation. The most serious failure mechanism is single event burnout (SEB). The calculation of SEB failure rate of power devices plays critical role in power device selection to make the system robust against cosmic radiation. The phenomenological SEB failure rate calculation approach proposed by Zeller is applicable only to terrestrial radiation environment. In this work, altitude dependent parameters are introduced in the Zeller formula to expand the application to higher altitudes by utilizing proposed TCAD based failure rate calculation method results.

### Introduction

Power semiconductor devices evolved as key components of power electronic systems in many applications ranging from consumer, industrial, medical and transportation sectors etc. and, estimated that they control around 50% of total electricity used in the world. During early nineties, a new catastrophic failure mechanism observed in high voltage power devices during blocking condition of the power device. Investigation on this indicated that terrestrial cosmic radiation particles are the cause of this failure.

When the high energetic particle of cosmic radiation interacts with the device, it generates electron-hole pairs along the path. During the conduction state of the device, these extra charge carriers do not affect the device. However, in the blocking state, the plasma of charge carriers shields its interior from electric field. The voltage drop occurs at pronounced electric field spikes at the edges of plasma. When these electric field spikes exceed the critical electric field of the device material, leads to further generation of carriers due to impact ionization as

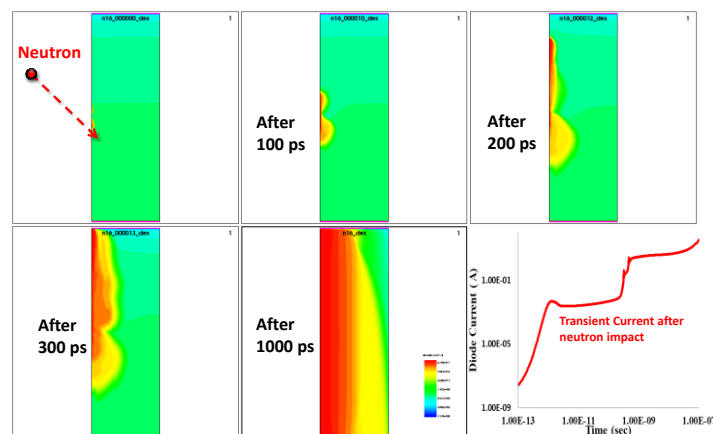


Fig 1. Electron density inside the PiN diode and transient current after the impact of neutron

shown in Fig 1. This phenomenon results in a destructive mechanism in power devices called Single Event Burnout (SEB).



The information of SEB failure rate of power devices plays critical role in power device selection to make the cosmic ray robust systems. The phenomenological failure rate calculation approach proposed by Zeller [1,2] in terms of device parameters shown in equation (1) is very easy and offers many advantages compare to real life tests and accelerated tests. However, this is an empirical formula from the accelerating testing result and thus only be applicable to evaluate the failure rate at sea level.

$$\frac{FIT}{\rho} = a_1 \cdot A \cdot S^2 \cdot e^{\frac{-b_1}{S}} = 1.45 \times 10^9 \cdot A \cdot S^2 e^{\frac{-83.41}{S}} \quad \text{----- (1)}$$

Where,  $S = \sqrt{\frac{V}{\rho}}$  for non-punch through,  $S = 0.2786 \cdot \frac{V}{t} + 0.8972 \cdot \frac{t}{\rho}$  for punch-through device.

$A$  is device area;  $\rho$  is resistivity of n-base;  $t$  is thickness of n-bae in  $\mu\text{m}$ ;  $FIT$  is failures in trillion device hours of operation.

However, the recent increase in electric power demand in aircraft necessitates the use of high-power semiconductor devices in avionics. This requires the expansion in SEB failure study of power semiconductor devices even to avionic applications. We proposed a TCAD based SEB failure rate calculation method [3,4] with destruction charge as failure criteria. The unique feature of decoupling between failure cross section and the neutron flux spectrum expands the application of proposed method to any operating environment, eg. Terrestrial, aviation, space environments. By evaluating the failure rate using the proposed TCAD based method up to the airplane altitude, we obtained the altitude dependent parameters  $a_1(H)$  and  $b_1(H)$ . By incorporating these parameters in the original Zeller method, the applicability of Zeller failure calculation method is extended to higher altitude applications.

### TCAD based SEB failure rate calculation method

Our group proposed a TCAD based failure rate calculation method with threshold charge as failure criteria of the device. The flowchart representing the calculation is shown in Fig 2. The unique feature of the proposed method is the decoupling between failure cross section and the cosmic ray flux spectrum. Due to this, once the failure cross section which is unique for a particular device is known, it is possible to obtain the failure rate of the device operating at any radiation condition like terrestrial, aviation or the satellite altitude.

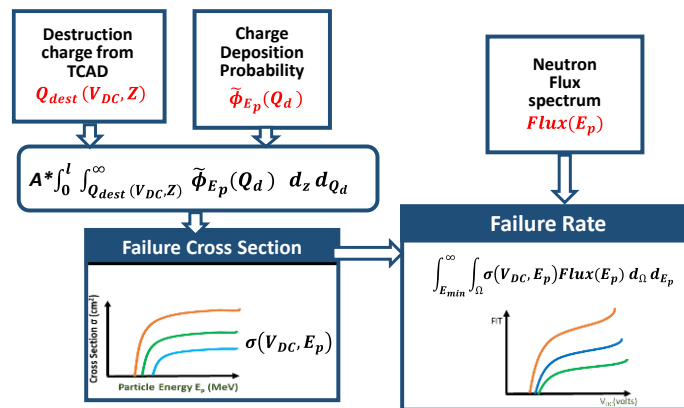


Fig 2. Block diagram representation of proposed TCAD based failure rate calculation method

The representation of various symbols in the proposed method is as follows.

- $\sigma$  = Failure cross section in  $\text{cm}^2$
- $V_{DC}$  = Applied voltage in Volts
- $E_p$  = Energy of particle in MeV
- $A$  = Device area in  $\text{cm}^2$
- $l$  = i-layer thickness in  $\mu\text{m}$
- $Q_{\text{dest}}$  = Critical amount of deposited charge in C
- $\tilde{\phi}_{E_{\text{si}}}$  = Deposited charge probability in silicon in  $\text{C}^{-1}\text{cm}^{-1}$
- $z$  = Position along depth direction in  $\mu\text{m}$

The failure rate obtained using the proposed TCAD based method is shown in Fig 3 at terrestrial altitude. This shows excellent agreement with the failure rate of Zeller method and the Alex Hales et al[5] in our previous work, we have reported the failure rate of 100  $\mu\text{m}$  and of 300  $\mu\text{m}$  PiN diode due to the impact of neutrons up to aviation altitudes [3] and protons at satellite altitude [4].

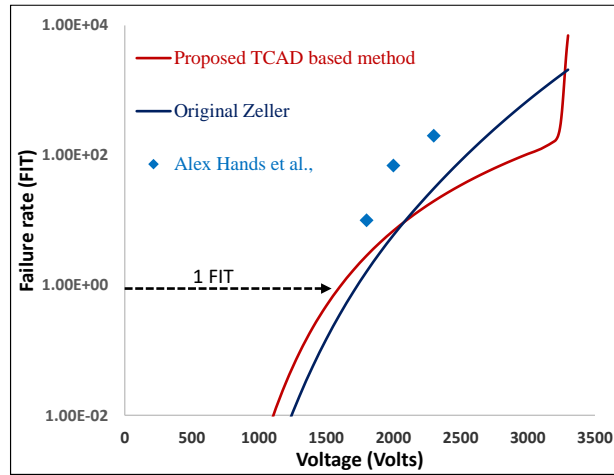


Fig 3. comparison of failure rate obtained at terrestrial altitude

### Modified Zeller method for high altitude applications

To enhance the application of Zeller method, we must include altitude dependent parameter in the formula. For this, we obtained the failure rate of the power device up to an altitude of 15 km from the sea level. From the failure rate at various altitudes, altitude dependent parameters are obtained, and the fitting curves are shown in Fig 4 and Fig 5 for  $a_1(H)$  and  $b_1(H)$ . With the inclusion of these parameters in the Zeller method, the applicability of the method can be extended to aviation altitudes. the modified Zeller formulation is shown in equation (2).

$$\frac{FIT}{\rho} = a_1(H). A. S^2. e^{\frac{-b_1(H)}{S}} \quad (2)$$

$$= (1.546 + 5 \times 10^{-5}H) \times 10^9. A. S^2 e^{\frac{-(79.73-4 \times 10^{-4}H)}{S}}$$

Where, H is altitude in feet. All other parameters are same as in original Zeller formula.

Using this method, the failure rate of 300  $\mu\text{m}$  PiN diode and 100  $\mu\text{m}$  PiN diode evaluated at 12 km altitude is

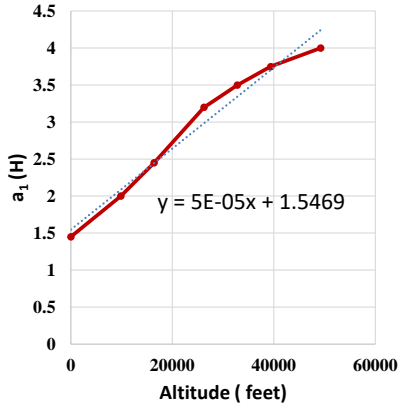


Fig 4. Fitting curve for parameter  $a_1$  (H)

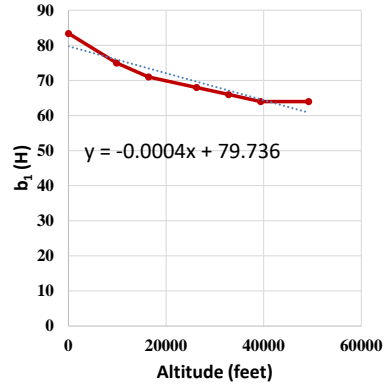


Fig 5. Fitting curve for parameter  $b_1$  (H)

shown in Fig 6 and Fig 7 respectively. the failure rate is compared with the TCAD based method and the Alex Hands et al. Since the power devices are chosen with a maximum allowable failure rate of 1 FIT, we have shown the compared the failure rate at 1 FIT and it shows good agreement with the other results. Since the failure rate is in terms of device parameters and altitude, it is very easy to obtain the failure rate using the modified Zeller method up to an altitude of commercial airline flying altitudes.

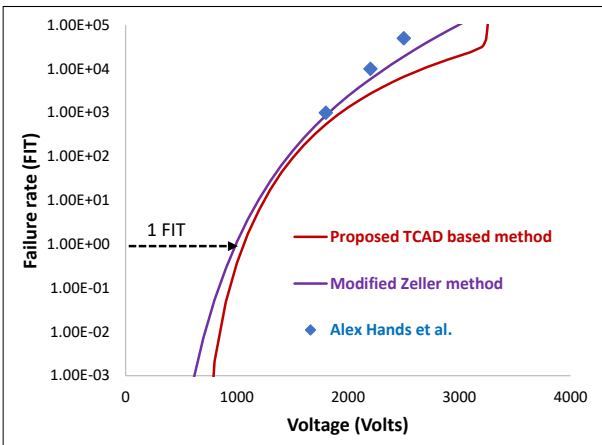


Fig 6. Failure rate comparison of 300  $\mu\text{m}$  PiN diode at 12 km altitude

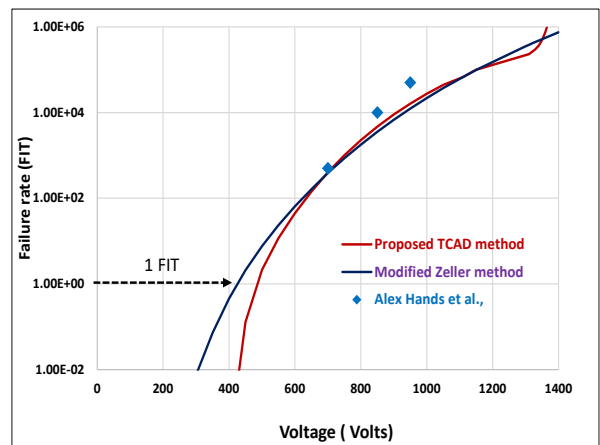


Fig 7. Failure rate comparison of 100  $\mu\text{m}$  PiN diode at 12 km altitude

## Conclusion

The original phenomenological failure rate calculation method proposed by Zeller has application limitation of terrestrial altitude. Using the proposed TCAD based failure rate approach, we included the altitude dependent parameters in the Zeller formula. Thus, the modified Zeller method can be used to evaluate the failure rate of high power semiconductor devices up to commercial aircraft flying altitudes.

## REFERENCES

- [1]. HR Zeller., Microelectron. Reliab. Vol.37,pp.1711-1718,1997.
- [2]. HR Zeller., Solid-State Electronics, Vol. 38, pp. 2041-2046, 1995.
- [3]. S Gollapudi et al., Jpn. J. Appl. Phys., Vol.60, pp. SBBD19, 2021.
- [4]. M Sudo et al., Microelectronics Reliability, Vol. 100-101, pp. 113396, 2019.
- [5]. Alex Hands et al., IEEE Trans. on Nuclear. Sci, Vol. 58, No.6, Dec 2011.

## Evaluation of $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystalline quality grown by crucible-free technique

Isao Takahashi<sup>1,2\*</sup>, Vladimir Kochurikhin<sup>1</sup>, Taketoshi Tomida<sup>1</sup>, Takamasa Sugawara<sup>2</sup>, Yongzhao Yao<sup>3</sup>, Koji Sato<sup>3</sup>, Yukari Ishikawa<sup>3</sup>, Kei Kamada<sup>1,2</sup>, Koichi Kakimoto<sup>2</sup> and Akira Yoshikawa<sup>1,2</sup>

<sup>1</sup>C&A Co., 1-16-23, Ichibancho, Aoba-ku, Sendai, 980-0811, Japan

<sup>2</sup>Tohoku University, 2-1-1, Katahira, Aoba-ku, Sendai, 980-8577, Japan

<sup>3</sup>Japan Fine Ceramics Center, 2-4-1, Mutsuno, Atsuta-ku, Nagoya, 456-8587, Japan

e-mail: takahashi\_isao@c-and-a.jp

### Abstract

We originally developed a new melt growth technique to obtain high quality  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> single crystals without a crucible based on skull melting techniques. As a result,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystals are successfully grown by the new growth technique, however several domain boundaries are observed by X-ray topography measurement. These boundaries seem to occur from a seed crystal. Impurity measurement reveals that most substances detected less than 1 ppm, therefore contamination is considered very low level in the grown samples.

### Introduction

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is an emerging material as a wide band-gap semiconductor for high-power and low-loss power devices because it can be produced as large size single crystals by melt-growth techniques. In practice, remarkable progresses on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal growth and device process technologies [1]. Previous researches success to obtain very good quality  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystals grown by Czochralski (Cz) [2], edge-defined film-fed growth (EFG) [3,4] and vertical Bridgman[5]. However, these techniques are required to use a precious metal crucible such as Ir or Pt-Rh which causes higher production cost and limitation of oxygen concentration in growth atmosphere. In particular oxygen concentration during growth is quite important condition for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystals to reduce point defects because decomposition reaction ( $\text{Ga}_2\text{O}_3 \rightarrow 2\text{Ga} + 3/2\text{O}_2$ ) is very active at high temperatures. Therefore, crucible free growth is a key technology to produce low cost and high quality  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> wafers. Skull melting method is one of the crucible free melt-growth techniques and famous for manufacturing of cubic zirconia crystals. However, the conventional technique can apply to only low resistivity materials due to the insufficient frequency of industrial power generators.

### Proposed a new growth method:

We originally developed skull melting to apply to low conductivity oxide materials and named Oxide Crystal growth from Cold Crucible (OCCC) method as shown in Fig. 1 [7]. In this method, Ga<sub>2</sub>O<sub>3</sub> feedstock is charged in a water flowed copper basket. The feedstock is directly heated by high frequency magnetic field and melts from the center part to outer area. In adjacent area to the basket, the melt is quenched and immediately freeze to solid state resulting in substitution of a crucible. Finally, a seed is touched on top followed by ingot growth like at conventional Cz method.

Important progress of the OCCC method are the magnetic field frequency of induction heating and control method of the frequency to follow the change in inductance which is affected by resistivity and volume of Ga<sub>2</sub>O<sub>3</sub>

melt. Following equation shows a relationship between the frequency  $F$  (Hz), resistivity  $\rho$  ( $\Omega\cdot\text{m}$ ) and diameter of volume to be heated  $D$  (m).

$$F \geq 3 \times 10^6 \rho / D^2$$

Conventional growth techniques use low resistivity crucibles such as copper, carbon, platinum or iridium which ranges from  $10^{-8}$  to  $10^{-6}$   $\Omega\cdot\text{m}$ . These materials require less than 1 kHz for induction heating as can be calculated by the equation. On the other hand, resistivity of oxide materials ranges from  $10^{-4}$  to  $10^{-2}$   $\Omega\cdot\text{m}$ . More than 100 kHz frequency is required to heat  $\text{Ga}_2\text{O}_3$  feedstock and melt. At first, we originally developed high frequency magnetic field generator and success to get  $\text{Ga}_2\text{O}_3$  melt. The second obstruction to grow  $\beta\text{-Ga}_2\text{O}_3$  crystals by skull melting is how to control frequency to keep stable temperature distribution of the melt. Because resonance frequency and inductance depend on  $\text{Ga}_2\text{O}_3$  state and volume which are changes as process time goes by. For example, resistivity dropped down by less than 1/10 when  $\text{Ga}_2\text{O}_3$  solid get melt. Absorption efficiency of magnetic field in  $\text{Ga}_2\text{O}_3$  also changes dramatically in melting process depending on the changes in resonance frequency and resistivity. Furthermore, melt volume is changed during crystal growth process which is required precise control of the frequency to keep stable temperature. We also developed crystal growth software to follow the changes in resonance frequency and get feedback to the frequency of applied voltage in the coil.

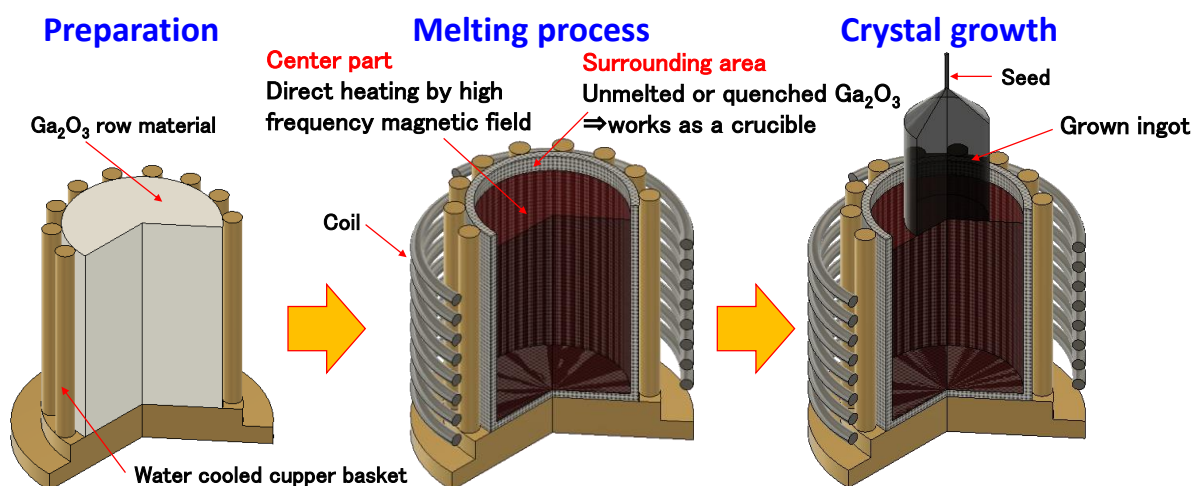


Fig. 1. Schematic diagram of the OCCC method

## Experimental

$\beta\text{-Ga}_2\text{O}_3$  crystals were grown by the OCCC method from 85mm diameter copper basket where un-doped  $\text{Ga}_2\text{O}_3$  feedstock with 1.2 kg was charged. After the feedstock was partially melted, a seed crystal was touched on the melt, and pulled up by 5mm/h in air. X-ray topography measurement was performed to observe crystalline quality and misorientation in the grown sample. X-ray diffraction was detected by charge-coupled device (CCD) camera during the  $\omega$  angle was changed in  $0.5^\circ$ . Impurities were measured by glow discharge mass spectrometry (GD-MS).

## Results and discussions

Fig. 2(a) shows a picture of a crystal grown along  $\langle 010 \rangle$  direction by OCCC method. Around 20 mm  $\beta\text{-Ga}_2\text{O}_3$  crystal was obtained in light blue color. Fig. 2(b) and (c) shows cross sectional picture and X-ray topography of

the same sample. It looks like single crystal in Fig.2(b), but there are several domain boundaries as shown in Fig.2 (c). These boundaries would be attributed in the seed crystal because they occur at initial stage of the growth and each domain epitaxially grow in growth direction. Hence complete single crystal is possible grown by the OCCC method when we use good quality seed crystal.



Fig. 2. (a) picture of grown crystal, (b) cross sectional picture and (c) X-ray topography of the same sample.

Table 1 shows GD-MS measurements results of the feedstock and the grown sample. Concentration of most impurities is less than 1 ppm or detection limit in the grown crystal. It notes that Ir and Cu are less than detection limit of GDMS. Ir is main impurity in the case of Cz and EFG method due to the use of crucible. In the OCCC method Cu is used for basket which keeps the  $Ga_2O_3$  feedstock and melt so diffusion might be occur from the basket to  $Ga_2O_3$  solid. It turns out that the Cu contamination is small enough to be ignored in the practical crystal. High concentration of Si remains in the grown crystal. It seems that Si is originated from the feedstock because main impurity in the feedstock is also Si.

Table I. Impurity analysis of the grown crystal and feedstock measured by GD-MS

Impurity substances	Concentration (ppm)	
	Grown crystal	Feedstock
Na	0.13	-
Mg	0.04	<1
Si	11	5
Ca	0.16	<1
Fe	0.89	<1
Cu	< 0.05	<1
Zn	< 0.1	<1
Ge	< 0.1	<5
Ti	0.007	-
Mn	< 0.05	-
Co	< 0.01	-
Zr	< 0.05	-
Pt	< 0.05	-
Ir	< 0.01	-

## Conclusions

We developed skull melting techniques for oxide material which has high resistivity and named the OCCC method. Special equipment to generate more than 100 kHz frequency magnetic field is installed to get melt  $Ga_2O_3$  feedstock. As a result,  $\beta$ - $Ga_2O_3$  crystal is obtained with a size of 20 mm. X-ray topography revealed several domain boundaries in the grown crystal which are attributed to the seed crystal. Impurity measurement shows low contamination of Ir, Cu and the other metal substances owing to the crucible free growth method. It concludes that the OCCC method is a promising growth technique to fabricate  $\beta$ - $Ga_2O_3$  crystals in high quality and low production cost.

## REFERENCES

- [1] M. Higashiwaki, AAPS Bulletin (2022) 32:3
- [2] Z. Galazka, S. Ganschow, K. Irmischer, D. Klimm, M. Albrecht, R. Schewski, M. Pietsch, T. Schulz, A.

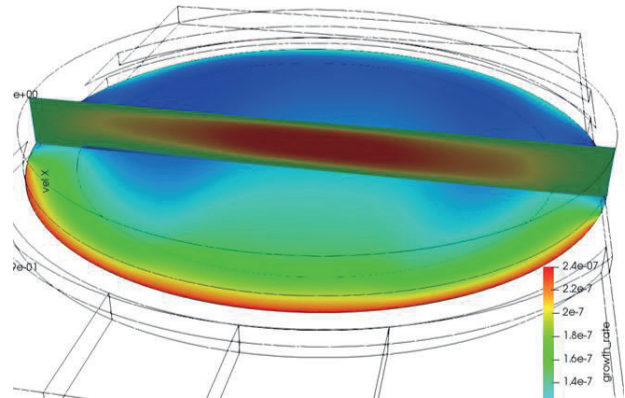
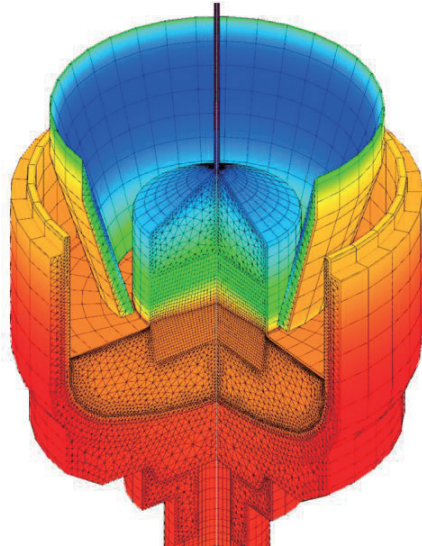
- Dittmar, A. Kwasniewski, R. Grueneberg, S. B. Anooz, A. Popp, U. Juda, I. M. Hanke, T. Schroeder, M. Bickermann, *Progress in Crystal Growth and Characterization of Materials* **67** (2021) 100511
- [3] A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui, and S. Yamakoshi, *Japanese Journal of Applied Physics* **55**, 1202A2 (2016)
- [4] H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, *Japanese Journal of Applied Physics*, Vol. **47**, No. 11, 2008, pp. 8506–8509
- [5] K. Hoshikawa, T. Kobayashi, E. Ohba, T. Kobayashi, *Journal of Crystal Growth* **546** (2020) 125778
- [6] E. Ohba, T. Kobayashi, T. Taishi, K. Hoshikawa, *Journal of Crystal Growth* **556** (2021) 125990
- [7] A. Yoshikawa, V.V. Kochurikhin, M. Yoshino, R. Murakami, T. Tomida, I. Takahashi, K. Kamada, Y. Shoji, H. Sato, R. Kucerkova, A. Beitlerova, M. Nikl, *Cryst. Growth&Des.* Submitted



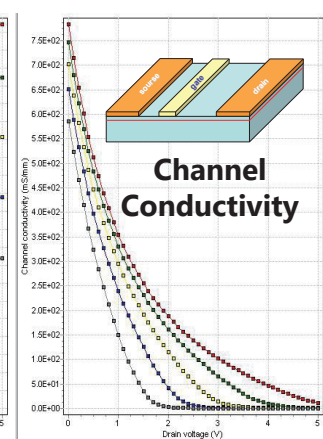
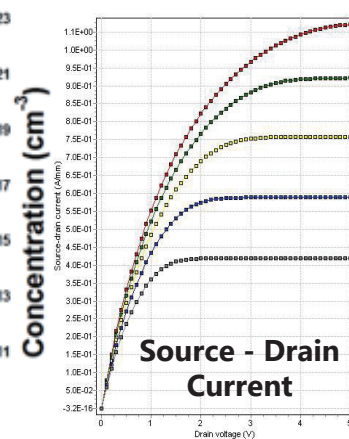
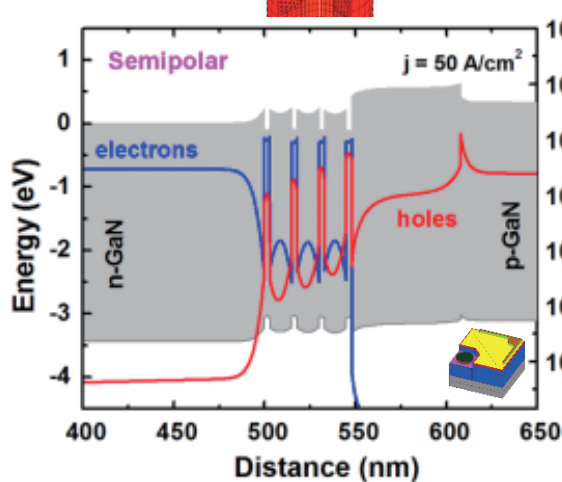




# Modeling Solutions for Crystal Growth and Devices



Growth rate uniformity on the wafer



## Crystal Growth Simulation

Crystal Growth from the Melt, Solution and Vapor phase

## Device Simulation

LED, Laser Diode, PV cell, HEMT

## STR Japan K.K.

East Tower 15F, Yokohama Business Park

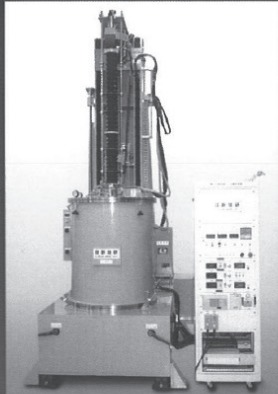
134, Goudo-cho, Hodogaya-ku, Yokohama, Kanagawa, 240-0005, Japan

Site: [www.str-soft.co.jp](http://www.str-soft.co.jp)

Global site: [www.str-soft.com](http://www.str-soft.com)

# CZ type Pullers Equipment for Oxide crystal growing

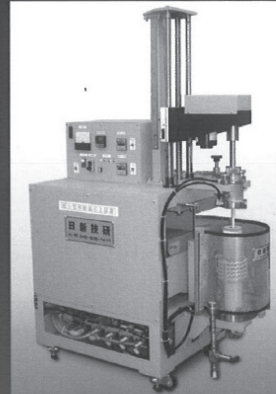
Chamber type



## Specifications

Heating temperature	2100°C (Normal)
Heating system	RF-generator
crucible	Pt, Ir, Mo, etc. φ150
Gas	Ar, N <sub>2</sub> , O <sub>2</sub>
Pulling rate	0.1~10.0mm/h
Main supply	3φ AC200V 50/60Hz 60kVA

Quartz tube type



## Specifications

Heating temperature	2100°C (Normal)
Heating system	RF-generator
crucible	Pt, Ir, Mo, etc. φ30
Gas	Ar, N <sub>2</sub> , O <sub>2</sub>
Pulling rate	1~10.0mm/h
Main supply	3φ AC200V 50/60Hz 6kVA

# SiC/AlN-Growth Equipment

Seeded Sublimation growth of SiC bulk single crystals

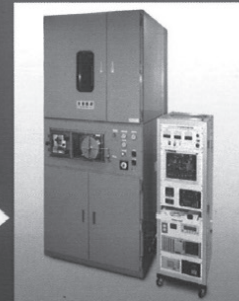


## Specifications

Heating temperature	2400°C (Normal) 2500°C (Max)
Temperature control accuracy	2400°C ± 5°C
Ultimate pressure	1.3 × 10 <sup>-3</sup> Pa (10 <sup>-6</sup> Torr)
Pressure control range	0.13 × 10 <sup>-3</sup> ~ 93.1 × 10 <sup>-3</sup> Pa (1 ~ 700 Torr)
Main supply	3φ AC200V 50/60Hz 70kVA

# SiC-CVD Equipment

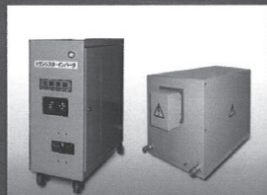
SiC-CVD by Vertical Hot-Wall reactor



## Specifications

Reactor	Vertical Hot-Wall reactor
Capacity	Two 2-inch wafers
Heating temperature	1600°C (Normal) 1700°C (Max)
Ultimate pressure	1.3 × 10 <sup>-4</sup> Pa (10 <sup>-7</sup> Torr)
Main supply	3φ AC200V 50/60Hz 65kVA

System-control by PLC via the GUI input the computer



RF-generator Matching-Box

RF-generator and Matching-Box is very small and its installation is flexible

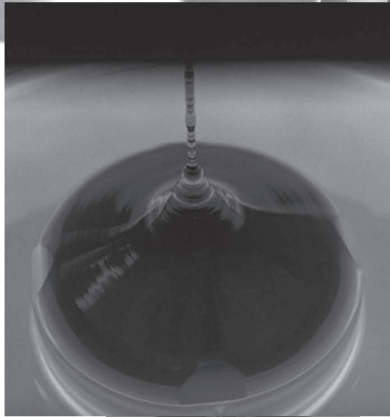
Challenge to the Future



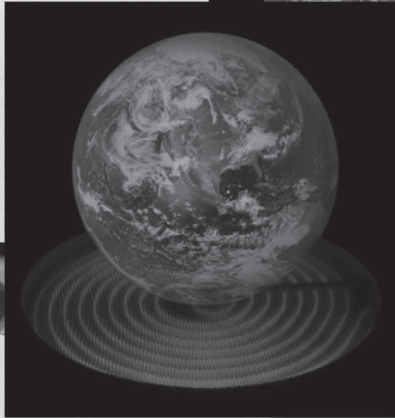
**Nissin-Giken.Co.,Ltd,**

TEL 04-2935-1411 <http://www.nissin-giken.co.jp>

To the creation of high value-added technology  
and innovative new leap



Global brilliance



Creation of unknown technology born  
from the Triangle



GlobalWafers Japan

6-861-5, Seiro-machi Higashikou, Kitakanbaragun, Niigata,  
957-0197, JAPAN

Phone: +81-25-256-3200      Facsimile: +81-25-256-1148

URL : <http://www.sas-globalwafers.co.jp/>

## 日本セミラボ株式会社

本사를ハンガリーに構え、월드ワ이드に事業展開する Semilab 社は半導体製造の評価・測定装置で世界トップクラスのシェアを保持しています。

日本法人である日本セミラボ社より高抵抗測定装置(新製品)、最新小型ホール効果測定機(新製品)、分光エリプソメーター等のご紹介をいたします。



### ★新製品紹介：超高抵抗品の抵抗測定機

**COREMA-2000**：旧 SemiMap 社の技術を引き継ぎました。

非接触・非破壊で各種化合物半導体(GaAs, SiC, GaN, CdTe, InP 等)の高抵抗材料の測定が可能です。(1x10<sup>5</sup>-1x10<sup>12</sup> Ωcm)

またマッピング表示も可能で工程管理、装置管理に最適です。

Semilab の技術を得て精度、信頼性がさらに向上しました。

### ★新製品紹介：ホール効果測定装置 / 少数キャリアの分離が可能(オプション)

**PDL-1000**：IBM 社が開発した技術を搭載した新しい卓上型ホール効果測定装置です

AC/DC 両磁界方式、ロックインアンプおよびフーリエ変換解析を組み合わせることにより、広い測定レンジでも省スペース化を実現しました。



### ●分光エリプソ(SOPLA の技術を継承したベストセラーシリーズ)

**SE-2000 シリーズ**：長年の実績で培われた経験と技術を継承しつ

つ、数多くのお客様の声を元に改善を行い測定精度、操作性、安定

性の向上を実現しました。使い勝手の良い解析ソフトウェアと

豊富なデータベースで、研究開発からインライン生産品質管理な

ど様々な用途でご使用いただけます。ラインナップ、オプション

とも豊富に揃っています。



### ●高感度 DLTS (Deep Level Transient Spectroscopy)

**DLS-83D/2000**：SEMILAB 社製 DLTS 測定システム DLS シリーズは高感度にも拘わらず、

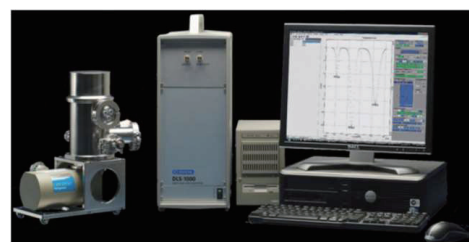
使い易いデジタル/アナログ式を採用しております。

S/N比をアナログで保持し、デジタルで使い易さを実現しております。

10<sup>9</sup>cm<sup>3</sup>レベルのバルク内欠陥、界面準位の

高感度な測定に対応し、ライブラリーを標準装備し

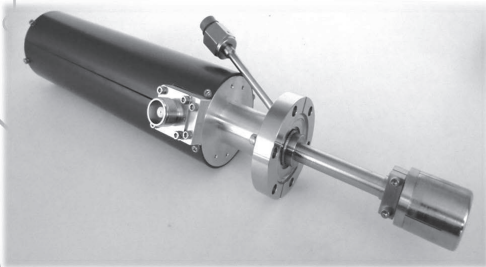
解析を容易にしております。豊富なオプション対応



### ●分光 PL(SPL)、化合物向け PL 測定機(LumiIR)、ナノインデント、卓上 AFM 等

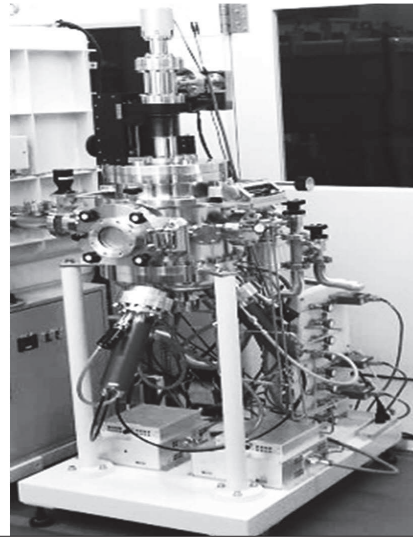
# Kenix's PGS Sputtering

Pressure Gradient Sputtering



## High density Sputtering Cathode

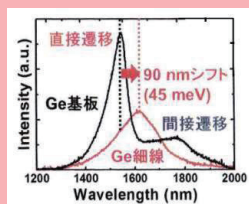
Kenix Corporation  
2-15-501 hojyoguchi,himeji,hyogo,670-0935,JAPAN  
kenix@leto.eonet.ne.jp  
<http://www.kenix.jp>



## PGS sputtering System

PGS Sputtering by *kenix*

## 顕微赤外PLスペクトル測定装置



ゲルマニウムのPLスペクトル測定  
(データ提供: 大阪大学大学院 渡部・志村研究室)

顕微赤外PLスペクトル測定装置は、赤外領域での色収差補正やInGaAs赤外マルチチャンネルディテクタに対応した光学設計、専用ノイズ除去ソフトウェアなど、長年のPL装置開発によるフォトンデザイン独自のノウハウを遺憾なく発揮したスペクトル測定装置で、S/Nの良いスペクトルを得ることができます。また、試料の面内分布を測定するマッピング機能、低温PL測定用のクライオスタットやクライオスタット周辺装置など、多くの関連装置も用意しています。

PHOTON Design

株式会社 **フォトンデザイン**

〒115-0043 東京都北区神谷2-17-1

Phone: 03-5249-5705

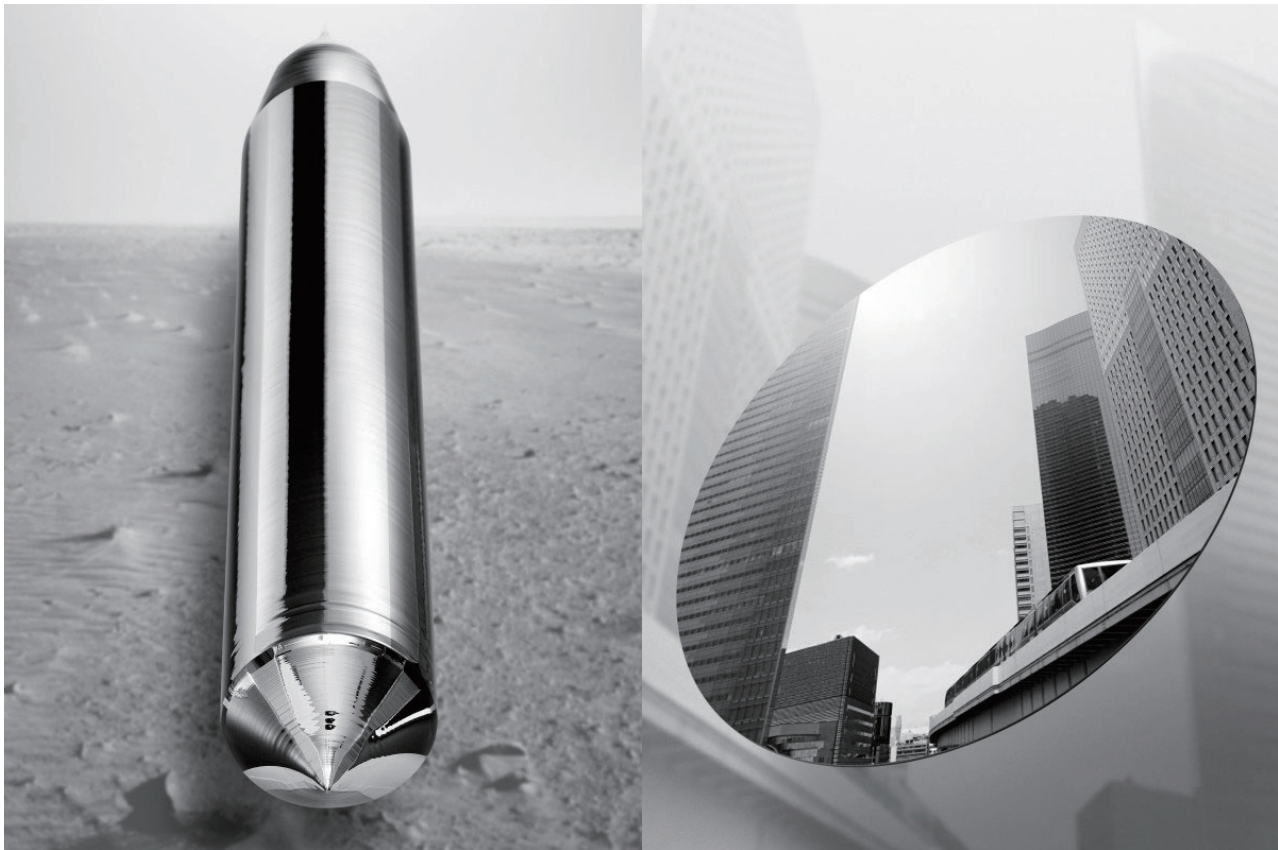
Fax: 03-5249-5706

E-mail: [sales@photondesign.co.jp](mailto:sales@photondesign.co.jp)



## For All Innovation

SUMCO manufactures high quality silicon wafers for semiconductors, meeting various needs of customers.



**Seavans North,  
1-2-1 Shibaura, Minato-ku, Tokyo 105-8634, Japan  
Tel : +81-3-5444-0808 Fax: +81-3-5444-0809  
URL: <https://www.sumcosi.com/english/>**

次世代開発型装置  
**Atomic Layer Deposition Systems**  
**ALD System MO-ZERO10**



新構造・新素材  
 AI時代に向けたプロセス  
 新たなチャレンジが始まっています

特材ガス導入ができる生産開発8inch ALD装置です  
 MOラインの追加が可能

MO-CVD System  
**MO-ZERO1 SP**



MOラインの追加が可能  
 開発向けに適したALD装置です  
 2~8inch PC Control Custom Possible

MO-CVD System  
**MO-ZERO2 SP Plasma**



MOラインの追加が可能  
 開発向けに適したALD装置です  
 2~8inch PC Control Custom Possible

ALDは近年各種アプリケーションへの応用が飛躍的に増加  
 半導体、化合物半導体デバイスの他、MEMS/NEMS (micro/nanoelectromechanical systems)  
 光学薄膜、レーザー薄膜、コーティング、腐食防止、2次電池、太陽電池などに代表される再生可能エネルギー  
 医療機器、生体材料、湿気防止バリアー、ガラスのクラック防止保護膜など 様々な分野に広がりを見せています  
 TMA B(CH<sub>3</sub>)<sub>3</sub> CH<sub>3</sub>SiCl<sub>3</sub> TDMAA Ru(EtCp)<sub>2</sub> BEMAS MgCp<sub>2</sub> TBA Li(t-OBu) POC<sub>13</sub> DEZ など  
 様々な材料の提案が可能です





# X-ray Single Crystal Orientation System

## s-Laue

Demo movie



— Desktop, Easy Measurement —

### Application / Features

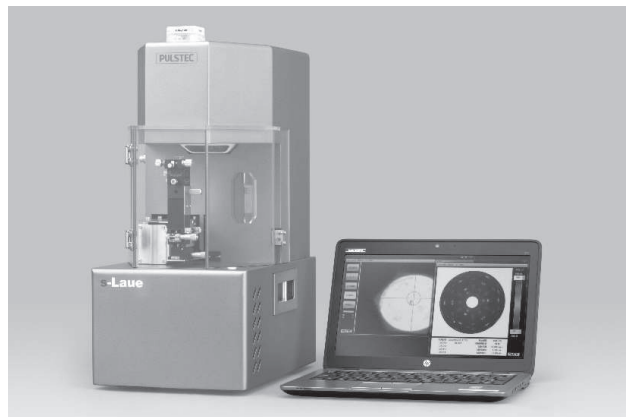
- ◆ Orientation check · Adjustment
- ◆ Crystalline check
- ◆ Air cooling · Compact
- ◆ Easy operation · Fast measurement

### Specification

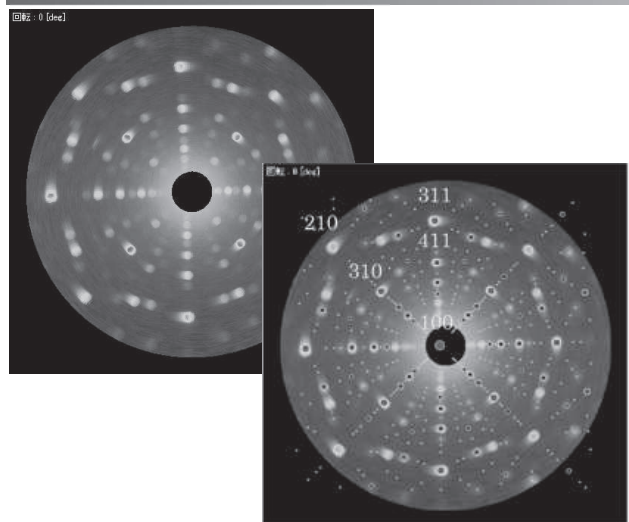
X-ray source	W (Tungsten)
Voltage/Current	30kV/1.5mA
Cooling	Air cool
Incident angle	0 degree
Irradiation spot	φ1.0mm (Standard collimator)
Sample distance	27mm
Measurement time	60secs ※Typical
Sample stage	6 axis (Θ/Tan./Rad./X/Y/Z)
Diameter	W224mmD364mmH480mm
Weight	Approx. 24kg
Power	AC100~240V,50/60Hz
Power consumption	150W max
Other	Door Interlock

※Please feel free to ask if the sample is large or on-site measurement, such as single crystal turbine blade.  
Portable type will be available.

### Configuration



### Output image



7000-35 Nakagawa, Hosoe-cho, kita-ku,  
Hamamatsu-city, Shizuoka 4311304 JAPAN  
TEL+81(0)535223611 FAX +81(0)535223666  
E-mail: sales@pulstec.co.jp

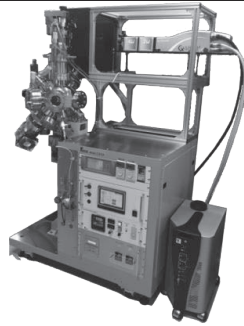
**PULSTEC**

**Pulstec Industrial Co.,Ltd.**

URL: <https://www.pulstec.co.jp/en/>

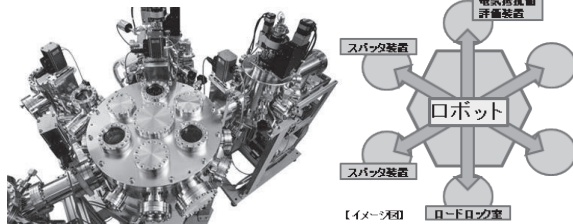


# (株) パスカルの 真空成膜・クラスターシステム



## PLDベーシック

- ミニマルサイズにまとめた新型PLD
- ハイエンドマシンに近い性能を得るための拡張性
- ハロゲンランプ基板加熱を標準装備
- 4円で自転・ツイスト機能を有したターゲットマニピュレーター
- RHEED, ロードロックチャンバー等の拡張が可能



## DL真空成膜システム

- クラスターシステム～AIとロボット技術の融合～
- AIとコンピューターでのロボット制御により、自動搬送・成膜・評価・最適化を実現
- ロボット制御により、PLD・スパッタ・各種評価装置へのアクセスが可能
- 容易なシステム拡張により、複数台の成膜装置・評価装置への接続が可能

成膜・評価・最適化サイクルの自動化を実現！

### 取扱商品

- アジレント(バリアン)社/真空ポンプ・真空計・その他真空部品
- 超高真空ビューイングポート ● ベリリウムウインドウ ● 電流導入端子 ● 極薄フォイル
- 超高真空/マニピュレーター・トランスファーロード・回転導入・直線導入機
- 真空コンポーネント/ラジカルビーム源・イオン源・マグネトロンスパッタ源・K-セル・RHEED
- 真空システム/各種PLD・レーザーMBE装置・各種スパッタ装置
- DL真空成膜システム ● 原子散乱表面分析装置



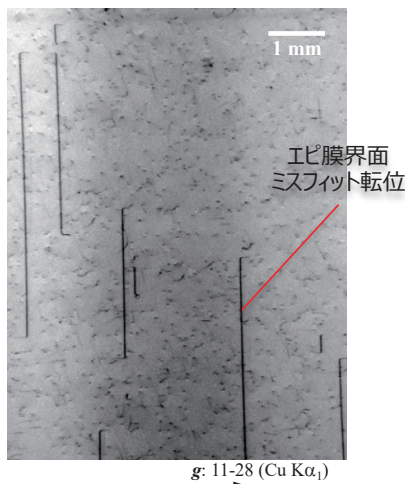
株式会社 パスカル

本社 〒545-0011 大阪市阿倍野区昭和町1丁目16番4号  
TEL: 06-6626-1321(代) FAX: 06-6626-1323  
関東支所 〒352-0001 埼玉県新座市東北2丁目30番26号  
(三上ビル3階B)  
TEL: 048-476-8741(代) FAX: 048-476-8713  
URL <http://www.pascal-co-ltd.co.jp/>  
E-Mail [pascal@pascal-co-ltd.co.jp](mailto:pascal@pascal-co-ltd.co.jp)

## X線トポグラフィメーキングシステム

# XRTmicron

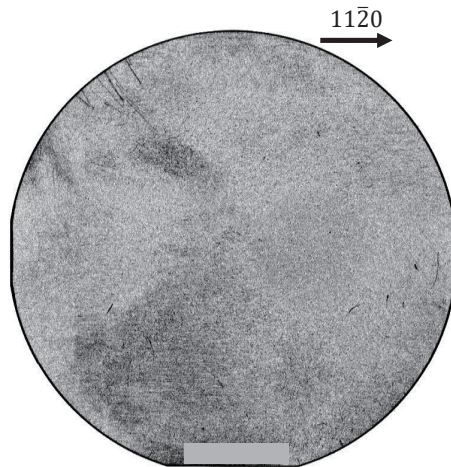
### 高分解能測定



### SiC エピタキシャルウェーハ

Cu K $\alpha$  による反射法による撮影, TSD, BPD, エピ膜界面のミスフィット転位が観察できます。

### 高速測定 (1.5 min)



3インチ SiC ウェーハ  
透過法全面高速測定



単結晶基板評価に広く活用していただいている  
**XRTmicron**  
に**高速測定モード**を追加

従来からの高分解能測定に加え、300 mmウェーハ全面測定に要する時間を5分程度に短縮できるハイスループットモードを追加しました。

広く、ウェーハの品質管理への活用をご検討ください。



株式会社 リガク

〒196-8666 東京都昭島市松原町3-9-12  
☎ (042) 545-8111 (代表電話案内) FAX: (042) 544-9795

<http://www.rigaku.co.jp/>

圧倒的な情報密度と高速性！

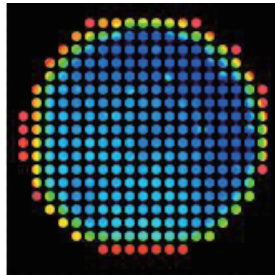
400万点90秒※で膜厚を全面測定

# 膜厚分布測定装置 FiDiCa®

ウェハの全面測定例

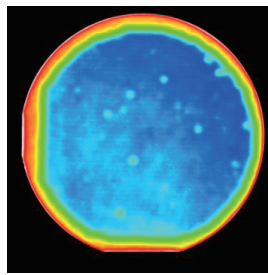
SOIウェハの全面測定例

【従来法】  
エリプソメトリ /  
分光干渉膜厚計

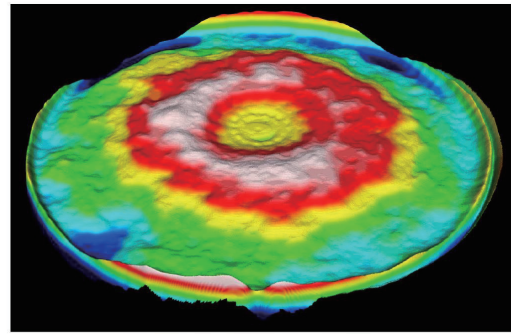


1万点/数時間

FiDiCa®



400万点/90秒



117nm 119nm 121nm

※材質・条件によります。



JFE テクノリサーチ 株式会社

<https://www.jfe-tec.co.jp>

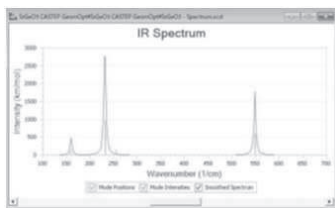
DAIKIN

## 分子シミュレーションソフトウェア Materials Studio

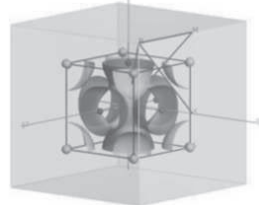
シリコン材料の研究に変革をもたらす先進の分子シミュレーション

Materials Studio® は、画期的な躍進をもたらす研究に携わる化学、物理学、材料科学の研究者に、新しい研究方法を提案します。CASTEPでは各種スペクトル予測が可能となります。

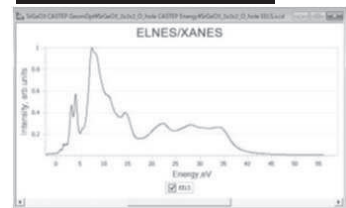
・ IR・ラマンスペクトル



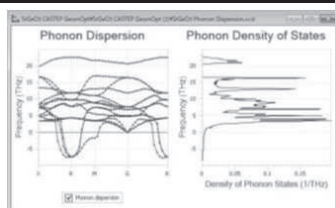
・ブリリアンゾーン、電子密度、ポテンシャルなどの3次元表示



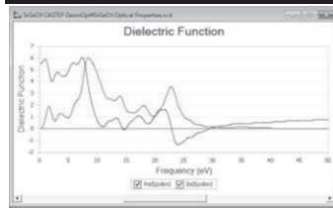
・内殻励起スペクトル (ELNES, XANES)



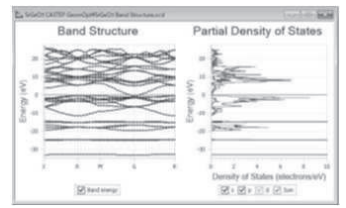
・フォノン分散・状態密度  
自由エネルギー等の熱力学的特性



・誘電関数・その他光学特性  
(屈折率・反射率・吸収係数)



・バンド構造・状態密度



ダイキン工業ホームページで、様々な論文事例をご紹介します  
<https://www.comtec.daikin.co.jp/SC/paper/>

デザイン／DTP／カラーオンデマンド・オフセット印刷／製本／発送業務

多様なニーズに  
お応えします



株式会社 **秋巧社**

<http://www.shukou-sha.co.jp>

〒162-0818 東京都新宿区築地町17番地

TEL. 03-3260-3884 FAX. 03-3260-3885



# 8th JSPS S i l i con Symposium T i metabl e

Nov. 7 (Mbn)

<b>Registration open</b>	<b>12: 00</b>
<b>Opening Remarks</b>	<b>13: 15-13: 30</b>
<b>Afternoon</b>	<b>13: 30-19: 30</b>
<b>120 mi n</b>	<b>13: 30-15: 30</b>
<b>Sessi on-A</b>	
A-1 T. Uj i hara	30 mi n
A-2 M. Taji ma	30 mi n
A-3 D. Macdonal d (Remote)	30 mi n
A-4 K. Kaneko	30 mi n
<b>Coffee Break</b>	<b>15: 30-15: 50</b>
<b>66 mi n (3 mi n/paper)</b>	<b>15: 50-17: 00</b>
<b>Sessi on-P: Short Presentation for Poster</b>	
P-1 H. Iwashiro	P-13 T. Shi nura
P-2 Y. Mukai yama	P-14 H. Myagawa
P-3 A. Sada	P-15 T. Iwai
P-4 Y. Fukui	P-16 K. Sahara
P-5 H. Tanaka	P-17 Y. Ito
P-6 D. Takeuchi	P-18 Y. Noda
P-7 J. Yuan	P-19 M. Sato
P-8 K. Qrote	P-20 K. Yamanaka
P-9 S. Sasaki	
P-10 E. Kami yama	P-22 S. Goll apudi
P-11 Y. Terada	P-23 I. Takahashi
P-12 K. Tanahashi	
<b>Coffee Break</b>	<b>17: 00-17: 20</b>
<b>150 mi n</b>	<b>17: 20-19: 50</b>
<b>Sessi on-P: Poster Presentation</b>	
Posters P-1 ~ P-23	

Nov. 8 (Tue)

<b>Mbrni ng</b>	<b>9: 30-11: 30</b>
<b>60 mi n</b>	<b>9: 30-10: 30</b>
<b>Sessi on-B</b>	
B-2 K. Sasaki	30 mi n
B-3 R. Yokogawa	30 mi n
<b>Coffee Break</b>	<b>10: 30-11: 00</b>
<b>30 mi n</b>	<b>11: 00-12: 00</b>
<b>Sessi on-C</b>	
C-1 C. Bal kas	30 mi n
C-2 M. Dudl ey	30 mi n
<b>Photo Sessi on</b>	<b>12: 00</b>
<b>Lunch Break</b>	<b>12: 00-14: 00</b>
<b>Afternoon</b>	<b>14: 00-17: 00</b>
<b>60 mi n</b>	<b>14: 00-15: 00</b>
<b>Sessi on-D</b>	
D-2 G. K i ssi nger	30 mi n
D-3 H. Sudo (Remote)	30 mi n
<b>Coffee Break</b>	<b>15: 00-15: 30</b>
<b>120 mi n</b>	<b>15: 30-17: 30</b>
<b>Sessi on-E</b>	
E-1 N. Mangel i nck-Nbél (Remote)	30 mi n
E-2 D. Yang (Remote)	30 mi n
E-3 M. Meneghi ni (Remote)	30 mi n
E-4 J. Murphy (Remote)	30 mi n
<b>Optional Dinner (ANA Hotel)</b>	<b>18: 00-20: 00</b>

Nov. 9 (Wed)

<b>Mbrni ng</b>	<b>9: 30-11: 30</b>
<b>120 mi n</b>	<b>9: 30-11: 30</b>
<b>Sessi on-F</b>	
F-1 T. Chshi ma	30 mi n
F-2 T. Yokoi	30 mi n
F-3 N. Sato	30 mi n
F-4 T. Mbr i	30 mi n
<b>Lunch Break</b>	<b>11: 30-13: 00</b>
<b>Afternoon</b>	<b>13: 00-14: 00</b>
<b>60 mi n</b>	<b>13: 00-14: 00</b>
<b>Sessi on-G</b>	
G-1 Y. Nagashi ma	30 mi n
G-2 A. M nani kawa	30 mi n
<b>Closi ng Remarks</b>	<b>14: 00-14: 15</b>