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Abstract

Ni(10 at.% Pt) monosilicide is used as contact in microelectronics but suffers from degradation at relatively low temperatures due to agglomeration. Recent results obtained on 28 nm-FDSOI microelectronics devices have demonstrated severe yield loss after an anneal at 550 °C/2 h linked to Ni(Pt)Si film dewetting. Such agglomeration thermal budget is 100 °C lower than the ones measured on blanket wafers with in-situ or ex-situ four-point probe measurements. In this context, the aim of this paper is to investigate the effect Ni(Pt)Si formation process on the Ni(Pt)Si agglomeration using different approaches as (i) the classical one in which one anneal is applied to form silicide and leads also to agglomeration, (ii) the silicide formation through the standard SALICIDE process, "Self-Aligned Silicide", and a subsequent anneal to induce agglomeration, and (iii) the standard SALICIDE process for silicide formation followed by an encapsulation of the top silicide surface by a SiN layer as applied in devices, and submitted finally to the agglomeration anneal. Our work demonstrated that the film thermal stability is influenced by the sequencing of the selective etch (SE) in the formation process and whether it is formed by a single or a double anneal. Another conclusion of this work is that four-point probe measurements are not sensitive enough to well estimate the real starting point of agglomeration phenomenon which is detrimental for devices (holes formation at the triple junctions). Some additional characterizations such as tilted Scanning Electron Microscopy (tilted SEM) are deeply needed for an accurate determination of agglomeration thermal budget. This study allows clarifying the main parameters leading to agglomeration: the film thickness and the grain size appear to be the more important ones.

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Keywords

Ni(Pt)Si silicide, agglomeration, partial reaction, microstructure, 3D sequential integration.

1. Introduction

In microelectronics devices, for technology nodes below 65 nm, the Ni-based silicide has been widely used as contacts on active Si regions (such as gate, source, and drain) due to its low resistivity, low thermal budget, and low silicon consumption during the NiSi formation [1]. On one hand, even though Ni silicides present attractive advantages as contact materials, two major drawbacks occurring at high temperatures could be underlined, *i.e.* the formation of the high-resistive $NiSi_2$ phase [2], and the NiSi thin film agglomeration (also called dewetting), [3]–[6]. As the alloying of Ni with Pt has allowed to postpone the formation of $NiSi_2$ to high temperature, the agglomeration has become the main concern for contacts based on Ni(Pt)Si [2]. Agglomeration is driven by the decrease of interfacial energies and its kinetics is controlled usually by diffusion (surface, volume, grain boundaries and/or interface). Consequently, agglomeration occurs for a combination of time and temperature and thus a thermal budget. As detailed by Geenen *et al*. [6], the agglomeration thermal budget is lower for thinner Ni(Pt)Si layers, *i.e.* severe agglomeration is detected after an annealing around 650 °C for 10 nm-thick $Ni_{0.9}Pt_{0.1}$ deposited films. On the other hand, the emergence of Fully Depleted Silicon On Isolator (FDSOI) technology, for the 28 nm node mainly, has paved the route to the reduction of silicide thickness for new complementary-metal-oxide-semiconductors CMOS) devices integrations [7]. Nowadays the typical Ni-silicide thickness for current "silicide first" technology is comprised between 10 and 15 nm [8]. To prevent an early morphological degradation of Ni-silicide films, several alloys were studied and a strong reduction of agglomeration sensitivity was demonstrated by addition of Pt [9]. Two main changes induced by the Pt alloying were proposed to explain such observations: the slow-down of Ni and Si atoms diffusion at the silicide/substrate interface [10], [11],

and near the grain boundaries [9], and the lowering of axiotaxy texture with Pt introduction [12]. Some recent results obtained on 28 nm-FDSOI devices showed that the agglomeration thermal budget seems to be lower in devices than the one usually reported for blanket experiments as previously introduced [13]. For this previous study, long annealing of 2 h, between 450 and 650 °C, were applied after the complete standard process flow of dies. The sheet resistances R_s measured in silicided areas, and yield of Static Random-Access Memory (SRAM) are reproduced in Fig. 1. The concomitant rise of R_s values and non-uniformity after an annealing at 550 °C for 2 h is related to the first stages of Ni(Pt)Si layer agglomeration (Fig. 1a) and leads to a drastic reduction of SRAM yield in that case (about zero, Fig. 1b). Such results might be then considered, in the frame of the emergence of new 3D imaging technologies, as a major concern. Indeed, one of the most promising integration for the newest CMOS Imager Sensor (CIS) is a 3D or 3D-sequential integration (Fig.1, [14]).

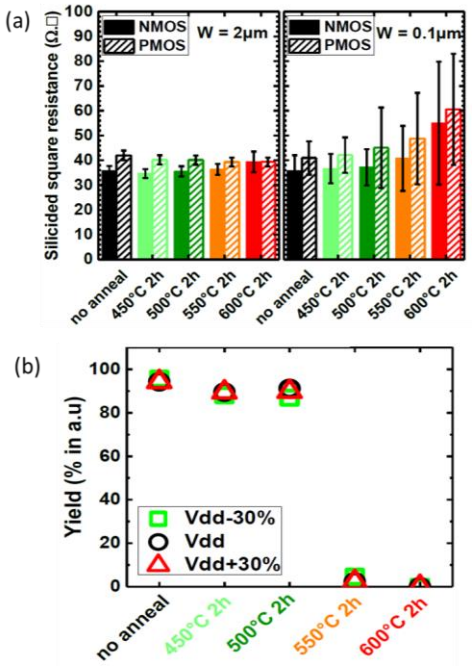

Figure 1. *Square resistance R_s (a) and yield (b) degradation as the function of additional thermal budgets applied on 28 nm FDSOI devices. Increasing of R_s value and its uniformity within the 300 mm-wafer indicates the early stages of Ni(Pt)Si film agglomeration at 550 °C/2 h related to drastic yield loss of the device, reproduced with permissions from* [13].

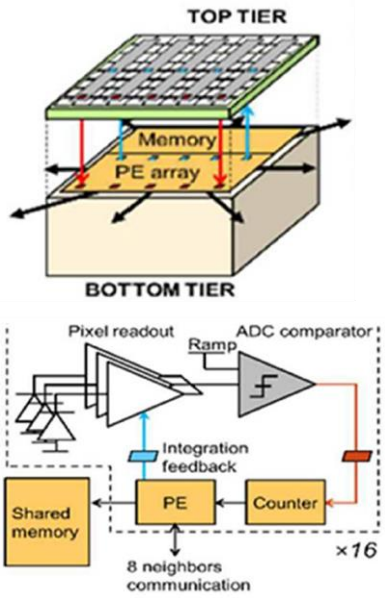

Figure 2. *Bloc diagram of a 3D CMOS Image Sensor (CIS) device including two 300 mm-wafers bonded to each other: the pixels are integrated on the "top tier" and the signal computing is performed by the "bottom tier", reproduced with permissions from* [14].

As 3D-stacked imager deals with a dual layer device, a CIS sensor is built on the top of an up-to-date CMOS device layer (Fig. 2). Consequently, this new technology requests additional thermal treatments at high temperatures, which might be detrimental for Ni(Pt)Si film morphological stability.

In this paper, we study the agglomeration of thin Ni(Pt)Si layers through different approaches: 1) the classical approach with only one anneal leading to the silicide formation and eventually to agglomeration (similar to in-situ and ex-situ results reported in literature) [6]; 2) the classical silicide formation through the standard SALICIDE process, "Self-Aligned Silicide", (including two rapid thermal annealings : RTA1, selective etch (SE), and RTA2) and a subsequent anneal to induce agglomeration, and 3) an alternative version of the second scenario, where the Ni(Pt)Si is encapsulated by a compressive SiN layer, as in real devices, before applying the final annealing to induce agglomeration. Sheet resistance (R_s) measurements as well as morphological, and microstructural characterizations are used to identify the thermal budget for agglomeration, and the main changes induced by agglomeration phenomenon for the three approaches.

2. Experimental

Three sets of samples were thus prepared for this study on monocrystalline Si(100) 300 mm-wafers using the same procedure for cleaning and deposition. After a wet cleaning of the top surface

of Si based on HF-0.5 % diluted solution, an in-situ remote plasma NF_3/NH_3 chemical etch is applied on all wafers to remove native Si oxide prior to the growth by Physical Vapor Deposition (PVD) of a 10 nm-thick Ni(10 at.% Pt) layer. To prevent any oxidation, a TiN capping layer is deposited without air-break on the top of the Ni(Pt) film.

For the first set of samples (referred in the following as series 1), the classical approach to identify the agglomeration thermal budget is used i.e., applying a unique Rapid Thermal Annealing (RTA) to the system to induce both the silicide formation and the agglomeration of the Ni(Pt)Si layer. The RTA temperature was varied between 400 and 800 °C with a duration of 30 s for each anneal. This annealing is notified in the following as RTAD to explicit that the dewetting of silicide layer occurs during this thermal treatment. For the second set (series 2), the classical silicide integration scheme (Salicide process) is performed on similar substrates before applying the different RTAD treatments. In this approach, a first RTA is set at 230 °C/20 s to form the Ni-rich phases (RTA1). The reaction of the Ni(Pt) layer is partial meaning that a part of the metal layer remains after RTA1 annealing [15]. Then, the excess of reactive metal and the TiN capping layer are removed during the SE, inside a hot H_2SO_4/H_2O_2 solution, and the mono-silicide Ni(Pt)Si layer is subsequently formed during a second RTA at 390 °C for 30 s (RTA2). At the end, as for series 1, a RTAD process is applied to induce agglomeration. The last set of samples (series 3) is identical to the second one but includes the deposition of a compressive SiN capping layer on the top of the silicide film after RTA2, and before applying RTAD annealings. For all samples, sheet resistance (R_s) measurements and tilted-view SEM observations (Scanning Electron Microscopy) are systematically applied. Four-point probe R_s measurements were performed with a KLA Tencor RS100 resistivity mapping system, equipped with Jandel B-type probes. A 49-points contour map with 6 mm edge exclusion was used.

Final Ni(Pt)Si microstructure, agglomerated grain shapes, main species atomic concentrations inside grains, and at interfaces as well as texture for non-agglomerated samples, are then determined by TEM (Transmission Electron Microscopy), Energy Dispersive X-ray (EDX), and Automated Crystal Orientation Mapping (ACOM-TEM) [16].

3. Results

Figure 3 shows the R_s evolution, measured through a 49-points mapping, for the three types of samples prepared for this study (series 1 to 3). A significant rise of the R_s values, usually related to agglomeration phenomenon, is clearly observed for all samples. For series 1, R_s is very stable until a thermal budget of 700 °C/30 s. At 800 °C, an abrupt increase of the R_s is measured and this degradation presents a high kinetics. For the series 2 and 3, for which the silicide is formed through the standard process flow before applying RTAD treatments, the R_s evolution is quite different. For RTAD below to 600 °C, the R_s values are slightly higher for the series 2 and 3 than for series 1, indicating a change in film thickness and/or microstructure. Thickness measurement by ellipsometry shows that it is mainly due to a change in thickness since the intrinsic resistivity ρ, calculated though R_s and ellipsometry is almost similar for all series after RTAD treatments at 400, 500 and 600 °C for 30 s. For series 2 and 3 the R_s values uniformity is degraded at 600 °C. The beginning of the Ni(Pt)Si agglomeration is measured by R_s at 600 °C/30 s for both series, significantly lower than for series 1 (100 °C at minimum).

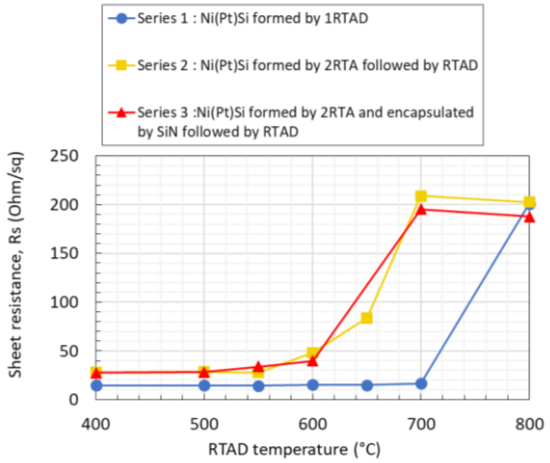

Figure 3. *R_s measurements of silicide layers formed from the reaction of a 10 nm Ni(10 at.% Pt) film with Si substrates. For series 1 the classical method is used (based on a single RTA, noted RTAD) contrary to the series 2 and 3, for which the RTAD is applied after performing the complete silicide process.*

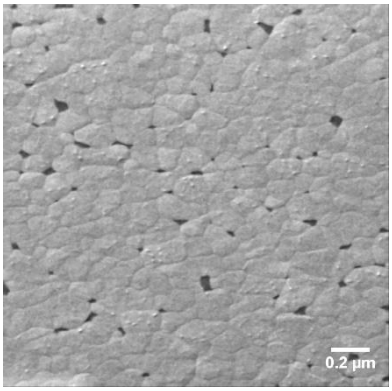

Figure 4. *Tilted-view SEM image showing the top surface of Ni(Pt)Si layer of series 2 when RTAD at 550 °C is applied after the complete silicide process.*

However, the R_s technique may not be sensitive enough to the early stages of agglomeration. Indeed, the tilted SEM view of Ni(Pt)Si surface of series 2 sample after a RTAD at 550 °C reveals some dark regions that corresponds to exposed Si surface and thus to holes in the silicide layer. These small holes are generally observed at triple junctions and sometimes inside a single grain boundary. As detailed in references [17], [18], these holes represent the very early stages of film agglomeration but were not observed before in the case of silicide thin film.

In Figure 5, the tilted SEM views performed on the samples of series 1 and 2 permit to follow the Ni(Pt)Si film morphology evolution. In agreement with the previous R_s results, the agglomeration takes place from 700 °C for series 1 (exposed Si observed, Fig. 5.f), and from 600 °C for series 2 since a large part of the sample surface correspond to exposed Si (dark contrast in Fig. 5.f and 5.k respectively). However, note that while no increase in R_s is measured at 700 °C for series 1 , several holes (i.e., exposed Si) are observed in the corresponding SEM image (Fig. 5.f). While the R_s values only start to increase at 600 °C, a clear, uniform, and advanced agglomeration is observed on SEM images (Fig. 5.k). Furthermore, a few holes are found for the thermal budget of 650 °C/30 s for series 1. SEM appears thus to detect agglomeration before R_s. This is illustrated by Fig. 6 that reports the change in the fraction of exposed silicon substrate after Ni(Pt)Si film agglomeration, f^{Si}(%) as the function of RTAD temperatures. For the same annealing thermal budget, f^{Si}(%) for series 2 is higher than that of the series 1. Moreover, at 550 °C, f^{Si}(%) is observed to have a slight increase due to the presence of holes as shown by SEM images in Fig. 5(j) for samples of series 2 while the evolution of f^{Si}(%) is stable up to 650 °C for samples of series 1.

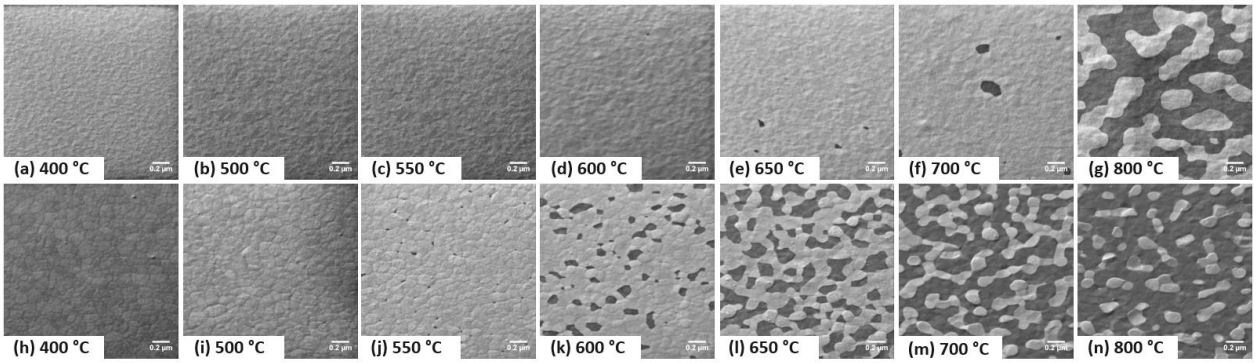

Figure 5. *Images of tilted SEM (45°) showing the top surface of Ni(Pt)Si thin films for series 1 with a single anneal (RTAD) process at 400 (a), 500 (b), 550 (c), 600 (d), 650 (e), 700 (f) and 800 °C (g); and for series 2 with the RTAD is applied after the classical salicide process at the same temperatures. For both series, the characterizations are performed after the selective etching and RTAD is applied for 30 s. Ni(Pt)Si thin film appears in light gray while the darker gray is the exposed Si substrate after film agglomeration.*

To further characterize agglomeration, TEM-EDX characterization results are displayed in the Figures 7 and 8. For the two samples of series 1 submitted to RTAD at 600 °C and 700 °C respectively (Fig. 7), one may note that the top surface of the Ni(Pt)Si layer is still flat and a slight increase of the roughness of Ni(Pt)Si/Si interface is observed for 700 °C (Figs. 7a and b). This increased roughness appears to be related to grain boundaries grooving since the silicide thickness is

smaller at the silicide grain boundaries in figure 7b. For series 2, in Fig. 8, very large silicide grains are observed after a RTAD at 600 °C (Fig. 8a); and the grain shape appears to be very angular near the grain boundaries. At 700 °C, a clear inverse agglomeration is observed as previously reported for NiSi systems [10], and the whole layer is agglomerated (Fig. 8b).

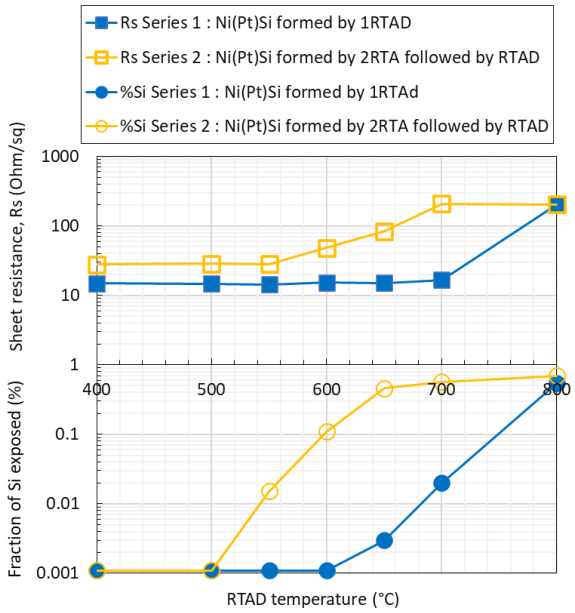

Figure 6. *Computed fraction of Si exposed (%) extracted from tilted SEM images presented in figure 5 as function of RTAD thermal budgets for series 1 and 2.*

Table 1 summarizes the average atomic concentrations of Pt, Ni, and Si inside silicide layers as well as the average thickness for these samples as obtained by the EDX mappings and profiles. From this, we could conclude that the early stages of agglomeration for series 1 do not imply significant changes in terms of main elements concentration and observed Ni(Pt)Si thicknesses. For series 2, a significant increase of Ni(Pt)Si thickness is measured in correlation with the inverse agglomeration phenomenon.

Table 1*. Average Ni(Pt)Si thickness and atomic concentrations of Ni, Si, and Pt elements extracted from EDX mappings and profiles (perpendicular to the sample surface) inside the silicide layer for samples of series 1 and 2 after a RTAD at 600 and 700 °C.*

			Atomic concentration inside the silicide layer (at. %)			
	RTAD T(°C)	NiSi Thickness (nm)	Ni	Si	Pt	Ni + Pt
Series 1	600	21.3	45.5%	48.6%	2.9%	48.4%
	700	21.0	43.9%	47.0%	2.8%	46.8%
Series 2	600	15.4	47.3%	49.1%	3.2%	50.5%
	700	29.4	47.3%	46.0%	3.6%	50.9%

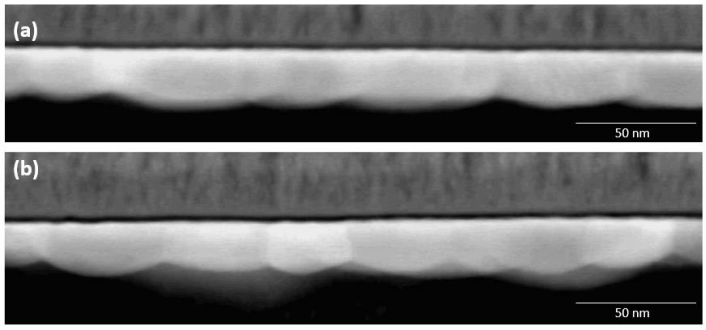

Figure 7. *STEM-HAADF cross-sections for samples of series 1 after a RTAD at 600 °C (a) and at 700 °C (b).*

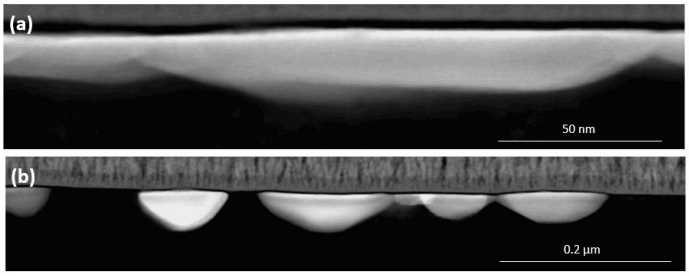

Figure 8. *STEM-HAADF cross-sections for samples of series 2 after a RTAD at 600 °C (a) and at 700 °C (b).*

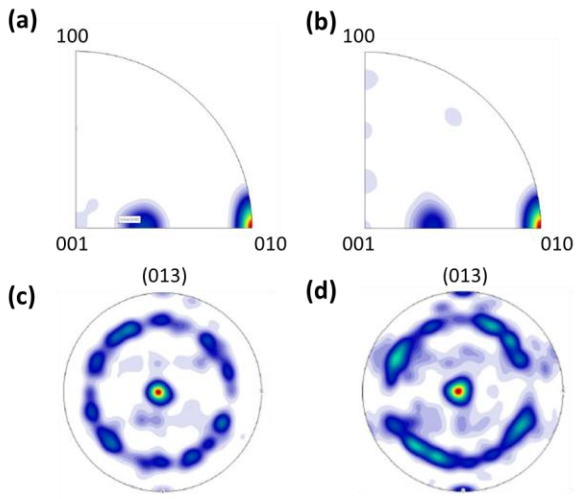

Figure 9. *Inverse pole figures (a,b) of Ni(Pt)Si texture and deduced pole figures (c,d) determined through ACOM-TEM technique for samples of series 1 after a RTAD at 600 °C (a,c) and at 700 °C (b,d).*

Finally, ACOM-TEM performed on series 1 shows that the Ni(Pt)Si layer texture remains almost unchanged after RTAD treatments at 600 °C and 700 °C (see figure 9). A (013) fiber texture aligned on Si(100) planes is detected for both samples and no axiotaxy has been figured out in our case.

4. Discussion

This work is part of a study on the differences regarding Ni(Pt)Si agglomeration sensitivity between integrated devices and blanket experiments. As presented in Figure 1, agglomeration was observed at 550 °C for 28 nm FDSOI devices, which is 100 °C lower (at least) than the usual value reported in literature that are usually obtained through classical R_s measurements (after one single RTA, in-situ, or ex-situ). This degraded stability in devices could be due to changes in several parameters such as : silicide thickness [17], intrinsic stress [17], and/or microstructural properties (texture, grain misalignment [19]). Finally, the highest sensitivity to agglomeration measured in devices could be more basically related to dimensional constraints. Indeed the “small” holes observed in Fig. 4 and 5 have only a small effect on the R_s of a blanket thin film (Fig. 2) but should have a strong effect in a device since their size are larger than the device dimensions. The early stages of agglomeration are detrimental for microelectronics devices. However, the origin and dynamics of such processes are not easily determined through macroscopic R_s measurements and/or SEM top-view observations. In the light of our findings, this can be understood by the strong inverse dewetting process associated with such phenomena. Moreover, matter movements have already damaged the integrity of the bottom interface (Ni(Pt)Si/Si) before leading to a discontinuity at the top surface (Fig. 7 and Fig. 8). Our work allows clarifying some hypotheses about thermal degradation of the Ni silicide layers. First, the difference in thickness could be a major part of explanation. Indeed, the silicide thickness is different for the three series. In general, agglomeration temperature for different systems is given as a function of metal thickness, before any thermal treatments, assuming that the metal is fully consumed (see for instance [1], [3]–[6]). Indeed, if in-situ or ex-situ R_s measurements are performed at a temperature higher than 400 °C (similarly to series 1) after deposition, full consumption of the metal is expected, and the final Ni silicide thickness is maximum. In our case, with 10 nm of Ni(Pt), this thickness should be 21 nm according to the atomic volumes of different phases. As shown in Table 1 for series 1 samples annealed at 600 °C and 700 °C, the final silicide thickness is indeed around 21 nm. In devices (where a maximum silicide thickness of 15 nm is required due to junction depth constraints) as well as for the series 2 and 3, the silicide formation is based on partial reaction leading to thinner silicide layers. As can be seen in Table 1, after a RTAD at 600 °C, the silicide thickness for series 2 sample is indeed around 15 nm. Indeed, for series 2, the selective etching (SE) process removes a fraction of the NiPt layer before the RTA2 treatment, forming a thinner Ni(Pt)Si film. Meanwhile for the series 1, the SE were carried out after RTAD, removing only the TiN capping, and allowing a total consumption of NiPt film. Thus, the film formed by the single anneal process has a higher resistance to agglomeration owing to its higher thickness as compared to the film formed by double anneal (as the standard SALICIDE process, series 2). Both SEM micrographs and R_s behavior demonstrated a degradation 100 °C later in the case of single anneal (series 1) as compared to double anneal (series 2).

Concerning the bi-axial stress which might be introduced by encapsulation of a highly compressive SiN layer, it seems to have a very low impact on Ni(Pt)Si layer stability based on Fig. 3. Moreover, suppression of the free top surface of the silicide layer due to the presence of the SiN layer appears to not introduce any changes in kinetics of agglomeration phenomena, surprisingly. Another major point could be differences in Ni(Pt)Si

grain misalignment linked to the total versus the partial reaction. Actually, no significant variations have been pointed out but precise studies on this aspect will be carried out in the future. At the end, as shown in Figs. 4 and 5, small holes in silicide layer or low-density agglomerated silicide grains do not induce a change in R_s measurements. In details, the R_s evolution , reported in Fig. 3, has clearly demonstrated that the necessary thermal budget to strongly degrade the silicide film stability is 700 °C/30 s for series 1, and 600 °C/30 s for series 2. However, as illustrated in Fig. 5, the presence of holes is already detected at 650 °C/30 s for series 1, and 550 °C/30 s for series 2. This showed that the determination of agglomeration thermal budget with four-point probe technique can be overestimated regarding devices. Indeed, in very small Si actives areas, such transformations of the Ni(Pt)Si film (holes formation) and associated slight change in intrinsic resistivity could be enough to explain the early degradation in devices.

Another possible contribution to agglomeration is the silicide grain size. Indeed, accordingly to the classical models [17], large grain size will promote agglomeration. Figs. 5, 7 and 8 indicate that the grain size is larger for series 2 than for series 1 and thus could, in addition to the difference in thickness, contributes to the decrease in agglomeration temperature.

Finally, the distribution of Pt may also impact agglomeration. Pt can not only change the silicide texture [20], but can also reduce diffusion of Ni and Si along different paths (grain boundary, surface, interface). For agglomeration to occur, diffusion of both Ni and Si is needed, and Luo et al. [10] have demonstrated that Si diffusion should be the limiting (and controlling) mechanism. Pt could play a role on the Si diffusion at the Ni(Pt)Si/Si interface that controls the agglomeration and possibly slows down the agglomeration. Consequently, another interesting point might be that for the SALICIDE process (as series 2 and devices), the selective etching of unreacted metal (including Pt) is performed before the final formation of Ni(Pt)Si layer contrary to series 1, where the selective etching of unreacted metal is applied after the final silicide layer formation. The total Pt concentration in the system could thus be affected by such a process difference, additional measurements being needed to confirm this hypothesis.

Table 2 summarizes the advantages and disadvantages of the three formation approaches.

Table 2. *Advantages and disadvantages of the three different Ni(Pt)Si processes used to form thin Ni(Pt)Si layers in this study : 1RTAD (series 1) , 2RTA+SE (series 2) and 2RTA+SE+SiN (series 3)*

Series	Advantages	Disadvantages
1	• Experimentally achievable thermal budget is 650°C/30s • Shorter process flow	• Film is too thick for device application
2	• Allow to obtain the required silicide for device application • Maintain the fiber texture during RTAD anneal	• Experimentally achievable thermal budget is 550°C/30s • Thinner film • Longer process flow
3	• Allow to obtain the required silicide for device application • Similar R_s behavior with Ni(Pt)Si film in series 2 • No earlier agglomeration is detected	• Difficulty of R_s verification due to dense SiN film

Comparing the three different formation processes, one may notice that the process of series 1 allows the comparison of agglomeration sensitivity with studies performed by other research groups because is it the most common way to form nickel silicide. The interest in the study of series 2 and 3 is the similarities with the standard process flow used in real devices, as Ni(Pt)Si final thickness and top surface configuration. We could underline here that for these series the thermal budget leading to agglomeration is very near than the one determined in devices (C. Cavalcante. *et al.* 2020). If one takes into account, the holes formation detected by SEM, this seems to indicate that this phenomenon is indeed responsible for devices degradation. However, in devices, other phenomenon and/or parameters (stress, confinement…) can contribute to the degradation.

5. Conclusions

During this work, three different approaches to form Ni(Pt)Si thin layers are studied to estimate their impact on film thermal stability, mainly agglomeration sensitivity. For the classical approach (series 1), in which only RTAD treatment is applied, the thermal budget needed to agglomerate is higher than the one for the samples

for which the RTAD is performed after the SALICIDE process (series 2 and 3). This result is certainly mainly due to the larger thickness of silicide layers in the case of the first series due to the full consumption of the metal layer; The difference in sequencing of selective etching process for both series types may also contribute to the change in thermal budget for agglomeration. Surprisingly for the third series, the encapsulation of the Ni(Pt)Si film by thin SiN layer before applying RTAD treatment has shown no change in the R_s behavior, comparing to the series 2 results, i.e., without any encapsulation. Effectively, an earlier agglomeration of silicide thin films due to the compressive strain induced by the SiN layer was at the beginning expected. Another main conclusion of this work is that four-point probe measurements can detect severe agglomeration but are not sensitive enough to well estimate the beginning of agglomeration (holes formation at the triple junctions) phenomenon, which should be detrimental for devices. Some additional characterizations, such as tilted SEM, are deeply needed to an accurate determination of the agglomeration temperature. Even though the reduction of Ni(Pt)Si thickness for series 2 samples (complete SALICIDE process as devices) might explain higher agglomeration sensitivity, several suggestions are formulated to deeply understand the results presented in this paper, opening the route to further investigations.

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