Influence of Si surface preparation on CoSi2 formation and agglomeration

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Keywords

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Abstract

In microelectronics, despite a difficult nucleation of cobalt silicide $CoSi_2$ in small dimensions, the $CoSi_2$ based contacts remain interesting for some specific devices designed in 65 nm technology. Therefore, to promote the formation of $CoSi_2$ in 65 nm technologies, it is possible to interfere on the formation of CoSi, that occurs during RTA1. To this end, the surface preparation of the Si substrate, before the Co deposition, may have an influence on the cobalt silicide phases formation. In this work, different surface preparations (SiCoNi, HF followed by SC1 and HF only), as well as several Soft Sputter Etch, SSE, processes have been applied on Si(100) wafers before the deposition of Co and TiN layers. Depending on the surface preparation, the formation temperatures and/or crystalline orientations for the Co silicide phases, including $CoSi_2$, are different, as observed by XRD and/or EBSD. Four-point probes measurements also show a strong dependency of the $CoSi_2$ agglomeration to the surface preparation scheme. These results highlight the influence of surface preparation on the Co silicides formation and agglomeration and its importance for the integration of $CoSi_2$ films in a 65 nm CMOS technology.

1. Introduction

Silicides have been used for many years in microelectronics, as contact on source, drain and gate of MOS (Metal Oxide Semiconductor) transistors [1]. However, with the decrease in the devices size, and more particularly from the 65 nm CMOS (Complementary Metal Oxide Semiconductor) technology, the low resistivity cobalt disilicide, $CoSi_2$, has been massively replaced by the nickel monosilicide, NiSi [2,3]. Indeed, the $CoSi_2$ phase has been reported to nucleate at the triple junctions of the CoSi phase [4] which is the phase previously formed during the first annealing step (RTA1, for Rapid Thermal Annealing 1) of the Self Aligned SiLICIDE (SALICIDE) process [5–7]. Therefore, by decreasing the transistors size, and thus the contacts size (especially the gate), the number of CoSi grains is reduced, leading to a decrease of the number of nucleation sites available for the $CoSi_2$ nucleation. In addition, other issues have also been observed such as the rise in resistance in very narrow lines caused by the presence of voids or the limited volume of Si available for the reaction since the Silicon On Insulator (SOI) becomes very thin [8,9]. This situation has led to a change of the silicides used in the devices in favor of the nickel monosilicide that is formed by diffusion, ~~and~~ thus not directly impacted by the transistors size, and which consumes less Si.

However, cobalt silicide-based contacts remain interesting in some 65 nm technology devices, such as flash memory and advanced imaging technologies. Therefore, to promote the formation of $CoSi_2$ in 65 nm technologies, it is possible to use methods that favor the $CoSi_2$

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nucleation. One possibility is to interfere on the formation of CoSi, that occurs during RTA1. Since the $CoSi_2$ phase is expected to nucleate on the triple junctions of the CoSi phase, reducing the CoSi grain size should increase the number of $CoSi_2$ nucleation sites and facilitate its formation in small dimensions [10]. Other methods that modify the kinetics and/or thermodynamics of nucleation can influence the $CoSi_2$ formation. To this end, it is possible to play with the surface preparation of the silicon substrate before the metal deposition. Indeed, in the case of a solid-state reaction of a Co thin film deposited on a Si substrate, the phase sequence is as follows:

$$a - Co_{1-x}Si_x \rightarrow Co_2Si \rightarrow CoSi \rightarrow CoSi_2 \quad \text{Eq. 1}$$

with a-$Co_{1-x}Si_x$ an intermixing layer related to the metal deposition process [11].

Since surface preparation is a process commonly used to modify the Si substrate surface [12–16], either by cleaning the Si substrate surface or by growing an oxide layer, it can have an influence on the cobalt silicide phase formation given that the presence of a silicon oxide layer between silicon and metal can prevent or alter the phase formation. Indeed, in the literature, when the formation of Co silicides occurs through an oxide layer (OME process, Oxide Mediated Epitaxy), the phase sequence can be modified [17–21].

In addition, it has also been reported that surface preparation can influence the thermal stability of silicides thin films, which is a key parameter in the performances and reliability of microelectronics devices [12]. Indeed, one of the problems encountered in thin films is agglomeration which depends on several parameters, including the texture of the film. This problem was observed in the case of $CoSi_2$ by TEM by Xiao and al. [22], Sun and al. [23] as well as Gambino and al. [24]. However, the $CoSi_2$ phase has a CaF_2 structure with a lattice parameter a_{CoSi2} = 0.5365 nm very close to the lattice parameter of the Si cubic diamond structure a_{Si} = 0.5431 nm at room temperature, that is a 1.2 % lattice mismatch [25,26]. Therefore, the $CoSi_2$ phase can grow in heteroepitaxy on the Si substrate under certain conditions as reported in the literature [27–37]. Furthermore, it has already been reported that the growth of cobalt silicides through an oxide layer leads to a $CoSi_2$ layer in heteroepitaxy with the silicon substrate Si(100) [17,18,21,38]. The heteroepitaxy of the $CoSi_2$ grains with the Si substrate may strongly influence the agglomeration [39,40] since it can play a role on the interface energies [17,22] and thus on the thermal stability of the thin films.

In this study, the influence of different surface preparations on the cobalt silicide phases formation as well as on the morphological degradation of $CoSi_2$ layer at high temperature, agglomeration, was analyzed using XRD, four-point probes measurement, EBSD, AFM and TEM-EDX.

2. Experiments details

Standard 300 mm and 200 mm Si(100) blanket wafers have been used for this study. Five different surface preparations were applied on Si(100) prior the deposition by Physical Vapor Deposition (PVD) of Co and TiN thin films. The targeted thicknesses for each film are respectively 75 and 100 Å. Depending on the wafers, two different tools were used to make these depositions, as reported Table 1. The recipe used for TiN depositions is slightly different for these two tools and results in different intrinsic resistivity. Indeed, the TiN resistivity measured for TiN deposited on substrate with a Si oxide layer using the same recipe than the TiN/Co/Si(100) samples is $\rho_{TiN\ (tool1)}$ = 209 µOhm.cm for Tool 1 and for Tool 2 is $\rho_{TiN\ (tool2)}$ = 174 µOhm.cm. The HF (hydrofluoric acid) solution is a wet etching process for removing native oxide from the silicon surface according to the reaction:

$$SiO_2 + 4\,HF \rightarrow SiF_4 + 2\,H_2O \quad \text{Eq. 2}$$

It has been used on all samples, concentrated at 0.5 % of HF and performed at room temperature. The SC1 (Standard Clean 1) is a wet etch based on a $NH_4OH/H_2O_2/H_2O$ chemical mixture (as ratio 1 : 2 : 80) heated to 60 °C to recreate a high-quality oxide layer having a thickness about 1.4 nm presenting a controlled composition and uniformity.

The SiCoNi™ surface preparation is a dry NF_3/NH_3-based chemical etch (from Applied Materials chamber name) [12,13]. This surface preparation has the particularity of using a remote plasma. This means that the plasma is not directly created near the Si surface but allows the formation of a NH_4F compounds (Eq. 3) which, brought to the Si surface, react with the silicon oxide and form salts (Eq. 4). Then, fluorine salts are sublimated by bringing the wafer surface closer to a showerhead heated at 180 °C (Eq. 5) [13,41].

$$NH_3 + NF_3 \rightarrow NH_4F \quad \text{Eq. 3}$$

$$NH_4F + SiO_2 \rightarrow (NH_4)_2SiF_6 + H_2O \quad \text{Eq. 4}$$

$$(NH_4)_2SiF_6 \rightarrow SiF_6 + NH_3 \quad \text{Eq. 5}$$

The abbreviation SSE corresponds to Soft Sputter Etch which deals with an Ar plasma bombardment of the Si surface prior Co deposition. One might notice that SSE and SiCoNi pre-cleans are performed in the same cluster as Co and TiN layers deposition under a secondary vacuum and without air-break. Such pre-cleans could be considered as in-situ surface preparation processes. That is not the case of wet cleanings which are, by definition, ex-situ ones.

To well identify different SSE surface preparation, the number corresponding to the thickness of oxide etched is added. For example, SSE12 means a removed oxide amount measured by ellipsometry prior and after applying on a thermally oxidized blanket wafer of 12 Å. HF and SiCoNi processes are both used to etch the oxide layer from the wafer surface but SiCoNi is more efficient to remove the silicon oxide. The SC1 solution is used to recreate a high-quality oxide layer while SSE is used to etch a certain thickness of this oxide layer. What's more, the SSE process introduces defects in the substrate.

The wafers name according to the surface preparation applied on Si(100) wafers before the deposition of Co and TiN layers is given in Table 1.

Table 1

Wafers name according to the surface preparation applied on Si(100) wafers before the deposition of Co and TiN layers.

Wafer name	Tool used	Surface preparation
P1	1	HF + SC1 + SiCoNi
P2	1	HF + SC1 + SSE12
P3	2	HF + SC1 + SSE7
P4	2	HF + SSE7
P5	2	HF "only"

Each wafer was cut in small pieces (about 1x1 cm²) that were subjected to further processing and characterizations. Rapid Thermal Anneals (RTA) were performed on sample pieces systematically by steps of 20 °C between 100 and 700 °C in a first time to roughly scan the phase transformation. In a second time, some temperature ranges of interest were investigated using smaller temperature step of 5 °C. X-Ray Diffraction (XRD) measurements were used to characterize the nature and the texture of phases in presence after RTA treatment. The sheet resistance, Rs, was determined by four-point probes measurements to

obtain additional information on phase formation and agglomeration. Transmission Electron Microscopy and Energy Dispersive X-ray spectroscopy (TEM-EDX) measurements were also performed to determine the thickness and the composition of the layers for each surface preparation. The crystallographic orientation and the size of the $CoSi_2$ grains was determined by Electron BackScattering Diffraction (EBSD) and Atomic Force Microscope (AFM) for two different surface preparations after the complete Salicide process which could descripted by a sequence of RTA1 at 500 °C during 30 s, a selective etch to remove the TiN capping layer and the non-reacted Co, and finally a RTA2 at 790 °C during 20 s.

3. Results

1. TEM-EDX

TEM-EDX measurements have been made on each post-deposition wafer to determine the thickness and the composition of the layers for each surface preparation. Figure 1 shows the TEM micrographs obtained for each sample as detailed in Table 1. From these micrographs, the thickness of the TiN layer and the Co layers can be identified. The TiN thickness varies between 9.4 ± 0.5 nm and 9.9 nm ± 0.5 nm, which is close to the nominal thickness (10 nm). As regards the Co layer, its thickness varies between 5.1 ± 0.4 nm and 5.8 ± 0.4 nm. An intermixing layer with a thickness between 1 ± 0.1 nm and 2 ± 0.2 nm is also present between the Co layer and the Si substrate. It is also possible to observe an oxide layer at the interface between intermixing layer and Si substrate in the case of a surface preparation including SC1 wet clean in addition with SSE pre-clean for P2 (HF + SC1 + SSE12) and P3 (HF + SC1 + SSE7) wafers (Fig. 1.b and 1.c) that appears as a very thin layer with a bright contrast as expected for a light element. On the P2 wafer, the oxide thickness is 0.7 ± 0.1 nm while on the P3 wafer, the oxide thickness is 0.8 ± 0.1 nm. This layer is not observed for P1 (HF + SC1 + SiCoNi), P4 (HF + SSE7) and P5 (HF “only”) wafers (Fig. 1.a, 1.d and 1.e). The oxide layer should be due to the surface preparation since the SC1 solution is used to grow an oxide on the substrate surface. However, it is not present on the P1 wafer because the SiCoNi surface preparation is very effective for removing oxide.

Figure 2 shows the in-depth EDX profiles associated to the TEM images in Fig. 1 for each surface preparation. These measurements allow determining the composition of the different layers in the samples. For the five surface preparations, the same layers as those observed on the TEM micrographs (Fig. 1) can be identified, namely TiN, Co, intermixing and Si substrate. In addition, for the P2 (HF + SC1 + SSE12) and P3 (HF + SC1 + SSE7) wafers, a small peak of oxygen is also present at the interface between the intermixing layer and the Si substrate, confirming the presence for these samples of an interfacial oxide layer. The TiN layers present a composition in Ti and N that are close to each other (between 35 and 40 at. %) for P2 to P5 wafers (respectively HF + SC1 + SSE12, HF + SC1 + SSE7, HF + SSE7 and HF “only”) while for P1 wafer (HF + SC1 + SiCoNi), there is a larger difference in concentration with 40 at. % of N and 30 at. % of Ti. The N and Ti compositions are smaller than expected for TiN and this appears to be linked to the large content of carbon C (around 20 at. %). The carbon contamination is probably introduced during the preparation of the TEM lamella or during the TEM observation and changes the quantification of the measured elements. The lower concentration in Ti for sample P1 is possibly due to a TiN over-oxidation on the surface of this wafer which induces under-detection of the metal element. In the Co layer, the Co concentration varies between 80 and 85 at. % whereas the O concentration varies between 7 and 13 at. % (Table 2). This large value of O concentration is certainly due to a similar contamination than the one for C.

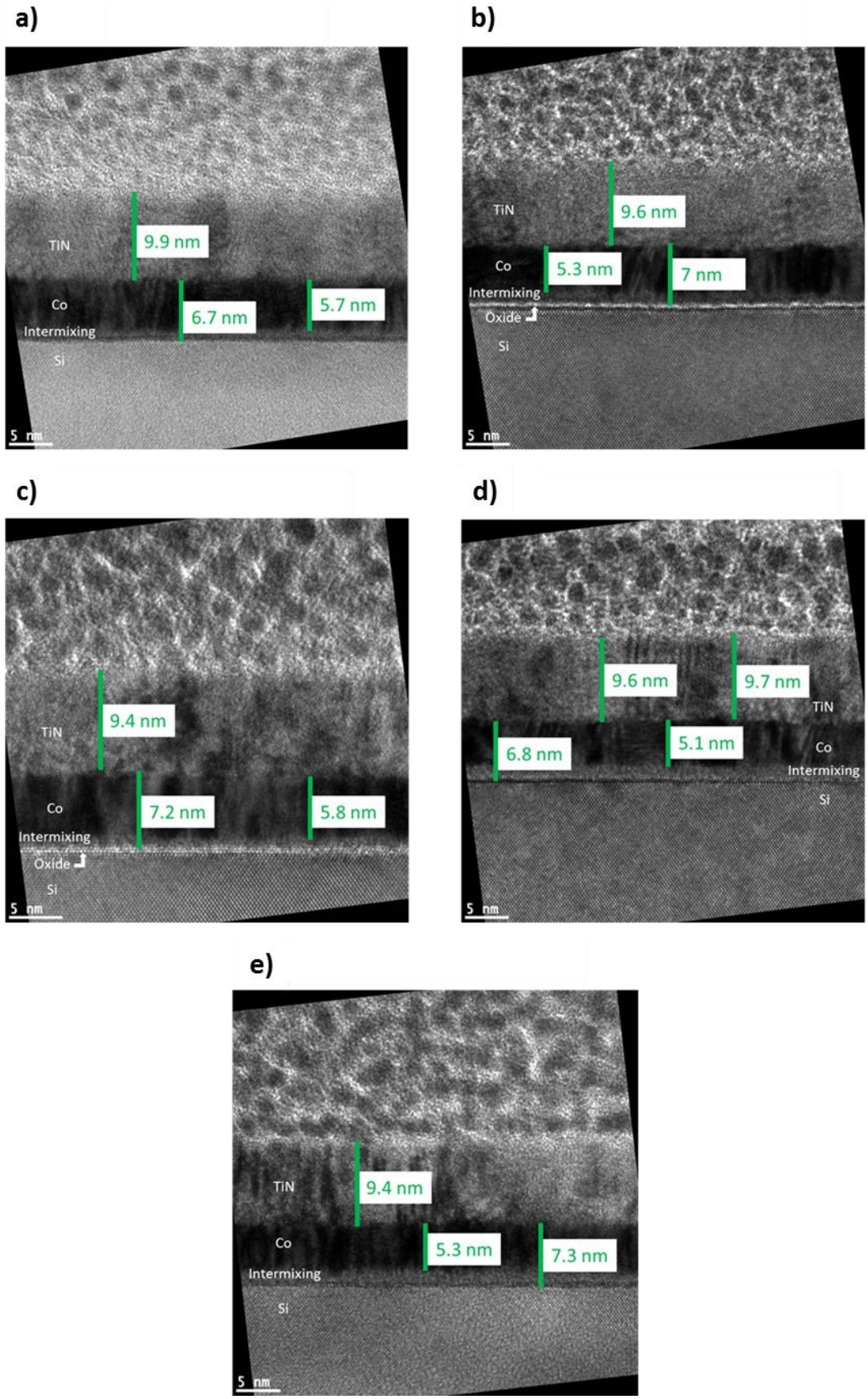

Figure 1: TEM micrographs after the metal deposition by PVD of Co and TiN layers on Si(100) blanket wafers for different surface preparations with a) HF + SC1 + SiCoNi, b) HF + SC1 + SSE12, c) HF + SC1 + SSE7, d) HF + SSE7 and e) HF "only".

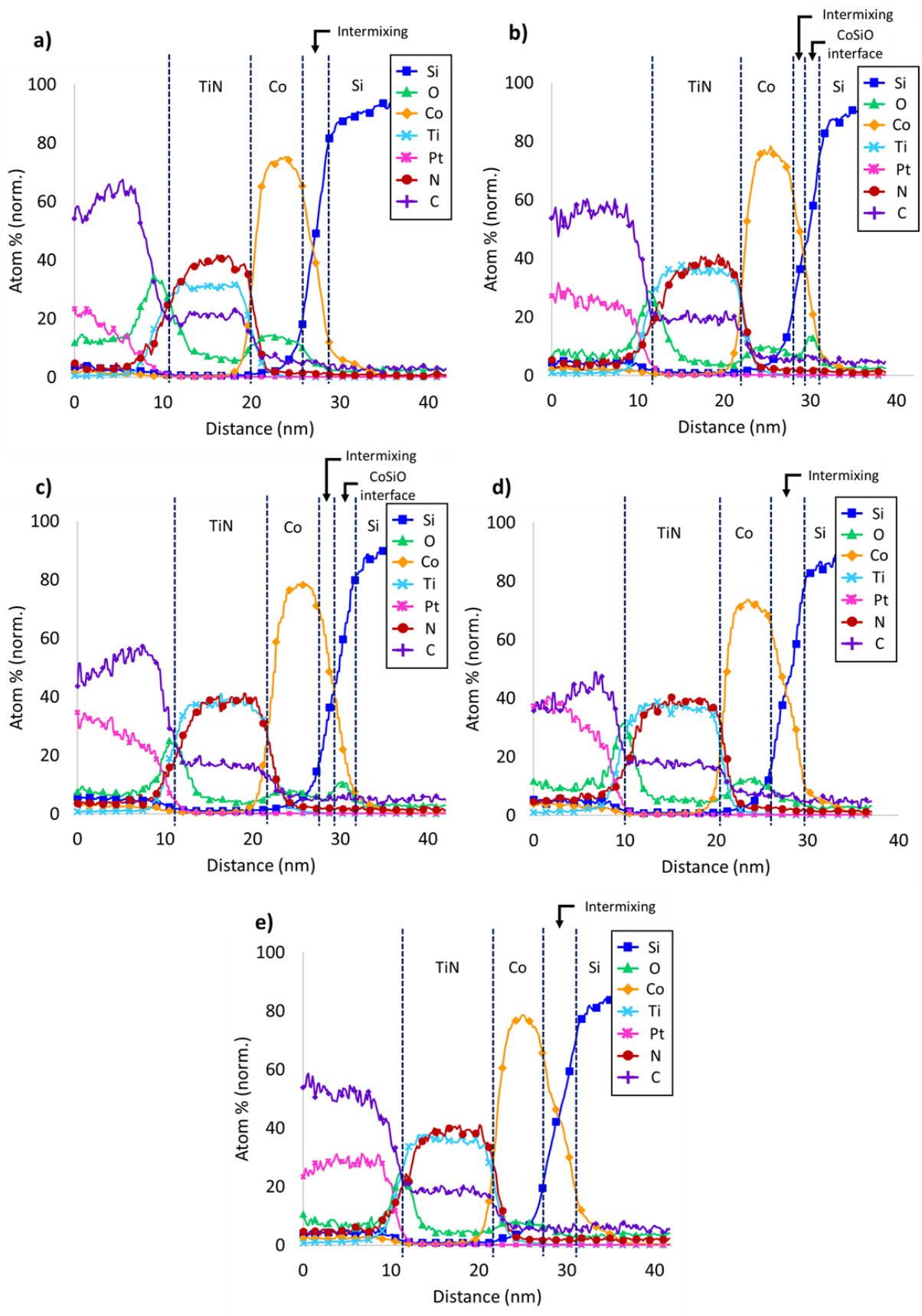

Figure 2: In-depth EDX profiles after the deposition by PVD of Co and TiN layers on Si(100) blanket wafers for different surface preparations with a) HF + SC1 + SiCoNi, b) HF + SC1 + SSE12, c) HF + SC1 + SSE7, d) HF + SSE7 and e) HF "only".

Although its composition is difficult to measure, an intermixing layer is also present for all the surface preparations. As the intermixing usually occurs during the metal deposition performed in this case at 100 °C, the surface preparations do not seem to hinder the intermixing formation. On the contrary, the oxide layer, which appears as a small but well identified O peak, is only observed for samples in the case of SC1 and SSE processes, since it is highly dependent on the surface preparation.

Table 2

Cobalt and oxygen concentrations in the cobalt layer measured by EDX according to the surface preparation applied on Si(100) wafers.

Wafer name	Surface preparation	Co concentration	O concentration
P1	HF + SC1 + SiCoNi	80 at. %	13 at. %
P2	HF + SC1 + SSE12	81 at. %	10 at. %
P3	HF + SC1 + SSE7	85 at. %	7 at. %
P4	HF + SSE7	84 at. %	11 at. %
P5	HF “only”	85 at. %	7 at. %

2. Sheet resistance Rs

To study the phase formation and the agglomeration at high temperatures for the different surface preparations, sheet resistance, Rs, measurements were performed at room temperature on each sample after RTA between 200 and 900 °C.

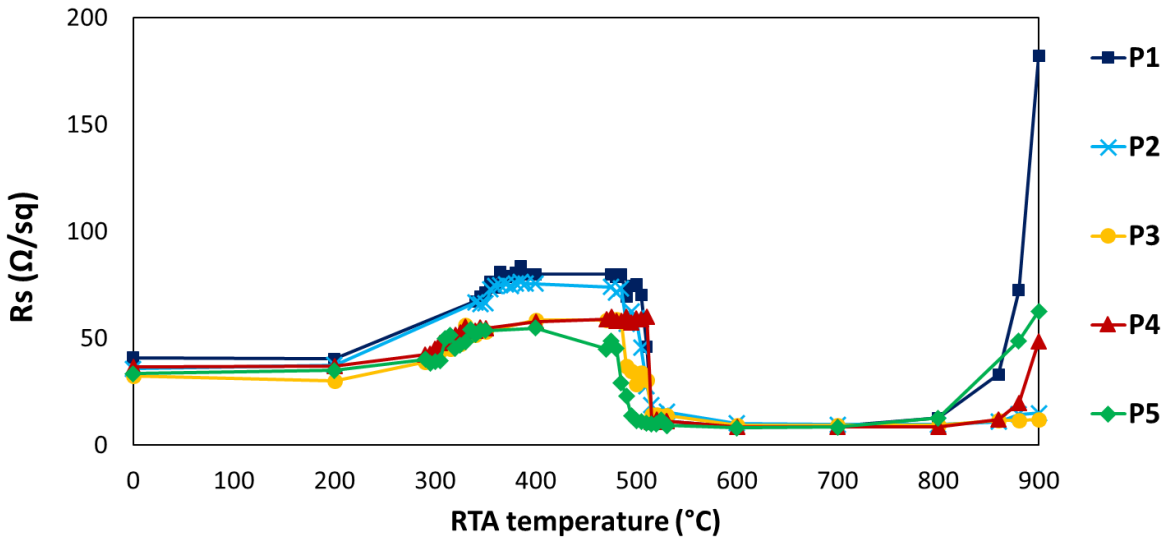

Figure 3: Sheet resistance, Rs, measurements for each surface preparation after RTA between 200 and 900 °C using variable temperature steps depending on the area of interest with P1 = HF + SC1 + SiCoNi, P2 = HF + SC1 + SSE12, P3 = HF + SC1 + SSE7, P4 = HF + SSE7 and P5 = HF “only”.

Figure 3 shows that the evolution of Rs values as a function of applied RTA temperature is similar for the different samples: below 200 °C, the Rs remains stable and then increases gradually when the temperature increases to 400 °C. This variation of Rs might be to the successive formation of Co_2Si (ρ_{Co_2Si} ≈ 110 µΩ.cm) and CoSi (ρ_{CoSi} ≈ 150 µΩ.cm) from the Co film (ρ_{Co} ≈ 30 µΩ.cm) in the temperature range 300 – 400 °C as reported in [42–44]. Then, a plateau is present until a sharp decrease of the Rs happens around 515 °C for the P1 to P4 wafers (respectively HF + SC1 + SiCoNi, HF + SC1 + SSE12, HF + SC1 + SSE7 and HF + SSE7) and around 495 °C for the P5 wafer (HF “only”). This sharp decrease is attributed to the

$CoSi_2$ formation since this phase has a low resistivity (ρ_{CoSi_2} ≈ 20 µΩ.cm) [42–44]. For higher temperatures, a plateau is again observed up to 800 °C. From 800 °C, two behaviors stand out: either the value of Rs remains stable in the case of SC1 + SSE surface preparation or a shFarp Rs increase is seen for other samples. This large increase in Rs value is characteristic of the deterioration of the $CoSi_2$ film by agglomeration.

3. *XRD measurements*

To complete the study on cobalt silicides formation, ex situ XRD measurements were first performed for each surface preparation type after RTA between 100 and 700 °C with a 20 °C step. Figure 4 shows the contour plot of θ-2θ XRD measurements with the angular position in x and the RTA temperature in y. The color represents the intensity of the diffraction peaks with the lowest intensity in blue and the highest intensity in red.

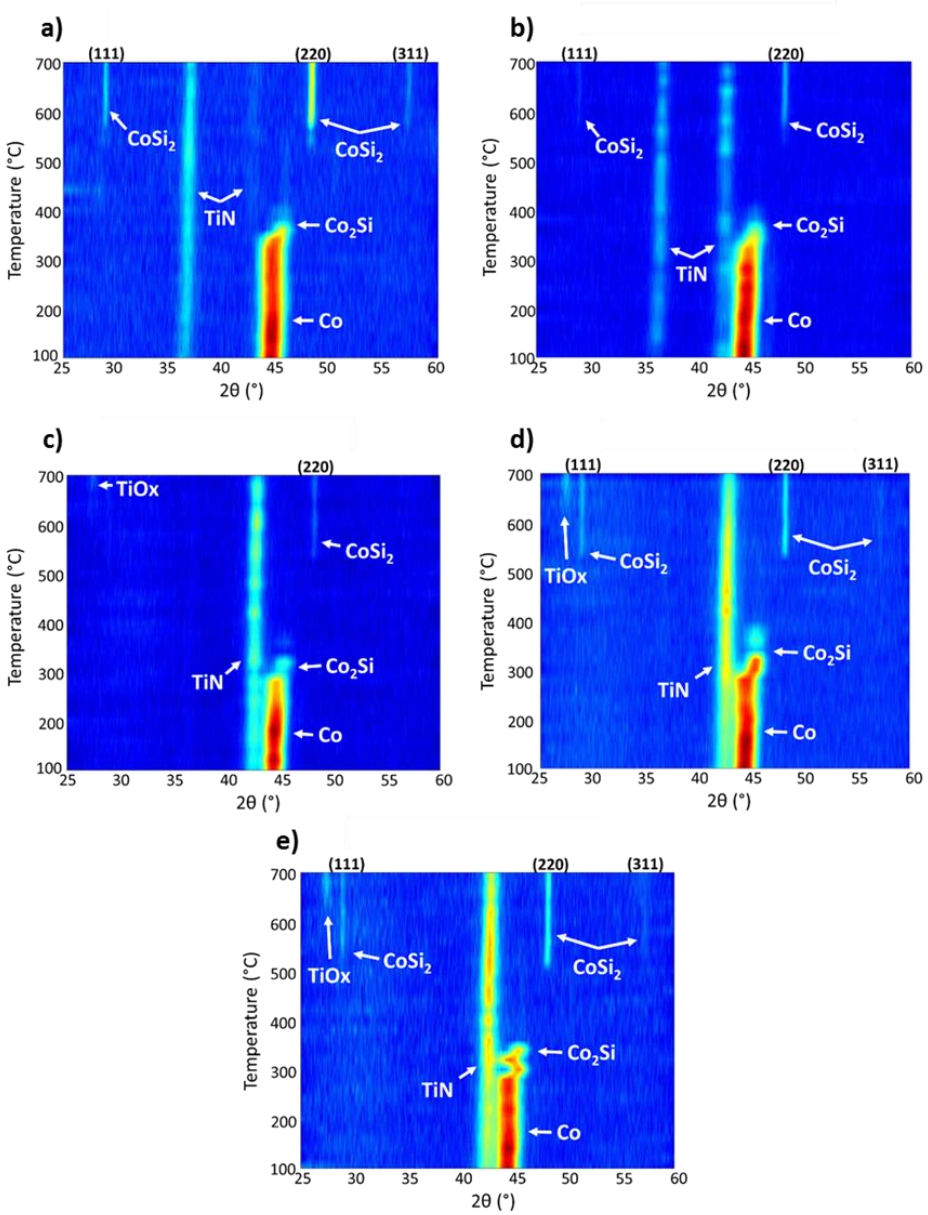

Figure 4: Contour plots of θ-2θ XRD measurements for each surface preparation types with a) HF + SC1 + SiCoNi, b) HF + SC1 + SSE12, c) HF + SC1 + SSE7, d) HF + SSE7 and e) HF "only" after RTA treatments for a temperature between 100 and 700 °C with a 20 °C step. The color represents the diffraction peaks intensity (blue for the least intense, red for the most intense).

In Figure 4, the Co layer is characterized by a peak at 2θ ≈ 44.2 ° and the TiN layer by one or two TiN peaks at 2θ ≈ 36.4 ° and 2θ ≈ 42.6 °. The difference in TiN crystallinity probably comes from the tool used when it was deposited. Thus, only one peak is observed for P1 and P2 wafers (tool 1) while two peaks are observed for P3, P4 and P5 wafers (tool 2). When the temperature increases to about 300 °C, the peak around 44 ° shifts to large angles (2θ ≈ 45.4 °) and this is attributed to the Co_2Si formation. At higher temperature, the formation of $CoSi_2$ is observed with one or more diffraction peaks at 2θ ≈ 28.9 °, 2θ ≈ 48.2 ° and 2θ ≈ 57.3°, depending on the sample. This formation starts at 520 °C for P1 to P4 samples (respectively HF + SC1 + SiCoNi, HF + SC1 + SSE12, HF + SC1 + SSE7 and HF + SSE7) and at 500 °C for P5 sample (HF "only"). Note that, for all samples, there is a temperature range between the disappearance of the Co_2Si peak and the formation of $CoSi_2$ where no diffraction peak assigned to monosilicide can be observed. As indicated by the disappearance of the peak, the Co_2Si phase should have been consumed by the formation of a new phase. According to the Co-Si phase diagram [45] and the previous study [46], this phase should be CoSi.

More precise XRD measurements were also performed on all samples annealed at 700 °C in the θ-2θ range of the $CoSi_2$ phase epitaxy peaks, that is around 33 ° for the (200) crystallographic orientation and 70 ° for the (400) crystallographic orientation. This temperature was selected to observe the presence or absence of epitaxy on a fully formed $CoSi_2$ phase. Only the diffraction peaks around 33 ° are shown in Figure 5 since no epitaxy peaks were found around 70 °. This is certainly due to the very high intensity of the Si substrate peak (2θ ≈ 69.1 °) that hides the (400) $CoSi_2$ peak. The double peak around 33 ° on all XRD measurements corresponds to the (200) peak of the Si substrate: accordingly to the PDF file for Si (00-027-1402), it should not appear but, due to the very good crystallinity of the Si, it is usually observed by XRD with a much lower intensity than the (400) Si peak.

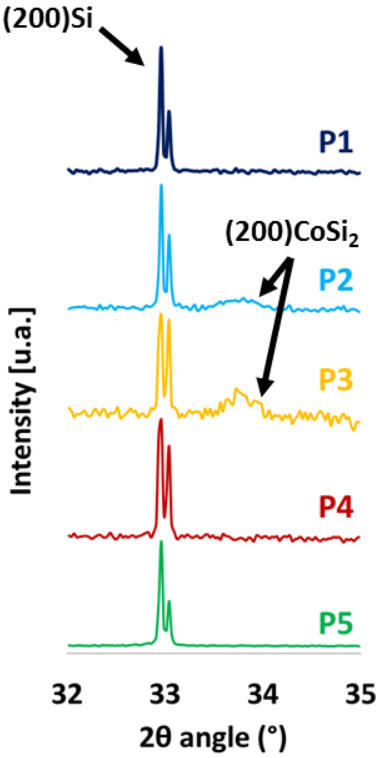

Figure 5: Superposition of XRD measurements around 33 ° for all surface preparations annealed by RTA at 700 °C during 10 min with P1 = HF + SC1 + SiCoNi, P2 = HF + SC1 + SSE12, P3 = HF + SC1 + SSE7, P4 = HF + SSE7 and P5 = HF "only".

For the P2 (HF + SC1 + SSE12) and P3 (HF + SC1 + SSE7) wafers, a peak attributed to the $CoSi_2$ phase in epitaxy is observed ($2\theta = 33.8$ °) while no peak is observed for the other surface preparations. In the $CoSi_2$ PDF file (00-038-1449), the (200) diffraction peak has a very low intensity. Thus, the presence of this peak on Figure 5 proves that this orientation is overrepresented on the P2 and P3 samples. Therefore, these results show the presence of a relatively strong epitaxy only for wafers with a thin oxide layer between the Si substrate and the intermixing layer shown in TEM micrographs (Fig. 1).

4. EBSD

As agglomeration can be related to the crystallographic orientation of grains [47] and in particular to heteroepitaxy in the case of $CoSi_2$, EBSD measurements were performed on two samples typical of the different behaviors regarding agglomeration, i.e. either the Rs is stable at 900 °C (P1: HF + SC1 + SiCoNi) or it increases strongly (P2: HF + SC1 + SSE12), after a complete Salicide brick formation (RTA1 500°C 30 s, selective etch, RTA2 790°C 20 s). However, it was possible to obtain EBSD results (i.e. to identify and to index grains) only for the P2 wafer. Indeed, it seems that the $CoSi_2$ grains on the P1 wafer are too small to be analyzed by EBSD. Consequently, only the EBSD results on the P2 wafer is shown in Figure 6.

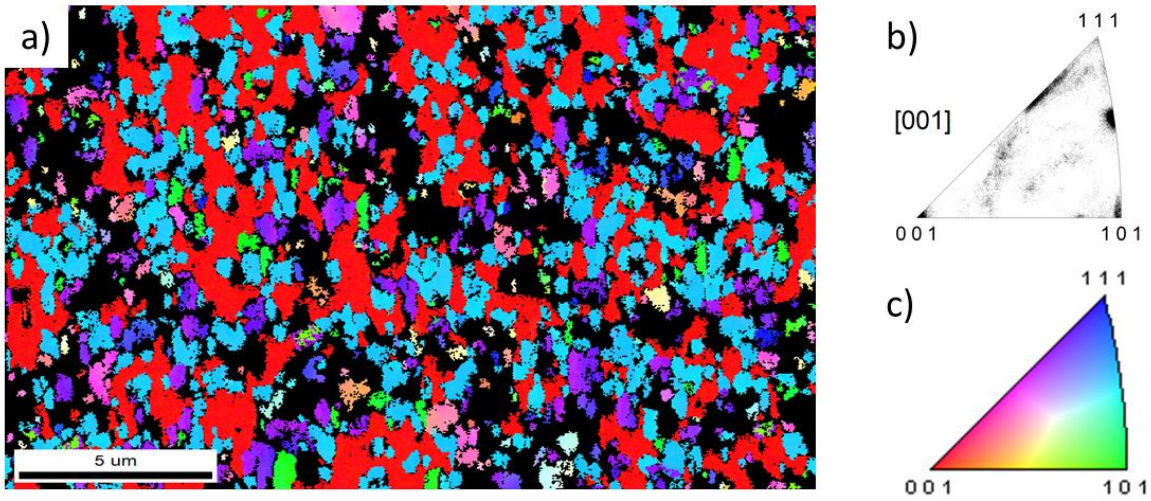

Figure 6: EBSD measurement of the P2 (HF + SC1 + SSE12) sample after a complete Salicide process with a) Orientation map along the normal direction to the sample surface, b) Inverse Pole Figure (IPF) perpendicular to (001) direction and c) the color map

The orientation map of the EBSD measurement (Figure 6.a) shows black areas that correspond to grains too small to be analyzed while the other colored areas correspond to grains that can be indexed. Two preferential grain orientations are predominant, in red and light blue. The red grains correspond to the (001) $CoSi_2$ orientation while the light blue grains correspond to the (212) $CoSi_2$ orientation perpendicular to the sample surface as well as the interface between $CoSi_2$/Si interface. The IPF (Inverse Pole Figure) of the EBSD measurement (Figure 6.b) confirms the predominance of these two orientations and shows also other orientations such as a few green grains with the (101) $CoSi_2$ grains orientation. For a better understanding of the texture, the main crystalline orientations present in the IPF (Fig. 6.b) were represented separately on Figure 7, with the (001) orientation in red, the (212) orientation in light blue, the (101) orientation in green and the other orientations in purple. Thus, the PF was determined for each of these orientations from the selected grains.

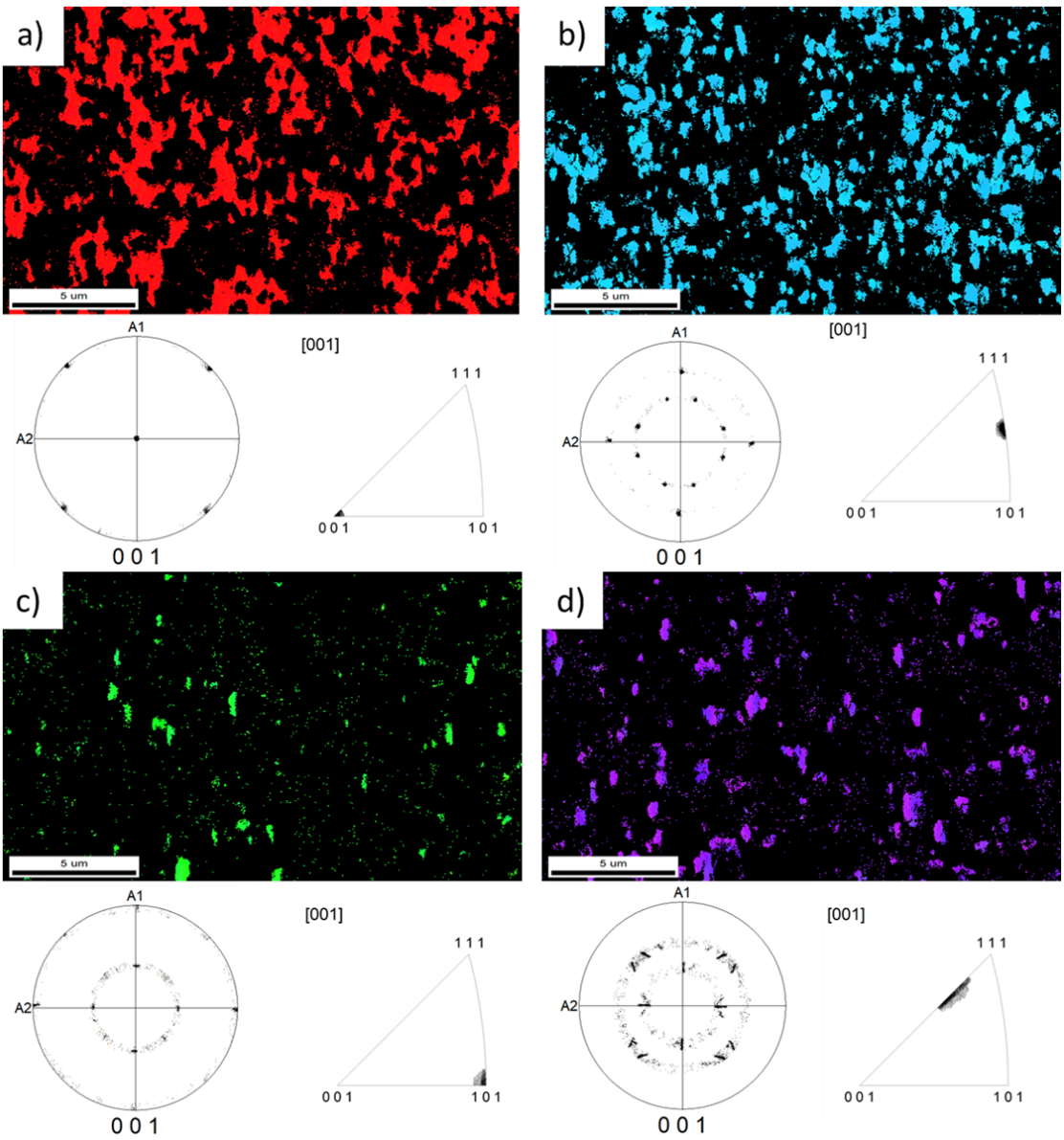

Figure 7: Detailed analysis of the main grain orientations selected from the IPF in Figure 5.b for the P2 (HF + SC1 + SSE12) sample after a complete Salicide process with the orientation map, the IPF and the PF for different crystalline orientations: a) (001), b) (212), c) (101) and d) other orientations.

In Figure7.a and 7.b, the (001) and (212) $CoSi_2$ orientations correspond to the two main orientations since they are predominant in the EBSD measurement. Points are clearly visible on the pole figures, showing the epitaxial relationships. In Figure 7.c corresponding to the (101) $CoSi_2$ orientation, the intensity of the points is much lower since this orientation is clearly less present in this sample along the Si(100) direction as one can observe on EBSD measurement (Fig 6.a). There is still an epitaxial relationship with the substrate, but a ring characteristic of a fiber texture is also present. These three epitaxial relationships, already reported in the literature by De Keyser and al. [27], are expressed in Table 3. The (212) orientation is identical to the (122) orientation in the cubic centered system of perfect cubic symmetry.

Table 3
Epitaxial relationships of $CoSi_2$ on a (001) orientated Si substrate [27].

Texture components	Relationships
Epitaxy A_{001} (red)	With $CoSi_2$(001)//Si(001) and $CoSi_2$(110)//Si(110)
Epitaxy B_{001} (light blue)	With $CoSi_2$(122)//Si(001) and $CoSi_2$(110)//Si(101)
Epitaxy C_{001} (green)	With $CoSi_2$(101)//Si(001) and $CoSi_2$(101)//Si(110)

Figure 7.d is different from Figures 7.a, 7.b and 7.c as it doesn't correspond to an epitaxy relationship but to an axiotaxial relationship reference. Indeed, the pole figure shows lines, not points, which are characteristic of the axiotaxy texture [48]. This was also reported by Özcan and al. [49] and is highlighted in Figure 8 with the off-normal $CoSi_2$ (110) fiber texture (= axiotaxy) with the fiber axis at $\chi = 45°$, $\Phi = 45, 135, 225, 315°$. The (001) Pole Figure image (PF) obtained from EBSD measurements is presented Figure 8.a. Figure 8.b highlights the different types of texture present in the analyzed sample, since epitaxy components are characterized by points while fiber textures including axiotaxy are represented by lines [27].

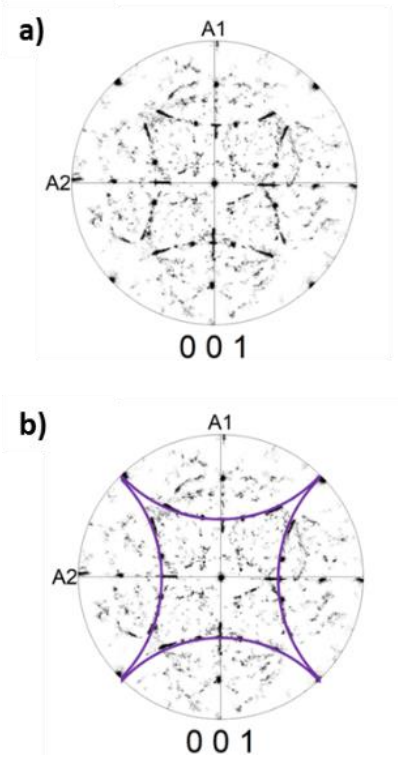

Figure 8: a) Pole figure of the P2 (HF + SC1 + SSE12) sample after a complete Salicide process and b) the same pole figure with the axiotaxy highlighted (off-normal $CoSi_2$(110) fiber texture with the fiber axis at χ = 45°, Φ = 45, 135, 225, 315°).

5. AFM

To check the $CoSi_2$ grains size, AFM measurements were made on the P1 (HF + SC1 + SiCoNi) and P2 (HF + SC1 + SSE12) samples after the complete Salicide process and are shown in Figure 9.

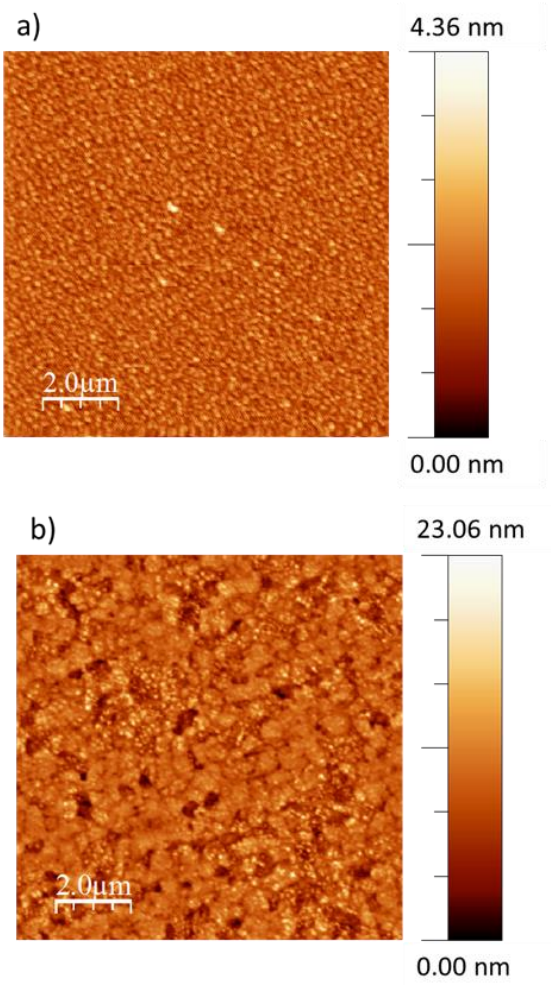

Figure 9: AFM measurements for a) the P2 and b) the P1 samples after a complete Salicide process (RTA1 at 500°C during 30s, selective etch and RTA2 at 790°C during 20s), with a) P1: HF + SC1 + SiCoNi and b) HF + SC1 + SSE12.

Only small grains are visible on the P1 sample (Fig. 9.a) with a size from 35 to 150 nm that appears to be too small to perform EBSD measurement. Figure 9.b shows different grain sizes for P2 sample, with large grains ranging from 300 to 800 nm as well as small ones. This is in accordance with the EBSD measurement (Fig. 6 and 7) in which the large grains have been analyzed while the small ones were not identified due to the resolution limit of the EBSD equipment. In addition, the roughness, calculated using the equation 6, is slightly higher for the P2 sample (Root Mean Square, RMS = 2.48 nm) than for the P1 sample (RMS = 0.44 nm) but remains low.

$$RMS = \sqrt{\frac{1}{L}\int_0^L |(y(x))^2|.dx} \qquad \text{Eq. 6}$$

With L the length of the profile on the x-axis used for measurement and y(x) is the variation of the height from the profile line for each data point.

4. Discussion

Our results, in particular the evolution of Rs as a function of temperature (Fig. 3), show that the different surface preparations have little influence on the Co silicide phase sequence and related formation temperatures ~~Co silicides formation~~ but have a significant effect on the agglomeration phenomena.

Concerning the phase sequence, the XRD measurements (Fig. 4) show a similar behavior for all surface preparations (P1 = HF + SC1 + SiCoNi, P2 = HF + SC1 + SSE12, P3 = HF + SC1 + SSE7, P4 = HF + SSE7 and P5 = HF "only"), with first the formation of Co_2Si followed by CoSi and finally $CoSi_2$. The fact that no diffraction peak is observed for the CoSi phase can be explained in three ways:

- The CoSi phase is amorphous and does not diffract;
- The CoSi phase has a special texture/epitaxy with no plane in diffraction condition for the XRD geometry used in this study;
- Due to the small thickness, the diffraction volume is too small compared to the XRD sensibility, so no peak is observed.

To determine which hypothesis is most likely, the same ex situ XRD measurements were performed for two wafers with an initial Co thickness of 15 nm after RTA between 100 and 700°C with a 20 °C step (not shown here). One of these wafers has the same surface preparation as P1, i.e. HF + SC1 + SiCoNi, and the other has the same surface preparation as P5, i.e. HF "only". The phase sequence is similar to Figure 4 and the same XRD peaks for TiN, Co, Co_2Si and $CoSi_2$ peaks were observed. In addition, low intensity XRD peaks at $2\theta \approx 45.6°$ and $2\theta \approx 50.3°$ corresponding to the CoSi phase were also observed between 400 and 500 °C. With an initial Co thickness of 15 nm, the CoSi phase is therefore polycrystalline, which excludes an amorphous phase or a specific texture orientation. Moreover, the lattice mismatch between CoSi (a_{CoSi} = 0.447 nm) and Si (a_{Si} = 0.5431 nm) is too important, around 17.7 %, to obtain the epitaxy of CoSi on the Si substrate. As the intensity of CoSi peaks is already very low for 15 nm of Co, it is possible that for 7.5 nm as initial Co thickness, the diffraction peaks are not intense enough to be measured.

The nature of silicide may also be determined by the intrinsic resistivity value which is characteristic of a given phase (Table 4). The Rs of a stack of layers is equal to:

$$\frac{1}{Rs^{tot}} = \sum_i \frac{1}{Rs_i} = \frac{1}{Rs^{TiN}} + \frac{1}{Rs^{Co-based\ layers}} \quad \text{Eq. 7}$$

$$\frac{1}{Rs^{tot}} = \sum_i \frac{L_i}{\rho_i} = \frac{L^{TiN}}{\rho^{TiN}} + \sum_j \frac{L^{Co-based\ layers}}{\rho^{Co-based\ layers}} \quad \text{Eq. 8}$$

with ρ_i the resistivity and L_i the thickness of each layer. In our sample, the film is constituted of at least two layers: i.e. the silicide and the TiN layers.

If the TiN resistance is constant for all the temperature range, the presence of a Rs plateau from approximately 400 °C to 480 °C (Fig. 3) indicates that a single silicide is present in this temperature range. However, there is a difference of the Rs values of this plateau for the different samples with two types of values around 60 and 75 Ω/square. In fact, these two types of values correspond to samples that were made in the two different tools. These tools are known to give TiN with different resistivity (see Part 2. Experiments details) and this may explain the two types of plateau values.

To confirm this hypothesis, the TiN contribution has been removed from the measured Rs for each surface preparation types to obtain the Rs of Co-based layers (Eq. 7) and the resistivity of the different phases are reported in Table 4.

Table 4

Resistivity values found in the literature [42–44] and modified resistivities of cobalt silicides and TiN

Phase	Resistivity values found in the literature (µOhm.cm)	Modified resistivity of P1 and P2 wafers (µOhm.cm)	Modified resistivity of P3, P4 and P5 wafers (µOhm.cm)
TiN	10 – 10 000	209	174
Co	30	32	32
Co_2Si	70 – 110	105	76
CoSi	100 – 150	163	119
$CoSi_2$	14 – 25	23	23

The TiN Rs is calculated with L(TiN) = 14 nm and $\rho_{TiN\ (tool1)}$ = 209 µOhm.cm for P1 and P2 wafers and with $\rho_{TiN\ (tool2)}$ = 174 µOhm.cm for P3, P4 and P5 wafers. For the different cobalt silicide, the resistivity values are within the range of the value reported in the literature [42–44] except for the CoSi for Tool 1, that is slightly above the maximum reported value. The difference in CoSi resistivity may come from a difference in grain size, impurity content and/or roughness.

Therefore, in our samples, the phase sequence obtained for all samples is a-$Co_{1-x}Si_x$ ➔ Co_2Si ➔ CoSi ➔ $CoSi_2$, whether there is an oxide layer between the Si substrate and the intermixing layer or not (Fig. 1).

As the SC1 ($NH_4OH/H_2O_2/H_2O$) surface preparation leads to the formation of a thin oxide layer of 1.4 nm at the Si surface, it can be considered as an OME (Oxide Mediated Epitaxy) process even if the SSE process etched a part of this layer in our samples.

However, when the formation of Co silicides occurs through an oxide layer (OME process,), the phase sequence can be modified: the Co_2Si and/or CoSi phases may not be observed. On one hand, in most articles [17–19], only the $CoSi_2$ phase is observed for an oxide layer formed from a $HCl/H_2O_2/H_2O$ solution (Shiraki oxides) with a thickness of about 2 nm. The same results was obtained by Tung [17] for an oxide layer grown by submerging the Si substrates in a hot (90 °C) $NH_4OH/H_2O_2/H_2O$ solution for 20 min. Chang and al. [20] have also only observed the $CoSi_2$ phase, but the $CoSi_2$ layer is thicker for a very thin oxide layer (0.8 nm) than for a 2 nm oxide formed by immersion into a hydrogen peroxide solution (H_2O_2). They conclude that Co diffuses more easily through a finer oxide layer. On the other hand, Heo and al. [21] report the formation of the Co_2Si phase before the $CoSi_2$ formation for an oxide layer with the same thickness that Tung [17] but formed by submerging the Si substrates into a H_2O_2 solution for 10 min.

A similar phase sequence change has been also reported with the TIME process (Titanium Interlayer Mediated Epitaxy) since only the $CoSi_2$ phase was observed by Ogawa and al. [50]. However, for Cardenas and al. [51] as well as Falke and al. [31], the CoSi phase is observed before the $CoSi_2$ formation and other works [34,52] mention a classical phase sequence (Co_2Si, CoSi, $CoSi_2$) despite the presence of a Ti intermediate layer between the Si substrate and the Co layer. Therefore, for the TIME process, a phase sequence change is not always observed.

However, our results do not show a phase sequence change in contrast to other studies [17–21]. This difference may be due to the way the oxide is grown and/or to its thickness. The influence of the oxide composition and its thickness on the Co silicides growth has already been mentioned by Tung [17]. He explains that a SiOx oxide layer with x < 2 and a thickness between 0.5 and 1.5 nm is likely to be more suitable for the OME effect since a 2 nm SiO_2 stoichiometric layer leads to a non-uniform and poor epitaxial $CoSi_2$ layer. Given that the initial small thickness of Co used in the studies in which only $CoSi_2$ is observed (about 2 nm for Tung [17] and Kleinschmit and al. [18], 4 nm for Chang and al. [19]), the thickness of the first formed silicides may be too low to be detected while for the 10 nm Co in Heo and Jeon [21], the Co_2Si formation has been observed before $CoSi_2$. Concerning the TIME process, the initial thickness of Co is usually much higher (15 nm for Ogawa and al. [50], 20 nm for Cardenas and al. [51] and Hong and al. [34], 20 to 30 nm for Falke and al. [31] and Wei and al. [52]), the phase sequence change could have been more easily observed.

Therefore, the similar phase sequence observed for our samples with or without an oxide layer contrasts with previous studies and could be due to the combination of the way the oxide is made (SC1 + SSE) as well as the thin oxide layer thickness (0.7 nm for the P2 wafer and 0.8 nm for the P3 wafer).

In addition to change in phase sequence, it was also reported that the presence of an intermediate layer (SiOx or Ti) can change the formation temperature of the $CoSi_2$ phase. However, in our samples, the XRD measurement (Fig. 4) show that the $CoSi_2$ formation temperature is the same for P1 to P4 wafers (520 °C) irrespectively to the presence of an oxide layer and is only slightly lower for P5 wafer (500 °C) with HF cleaning. Similar results were obtained with the Rs measurements (Fig. 3) since the Rs drop attributed to the $CoSi_2$ formation are close to the formation temperatures obtained by XRD, that is 515 °C for P1 to P4 wafers and 495 °C for P5 wafer. So, our results show that surface preparation has little influence on the formation temperature of the $CoSi_2$ phase with nevertheless a slight decrease for HF surface preparation only. These results contrast with former works [17,18,20].

Indeed, for a SiOx intermediate layer, Tung [17] obtains the $CoSi_2$ phase at 600 °C without oxide layer and at 460 °C with a 2 nm oxide layer. However, $CoSi_2$ is discontinuous at low temperatures, and it is necessary to reach 550 °C to obtain an almost perfectly continuous $CoSi_2$ layer. A lower $CoSi_2$ formation temperature was also observed by Chang and al. [20] with an oxide layer (500 – 700 °C) than without an oxide layer (> 750 °C). Kleinschmit and al. [18] observe that the $CoSi_2$ phase forms completely at a lower temperature without an oxide layer than with an oxide layer. Therefore, the $CoSi_2$ phase forms at lower temperature with an oxide layer than without an oxide layer but takes longer to form completely.

In the case of a Ti intermediate layer, Ogawa and al. [53] annealed and compared samples with 1, 2 or 5 nm of Ti and 15 nm of Co on Si(100) to samples without Ti and the same heat treatment. With a Ti layer, only the $CoSi_2$ phase is observed from 400 °C while without this layer, the $CoSi_2$ forms from 450 °C. However, the $CoSi_2$ phase is completely formed at 600 °C without a Ti layer and at 800 °C with a Ti layer. A delay in the end of $CoSi_2$ formation is also observed by Cabral and al. [54] which shown the $CoSi_2$ formation ends at 640 °C without a Ti layer and at 715 °C with 2 nm of Ti. However, contrary to Ogawa and al. [53], Detavernier and al. [55] show the $CoSi_2$ formation at higher temperature with a Ti layer than without a Ti layer, and this even for a very low Ti thickness of 0.1 nm. This result was also observed by Yang and Bene [56] as well as Barmak and al. [57]. Thus, whether it is an interlayer of SiOx or Ti, the $CoSi_2$ phase takes longer to form completely and forms at a different temperature (lower or higher with an intermediate layer).

However, these results do not match with our XRD and Rs measurements since $CoSi_2$ is formed at the same temperature for P1 to P4 wafers, whether there is an oxide layer or not. There also does not appear to be any difference in formation kinetics depending on the surface preparation since, once $CoSi_2$ is formed, the Rs remains stable around 10 Ω/square for all samples up to 800 °C which means there is no change in thickness (this is also confirmed by the constant and maximum intensity of the XRD peaks in Fig. 4). It is communally argued that SiOx (or Ti) acts as a Co diffusion barrier during the early stages of the Co-Si reaction in the literature [15,16,49,52,53] and this should lead to a delay in silicide formation. As detailed before for the phase sequence, our similar temperatures of $CoSi_2$ formation could be due to the combination of production method (SC1 solution) as well as the thin oxide layer thickness (0.7 nm and 0.8 nm for the P2 and P3 wafers respectively). The difference between our results and those of the literature may depend on other parameters such as layer thicknesses (Co, SiOx, Ti), the presence of a capping layer or the applied thermal annealing. Concerning the slight difference in formation temperature for the P5 wafer, the HF surface preparation allows to obtain F terminated surface that is efficient to avoid oxidation so, as explained above, the presence of a Si oxide is known to slow down the formation of the silicide so the efficiency of the HF preparation should decrease the silicide formation temperature.

Nevertheless, in our case, although the presence of oxide does not affect the formation of $CoSi_2$, it does affect thermal stability. Indeed, in Figure 3, the agglomeration of the layer is observed for samples without oxide (P1, P4 and P5) while the values of Rs remain stable for wafers if an oxide is at the interface between intermixing layer and Si prior silicide formation (P2 and P3). In the literature, agglomeration is generally found at lower temperatures for large grains than for small grains experimentally [58], in accordance with theoretical models [22,47]. Indeed, several models [47] based on the equilibrium shape due to interfacial energies have shown that, for a given thickness, there is a critical grain size above which agglomeration will occur. In particular, a model was proposed by Srolovitz and Safran [59] considering an idealized 2D grain structure. In the case of a polycrystalline film, an energy balance at the intersection of the grain boundary and the film surface is given by:

$$2\gamma_f \sin\varphi = \gamma_{gb} \quad \text{Eq. 9}$$

with γ_f the isotropic surface, φ the groove angle and γ_{gb} the grain boundary. This energy balance leads to a curved surface with a groove depth δ at the grain boundary given by:

$$\delta = R\frac{2-3\cos\varphi+\cos^3\varphi}{3\sin^3\varphi} \quad \text{Eq. 10}$$

When the groove depth becomes larger than the thickness of the film, h, a hole can be formed where the groove contacts the surface which is the first stage of the agglomeration. Thus, a critical grain size R_C could be determined by:

$$R_C = h\frac{3\sin^3\varphi}{2-3\cos\varphi+\cos^3\varphi} \quad \text{Eq. 11}$$

Therefore, Eq. 11 states that the agglomeration can be avoided if the grain size is smaller than this critical value and it is why the agglomeration is generally found at lower temperatures for large grains than for small grains. However, in our case, the agglomeration of the $CoSi_2$ film occurs for the P1 wafer and not for the P2 wafer (Fig. 3) while the AFM measurements (Fig. 9) show smaller grains for the P1 wafer (35 to 150 nm) than for the P2 wafer (300 to 800 nm) after a complete Salicide process. Thus, these results contrast with the models described above. This difference can be explained by the texture of $CoSi_2$ since the heteroepitaxy of the $CoSi_2$ grains with the Si substrate may strongly influence the

agglomeration [39,40]. Indeed, it has already been reported that the growth of cobalt silicides through an oxide layer leads to a $CoSi_2$ layer in epitaxy with the Si(100) (OME process) [17,18,38]. In our samples, the presence of epitaxy is confirmed in the P2 (HF + SC1 + SSE12) wafer with the growth of the Co silicides through an oxide layer unlike the P1 (HF + SC1 + SiCoNi) wafer with the growth of the Co silicides directly on the Si substrate by XRD (Fig. 5). Furthermore, our EBSD measurements (Fig. 6) show that the percentage of epitaxy in the P2 wafer is very important. Indeed, if we calculate the proportion of epitaxy orientations compared to other orientations without considering the non-indexed grains, that is the proportion of red, light blue and green in the EBSD measurement (Fig. 6.a) compared to the other colors, a percentage of 75.5 % of grains in epitaxy with the substrate has been found.

As a result, the agglomeration of the $CoSi_2$ film occurs at a lower temperature for the P1 wafer than for the P2 wafer (Fig. 10) despite a smaller grain size for P1. Moreover, the influence of epitaxy on thermal stability is also found in other wafers. Indeed, Figure 5 shows the presence of epitaxy only for wafers with a thin oxide layer between the Si substrate and the intermixing layer (P2 and P3) while Figure 3 shows the agglomeration for wafers without this oxide layer (P1, P4 and P5). Thus, it is confirmed that the presence of an oxide layer leads to the epitaxy of the $CoSi_2$ layer that provides a better thermal stability.

In our samples, the epitaxy is favored even if the oxide layer is very thin. Several explanations for this epitaxial growth through an oxide layer have been reported in the literature. Tung [17] argues that since the role of SiOx in the OME process is analogous to that of Ti in the TIME process, the intermediate layer (Ti or SiOx) acts as a diffusion barrier, delaying the Co-Si reaction until the temperature exceeds 500 °C and allowing the $CoSi_2$ formation in epitaxy. He also suggests that, since $CoSi_2$ growth was not prevented by oxygen from the SiOx layer, Co diffuses through the SiOx layer and reacts directly with the substrate. This role of diffusion barrier played by the SiOx layer is also mentioned by Sakamoto and al. [38] which express two important points for the $CoSi_2$ formation in epitaxy. This requires (i) a reaction barrier that suppresses the Co/Si reaction until the temperature is high enough to directly form $CoSi_2$ by skipping Co-rich phases and (ii) a kinematic barrier to suppress surface migration which delays the development of holes and islands to preserve a uniform and flat $CoSi_2$ layer in epitaxy. Another explanation is reported by Detavernier and al. [55,60] to explain both the difference in nucleation temperature and the preferential orientation of grains in the case of an intermediate layer (Ti, Ta, W…). It is based on the classical theory of heterogeneous nucleation in which the activation energy for nucleation ΔG^*, is:

$$\Delta G^* \approx \frac{(\Delta\sigma)^3}{(\Delta H - T\Delta S)^2} + Q \qquad \text{Eq. 12}$$

With $\Delta\sigma$ the interfacial energy difference before and after the $CoSi_2$ nucleation, ΔH the formation enthalpy, T the temperature and ΔS the entropy. Q is the kinetic term representing the activation energy for the local atomic rearrangement needed to form the nucleus.

The interfacial energy difference during the formation of a $CoSi_2$ nucleus can be expressed by:

$$\Delta\sigma = \sigma_{CoSi_2/Si} + \sigma_{CoSi_2/CoSi} - \sigma_{CoSi/Si} - \sigma_{CoSi/CoSi} \qquad \text{Eq. 13}$$

With $\sigma_{CoSi_2/Si}$ the interfacial energy of $CoSi_2$ and Si, $\sigma_{CoSi_2/CoSi}$ the interfacial energy of $CoSi_2$ and CoSi, $\sigma_{CoSi/Si}$ the interfacial energy of CoSi and Si, and $\sigma_{CoSi/CoSi}$ the CoSi grain boundary energy.

Detavernier and al. [55,60] report that, since Ti is not soluble in CoSi and $CoSi_2$, it will be present at grain boundaries and interfaces so $\sigma_{CoSi/CoSi}$ may decrease which will cause the

increase of $\Delta\sigma$. The increase in $\Delta\sigma$ will therefore increase ΔG^*, the nucleation barrier and may lead to an increase in nucleation temperature. However, it can also induce the preferential nucleation of $CoSi_2$ grains in epitaxy since these grains will have the lowest nucleation barrier ($\Delta G^*_{epitaxy} < \Delta G^*_{random}$). Another effect of the presence of impurity (Ti, Ta, W…) at grain boundaries and interfaces can be the increase of Q by slowing down the diffusion grain boundary and/or interface that should lead to an increase of the $CoSi_2$ nucleation temperature. As reported above, delaying the Co-Si reaction to higher temperature should then allow a better epitaxy formation of $CoSi_2$. Thus, they conclude that the slow down grain boundary diffusion and/or enhance interfacial cohesion caused by the presence of impurities in the CoSi increase the nucleation temperature and enhance the epitaxy of $CoSi_2$ according to the heterogeneous nucleation theory.

This hypothesis can explain the increase in epitaxial $CoSi_2$ in our sample (Fig. 6.a) with the presence of an SiOx interlayer. Indeed, the oxygen segregation at grain boundaries interfaces can allow a lower Co flow and thus promotes the epitaxial growth of $CoSi_2$. However, in our case, the nucleation temperature increase of $CoSi_2$ is not observed.

In the literature, it is sometimes argued that a small CoSi grain size can decrease the nucleation temperature of $CoSi_2$. We tried to measure the CoSi grain size using EBSD, but it was too small. Moreover, the grain size of $CoSi_2$ is larger for sample with an oxide layer (Figure 9.b) for which this effect might be effective. This large grain size of $CoSi_2$ should come from a larger grain size of CoSi (larger distance between two nucleation sites). Thus, it seems that the CoSi grain size is not at the origin of the similar nucleation temperature for all the samples.

Therefore, we suppose that for the epitaxial grains, $\sigma_{CoSi_2/Si}$ may decrease and can compensate the $\sigma_{CoSi/CoSi}$ decrease. This compensation could lead to the same formation temperature, whether there is an oxide layer or not as observed for our samples. As a result, growth through a thin oxide layer improves the epitaxial quality of $CoSi_2$ and thus improves its thermal stability despite a bigger grain size.

5. Conclusion

Cobalt silicide-based contacts are interesting in some 65 nm technology devices, such as flash memory and advanced imaging technologies, despite a more difficult formation in small dimensions. To promote the formation of $CoSi_2$ in 65 nm technologies, it is possible to play with the surface preparation of the silicon substrate before the metal deposition. In this study, the influence of ~~the~~ different surface preparations on the cobalt silicides formation as well as on the agglomeration was analyzed using XRD, four-point probes measurement, EBSD, AFM and TEM-EDX.

Our results show that the different surface preparations have little influence on the Co silicides formation but have a significant effect on the agglomeration. Indeed, the same phase sequence:

$$a - Co_{1-x}Si_x \rightarrow Co_2Si \rightarrow CoSi \rightarrow CoSi_2 \qquad \text{Eq. 1}$$

was observed for all the surface preparations whether there is an oxide layer or not. In addition, the $CoSi_2$ formation temperature is the same (515 – 520 °C) irrespectively to the presence of an oxide layer, except for the HF cleaning which is slightly lower (495 – 500 °C) while no delay in silicide formation was observed whatever the surface preparation. This result contrasts with the previous studies and could be due to the combination of the way the oxide is made (SC1

solution) as well as the thin oxide layer thickness (0.7 nm for the P2 wafer and 0.8 nm for the P3 wafer).

Nevertheless, although the presence of oxide does not affect the formation of $CoSi_2$ in our case, it does affect thermal stability as we can see with the evolution of Rs as a function of RTA temperature. Indeed, the agglomeration of the $CoSi_2$ layer is observed for wafers without oxide while the thermal stability of wafers with oxide is improved. This result can be explained by the improvement of the epitaxial quality of $CoSi_2$ with the cobalt silicide formation through an oxide layer despite a bigger grain size. This behavior is very interesting for devices applications since the epitaxy is favored for a same thermal budget and a same phase sequence which would be compatible with the Salicide process currently used in the microelectronics industry.

Author contributions

Andrea Newman: Writing - original draft, Conceptualization, Methodology, Investigation, Andrea Campos: Investigation, David Pujol: Investigation, Resources, Pascal Fornara : Conceptualization, Resources, Supervision, Magali Gregoire: Writing - review & editing, Funding acquisition, Conceptualization, Methodology, Resources, Supervision, Dominique Mangelinck: Writing - review & editing, Funding acquisition, Conceptualization, Methodology, Supervision.

Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

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