Characterization of 3.3 kV Discrete SiC MOSFETs in Synchronous Rectification Mode for PV Current Source Inverter Applications

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Abstract

With the newest $3.3\,\mathrm{kV}$ discrete SiC MOSFET being released, Current Source Inverters (CSI) are able to be adapted to $1.5\,\mathrm{kV_{OC}}$ PV strings and substitute actual voltage source-based conversion systems. In order to characterize the switching performances of these new devices, a Double-Pulse Test (DPT) circuit has been developed. The tested switching cell is based on $3.3\,\mathrm{kV}$ / $120\,\mathrm{m\Omega}$ TO-263-7 discrete MOSFETs using synchronous rectification mode. This configuration implies some challenges and introduces extra body diode reverse recovery losses. This paper discusses the main choices, methods, issues and results concerning the switching event for future CSI using $3.3\,\mathrm{kV}$ SiC MOSFETs.

1 Introduction

1.1 Current Source Inverter in photovoltaic conversion system

Concerning photovoltaic (PV) conversion system, many configurations exist. Nowadays, at least half of the PV worldwide power plants [1] employ string (or multi-string) inverter topology. For this configuration, a DC-DC Boost followed by a three-phase Voltage Source Inverter (VSI) is mainly used (Fig. 1).

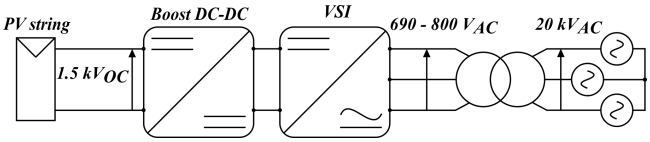

Fig. 1: Boost DC-DC + VSI for $1.5\,\mathrm{kV_{OC}}$ PV string.

Some drawbacks still remain as short lifetime capacitors [2] and multistage conversion system. Furthermore, actual PV systems require a voltage conversion from $1.5\,\mathrm{kV_{OC}}$ to 690 or $800\,\mathrm{V_{AC}}$ delivered to the grid. Due to both limited AC voltage and high number of converters (and then AC cables and connections over long distances) in PV power plants, this configuration presents relatively high AC cabling losses.

A relevant alternative solution would be to use a single or paralleled CSI compared to DC-DC+VSI for $1.5\,\mathrm{kV_{OC}}$ PV strings [3] [4]. In spite of such topology, actual CSI using $1.7\,\mathrm{kV}$ SiC (Fig. 2) devices is not adapted to $1.5\,\mathrm{kV_{OC}}$ PV strings due to CSI voltage step-up conversion characteristic.

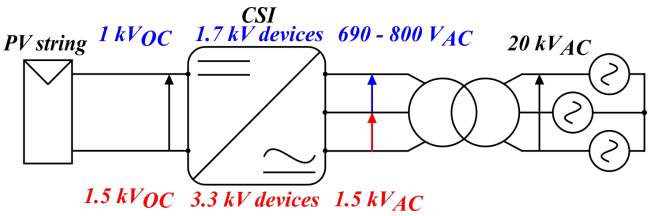

Fig. 2: CSI based on $1.7\,\mathrm{kV}$ devices for $1\,\mathrm{kV_{OC}}$ (blue) and on $3.3\,\mathrm{kV}$ devices for $1.5\,\mathrm{kV_{OC}}$ (red) PV string.

Equation (1) describes the CSI voltage conversion where V_{DC} is the PV string voltage, $\hat{V}_{l-l}$ corresponds to output AC peak voltage (and then MOSFET maximum blocking voltage), M is the modulation index (between 0 and 1) and with φ being the displacement power factor angle.

$$V_{DC} = \frac{\sqrt{3}}{2} \cdot \hat{V}_{l-l} \cdot M \cdot cos(\varphi) \qquad (1)$$

Thus, for a $1.5\,\mathrm{kV_{OC}}$ string voltage, $\hat{V}_{l-l}$ exceeds $1.7\,\mathrm{kV}$ MOSFET voltage limitation. To tackle with this voltage limitation, a solution consists in using new $3.3\,\mathrm{kV}$ SiC MOSFET devices in discrete or module packages and therefore unlocks the use of CSI for $1.5\,\mathrm{kV_{OC}}$ PV strings.

Again, thanks to CSI boost conversion, an AC voltage as $1.5\,\mathrm{kV_{AC}}$ could be delivered to the grid and then reducing AC cabling losses compared to 690 or $800\,\mathrm{V_{AC}}$ grid voltage, while employing a single-stage converter topology.

Figure 3 summarizes this important modification of PV conversion system. This paper proposes a characterization of $3.3\,\mathrm{kV}$ discrete SiC MOSFET, based on DPT method, in order to evaluate switching energies (MOSFET + body diode) for a CSI-based PV conversion system.

1.2 Proposed CSI configuration

The proposed CSI operates in a synchronous rectification mode. The topology is shown in Fig. 3. Two GeneSiC $3.3\,\mathrm{kV}/120\,\mathrm{m\Omega}$ SiC MOSFET (G2R120MT33J) are set in common source anti-series. The aim is to reduce conduction losses, by using MOSFET channel instead of body diodes.

The only function of anti-series MOSFETs' ($\mathrm{D_{P(1,2,3)}}$ and $\mathrm{D_{N(1,2,3)}}$) body diodes is to satisfy bidirectional voltage requirement, which produces recovery losses, normally avoided when using dedicated Schottky diodes. Synchronous rectification mode challenges are exposed in [5] and [6].

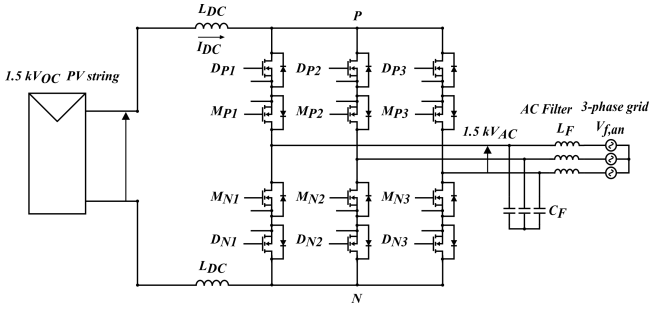

Fig. 3: CSI for 1.5 $\mathrm{kV_{OC}}$ PV string using synchronous rectification mode.

In order to estimate future CSI performances with new $3.3\,\mathrm{kV}$ SiC MOSFET devices, the switching event needs to be investigated.

2 Switching characterization board and protocol

This section is intended to detail the switching cell main features and the protocol that has been established in order to characterize the switching behaviour of $3.3\,\mathrm{kV}$ SiC MOSFET.

2.1 Characterization protocol

The switching losses characterization setup is based on a classic DPT circuit as depicted in Fig. 4. During tests, LS-M (Low-Side MOSFET) is the switching device (DUT - $\mathrm{V_{GS_{LS-M}}} = -5$ or $20\,\mathrm{V}$), HS-D (High-Side Diode) and LS-D are turned off (respectively applying $\mathrm{V_{GS_{HS-D}}} = 0\,\mathrm{V}$ and $\mathrm{V_{GS_{LS-D}}} = -5\,\mathrm{V}$) and HS-M is turned on ($\mathrm{V_{GS_{HS-M}}} = 20\,\mathrm{V}$).

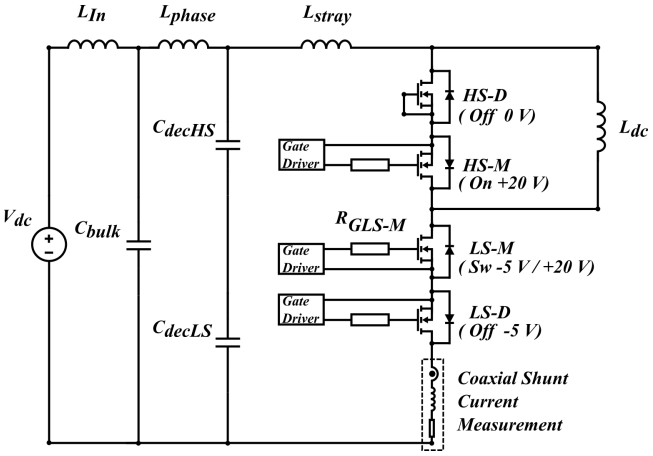

Fig. 4: Switching cell for the proposed CSI Double-Pulse Test.

Moreover, this characterization board is also designed to determine body diode reverse recovery losses. The protocol adopted in this paper is the same as presented in [7], which determines the reverse recovery current during switching event to obtain recovery losses. The CSI cell configuration set for DPT needs to be modified in order to perform this measurement: $\mathrm{L_{dc}}$ has to be connected across the low-side switches instead of the high side and the voltage source $\mathrm{V_{dc}}$ needs to be reversed. Low-side and high-side switches command are swapped to perform DPT. The actual PCB layout has been designed in this purpose.

2.2 Switching cell layout

The CSI layout design, particularly in case of discrete devices, requires an unconventional switching

cell geometry to balance stray inductance between all MOSFETs. A triangular layout has been selected and developed, based on [6]. Despite the balanced parasitic inductances, voltage isolation between $3.3\,\mathrm{kV}$ discrete devices imposes an increased stray inductance ($\mathrm{L_{stray}}$) and PCB thermal resistance ($\mathrm{R_{th,PCB}}$). The PCB stack-up is made of four copper layers. External layers are insulated from internal layers by a $190\,\mu\mathrm{m}$ FR4 layer. Internal layers are insulated from each other by a $1\,\mathrm{mm}$ FR4 layer. The total PCB thickness is $1.6\,\mathrm{mm}$.

The imposed minimal clearance distance in this DPT board is $5\,\mathrm{mm}$. Figure 5 and Fig. 6 show, respectively, the layout schematic and the Double-Pulse Test board. The same board is used for body diode reverse recovery losses evaluation.

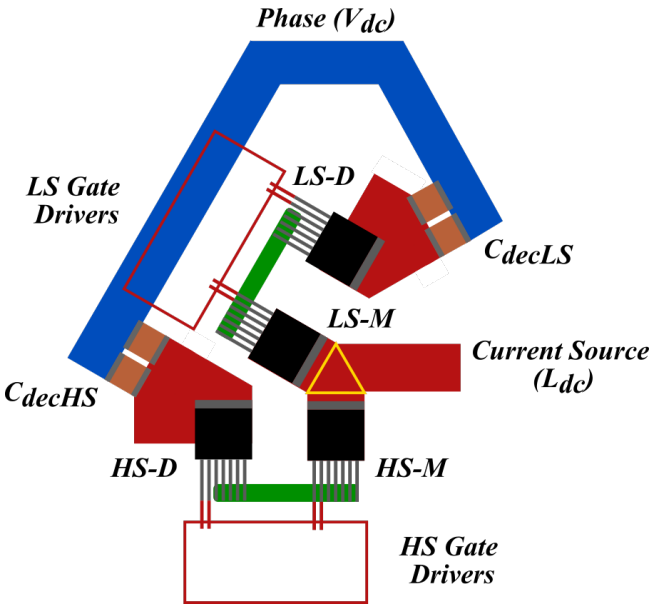

Fig. 5: Switching cell layout.

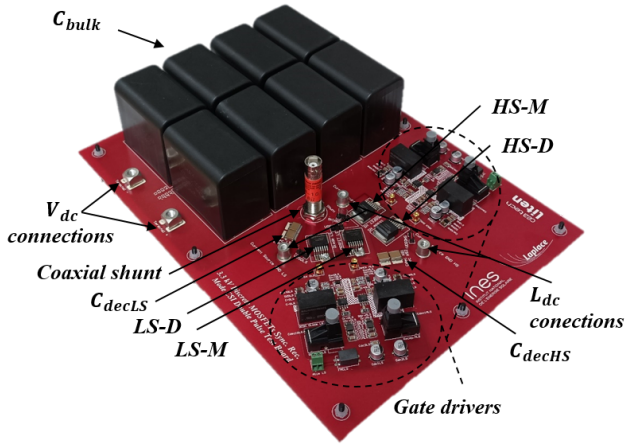

Fig. 6: Double-Pulse Test board.

2.3 Gate driver characteristics

The gate driver used is a Silicon Labs SI826BCC-C-ISR isolated device. Gate to source voltage goes from -5 ($\mathrm{V_{GSoff}}$) to $+20\,\mathrm{V}$ ($\mathrm{V_{GSon}}$). Even if Low-Side (LS) and High-Side (HS) devices are common source connected, each MOSFET has its own gate driver circuit and are isolated to avoid any bouncing potentials during the switching event. Moreover, to insure safe DPT, High-Side Diode gate has also been short-circuited with source connection to set $\mathrm{V_{GS_{HS-D}}}$ at $0\,\mathrm{V}$.

2.4 Voltage and current tested ranges

To evaluate the properties of the switching cell and MOSFET SiC devices, tested switching voltage and current has to be determined. CSI switched voltage range goes from zero to $\hat{V}_{l-l}$: for a $1.5\,\mathrm{kV_{AC}}$ voltage grid, it is $2.1\,\mathrm{kV}$. About the current range, it mainly depends on the chosen device. From a pre-sizing calculation using [4] it appears that maximum current during nominal operation could never exceed $22\,\mathrm{A}$ even with a $30\,\mathrm{W}$ power dissipation. Thus, the maximum current for DPT is established at $22\,\mathrm{A}$ to perform a wide enough characterization.

2.5 Measuring probes

Switching current measurement is performed by a coaxial shunt ($\mathrm{R_{shunt}} = 15\,\mathrm{m\Omega}$, $\mathrm{Bandwidth} = 1.2\,\mathrm{GHz}$) located in the switching loop. Inductance current ($\mathrm{I_{dc}}$) measurement is done with a $30\,\mathrm{A}$ current sensor.

Switched voltage is measured with a $2\,\mathrm{kV}$ passive probe ($\mathrm{BW} = 400\,\mathrm{MHz}$). This probe measures $\mathrm{V_{DS_{LS-M}}} + \mathrm{V_{DS_{LS-D}}}$, this last term is equal to voltage drop through body diode from LS-D. It has to be considered to report more precise switched voltage $\mathrm{V_{DS_{LS-M}}}$. This value is determined during switching data analysis. Bus voltage $\mathrm{V_{dc}}$ is observed by a $6\,\mathrm{kV}$ differential probe. Finally, $\mathrm{V_{GS_{LS-M}}}$ measurement is done with a $25\,\mathrm{V}$ isolated probe : Saker-ISOVP ($\mathrm{BW} = 175\,\mathrm{MHz}$).

3 Switching characterization results

This section discusses MOSFET switching characterization through waveforms analysis, switching energies calculation and then parameters influence on switching event.

3.1 Gate resistance influence on switching event

In order to limit switching losses, $R_{G_{LS-M}}$ influence is investigated. The studied values goes from 10 to $2\,\Omega$. As intended, low $R_{G_{LS-M}}$ reduces switching losses, for both turn-on and turn-off. The counterpart is an increased switching speed $dV_{DS_{LS-M}}/dt$. High $dV_{DS_{LS-M}}/dt$ could provoke crosstalk between devices and then a false turn-on [8] [9]. Double-Pulse preliminary tests have shown that crosstalk effect is likely to occur in operation ranges (especially at high junction temperature (T_j), switched current and voltage) even with a $6\,\Omega$ gate resistor. In order to prevent this phenomenon on any operating point, for the following sections, $R_{G_{LS-M}}$ is established at $8\,\Omega$. This value permits to insure a turn-on $dV_{DS_{LS-M}}/dt$ below $50\,V/ns$ which corresponds to the driver common-mode transient immunity typical value.

3.2 Switching waveforms and energies

Figures 7 and 8 show, respectively, the turn-off and turn-on transients for $I_{DS_{LS-M}} = 22\,A$ and for several $V_{DS_{LS-M}}$ values going from $200\,V$ to $2100\,V$ at $T_{j_{LS-M}} = 25\,℃$.

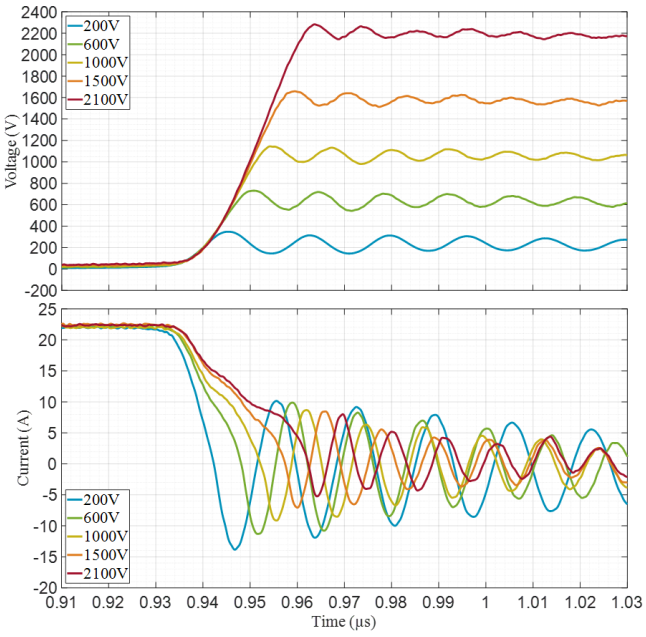

Fig. 7: Superimposed $V_{DS_{LS-M}}$ (top) and $I_{DS_{LS-M}}$ (bottom) waveforms at turn-off at $I_{DS_{LS-M}} = 22\,A$ and for $T_{j_{LS-M}} = 25\,℃$.

At turn-off, $dV_{DS_{LS-M}}/dt$ is around $105\,V/ns$ and $dI_{DS_{LS-M}}/dt$ goes from 3.1 to $0.87\,A/ns$ between $200\,V$ and $2100\,V$.

As intended for a MOSFET, higher voltage turn-off presents a slower current switching compared to lower voltage turn-off but also presents a lower switching current overshoot and oscillations.

For $V_{DS_{LS-M}} = 200\,V$ and $I_{DS_{LS-M}} = 22\,A$, current overshoot reaches $-14\,A$. Concerning voltage overshoot, at low switching voltage, for $V_{DS_{LS-M}} = 200\,V$, it exceeds $60\,\%$ of V_{dc}. At high switching voltage, voltage overshoot is small with only $8\,\%$ of V_{dc} (around $2250\,V$), for $V_{DS_{LS-M}} = 2100\,V$.

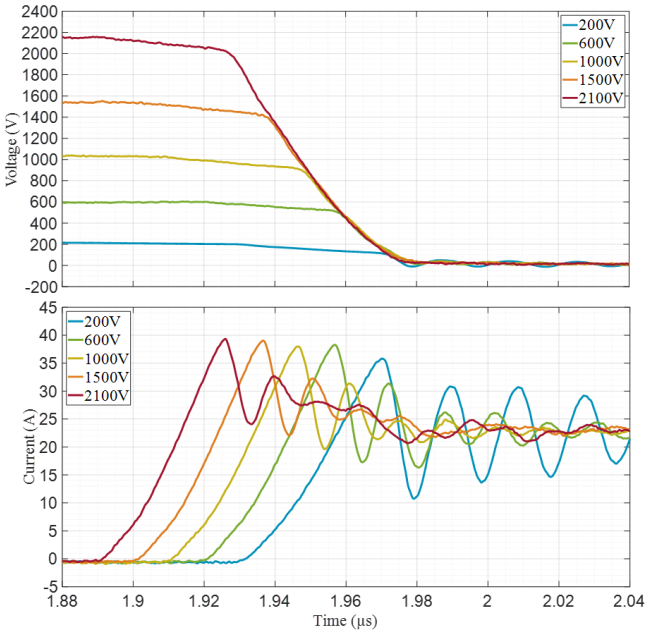

Fig. 8: Superimposed $V_{DS_{LS-M}}$ (top) and $I_{DS_{LS-M}}$ (bottom) waveforms at turn-on at $I_{DS_{LS-M}} = 22\,A$ and for $T_{j_{LS-M}} = 25\,℃$.

At turn-on, $dV_{DS_{LS-M}}/dt$ is around $43.5\,V/ns$ and $dI_{DS_{LS-M}}/dt$ goes from 0.98 to $1.32\,A/ns$ between $200\,V$ and $2100\,V$. Higher turn-on voltage presents an earlier rising current which provokes a slightly higher current overshoot : almost $40\,A$ for $V_{DS_{LS-M}} = 2100\,V$ instead of $36\,A$ for $V_{DS_{LS-M}} = 200\,V$ for a $22\,A$ switched current value.

Although this lower overshoot current value, low switched voltage waveforms shows a slow mitigation in oscillations of switched current, as for turn-off event.

Thus, switching energies are calculated. They are considered between $V_{GS_{LS-M}} = 10\,\% \cdot \Delta V_{GS}$ and $V_{DS_{LS-M}} = 10\,\% \cdot V_{dc}$ for turn-on, between $V_{GS_{LS-M}} = 90\,\% \cdot \Delta V_{GS}$ and $V_{DS_{LS-M}} = 90\,\% \cdot V_{dc}$ for turn-off calculation.

Figure 9 shows the energies for three switching current values at $\mathrm{T_{j_{LS-M}}} = 25$ ℃.

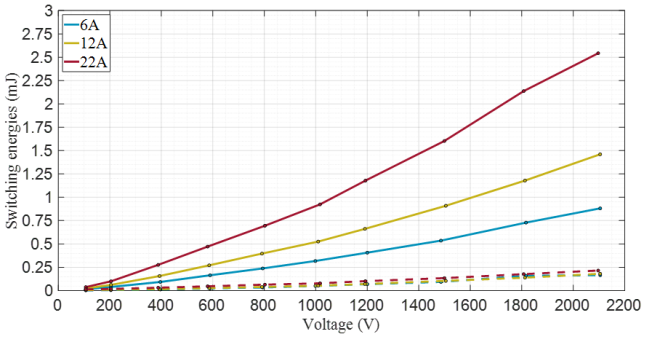

Fig. 9: Turn-on (full lines) and turn-off (dashed lines) switching energies for $\mathrm{I_{DS_{LS-M}}} = 6, 12$ and 22 A and $\mathrm{T_{j_{LS-M}}} = 25$ ℃.

Based on observation of Fig. 9, switching energies are mainly due to turn-on event. They increase with both current and voltage. Due to restrictive switching cell layout, high parasitic inductance penalizes switching voltage drop and then, rises turn-on losses by a significant factor. This inductance has been measured: $\mathrm{L_{stray}} = 120$ nH.

A rapid comparison with device datasheet clearly indicates that with this particular layout turn-on energies are heavily increased. Moreover, to make a 3.3 kV SiC MOSFET switching at 2100 V, i.e at 64 % of its drain-source breakdown voltage value, imposes a substantial constraint.

3.3 Temperature influence on switching event

Concerning temperature influence on switching event, the use of MOSFET body diode may imply a significant increasing of switching energies with an increased junction temperature.

Therefore, this section aims is to determine the influence of MOSFET junction temperature ($\mathrm{T_j}$) on switching energies. Concerning thermal conditions, a heat plate is used to rise and control the semiconductors junction temperatures, from 25 to 150 ℃.

Drivers temperatures are maintained below 70 ℃ to perform a realistic switching and not to bias the results. Temperatures are checked during tests by a thermal camera.

Figure 10 shows turn-on transients for a varying junction temperature. Concerning turn-off event, it is not affected by increased MOSFET junction temperature.

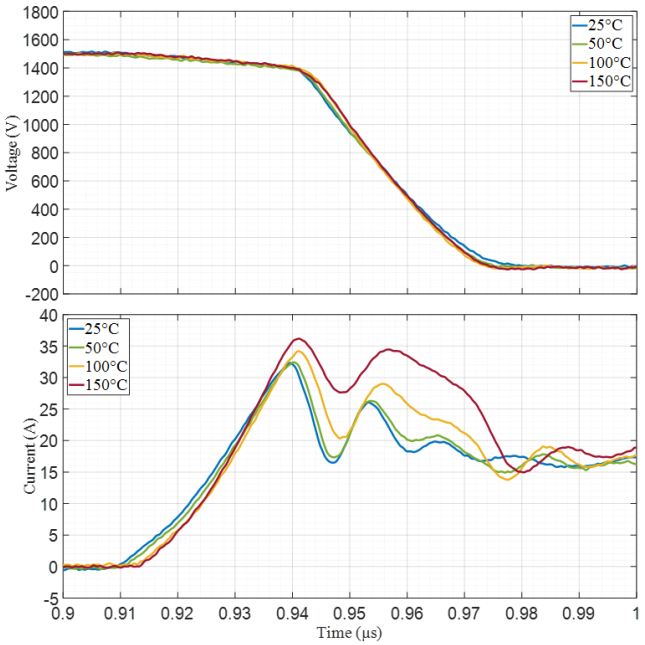

Fig. 10: Superimposed $\mathrm{V_{DS_{LS-M}}}$ (top) and $\mathrm{I_{DS_{LS-M}}}$ (bottom) waveforms at turn-on for $\mathrm{T_{j_{LS-M}}}$ varying from 25 to 150 ℃ at $\mathrm{V_{DS_{LS-M}}} = 1500$ V and $\mathrm{I_{DS_{LS-M}}} = 16$ A.

This last figure indicates that the peak current increases with increasing junction temperature. Switched voltage $\mathrm{V_{DS_{LS-M}}}$ is not affected by temperature variation. $\mathrm{dI_{DS_{LS-M}}/dt}$ is slightly affected by temperature increased. Additional losses are due to current higher oscillations during the switching event.

Moreover, table 1 below highlights increased energies (and then losses) due to increased temperatures for Fig. 10 waveforms.

Junction temperature (℃)	Switching energy (µJ)
25	1166
50	1139
100	1200
150	1351

Tab. 1: Turn-on switching energies at $\mathrm{V_{DS_{LS-M}}} = 1500$ V, $\mathrm{I_{DS_{LS-M}}} = 16$ A and for $\mathrm{T_{j_{LS-M}}}$ varying from 25 to 150 ℃.

To determine the impact of temperature, Fig. 11 resumes switching energies at $T_{j_{LS-M}} = 150$ ℃ compared with energies obtained at $T_{j_{LS-M}} = 25$ ℃.

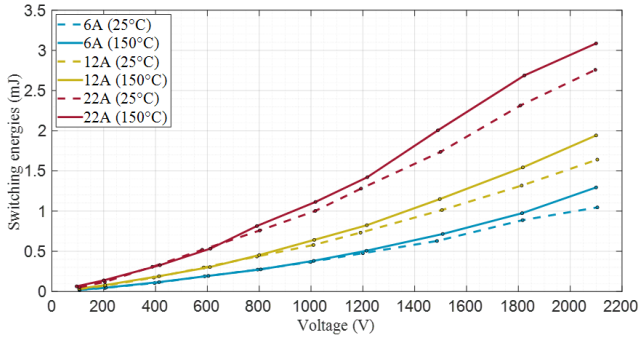

Fig. 11: Total switching energies at $T_{j_{LS-M}} = 25$ ℃ (dashed lines) and $T_{j_{LS-M}} = 150$ ℃ (full lines) for $I_{DS_{LS-M}} = 6, 12$ and 22 A.

Thus, increasing the junction temperature from 25 to 150 ℃ causes an increase in turn-on switching energies between 10 and $20\,\%$ (at high voltage) when compared to Fig. 9 (or Fig. 11 dashed lines). Thereby, switching behaviour of MOSFET device is affected by increased temperature. This dependence will have to be taken into account for the design of the final converter.

4 Body diode reverse recovery characterization

Body diode main issues are maximal recovery current $I_{rr,max}$ that could exceed device limits in specific conditions and voltage, current and temperature impact on turn-off event. To apprehend switching energies generated by MOSFET body diode also allows to have a more precise approach of switching losses distribution compared to MOSFET channel.

Moreover, determining the body diode behaviour becomes necessary to study the deadtime used in synchronous rectification operating mode.

4.1 Body diode turn-off waveforms

Figure 12 shows the body diode turn-off transient for $I_{D_{LS-D}} = 20$ A and for varying voltage $V_{DS_{LS-D}}$ going from 200 V to 2100 V at $T_{j_{LS-D}} = 25$ ℃. This figure shows limited recovery current oscillations at high voltage compared to low voltage, especially for $V_{DS_{LS-D}} = 200$ V.

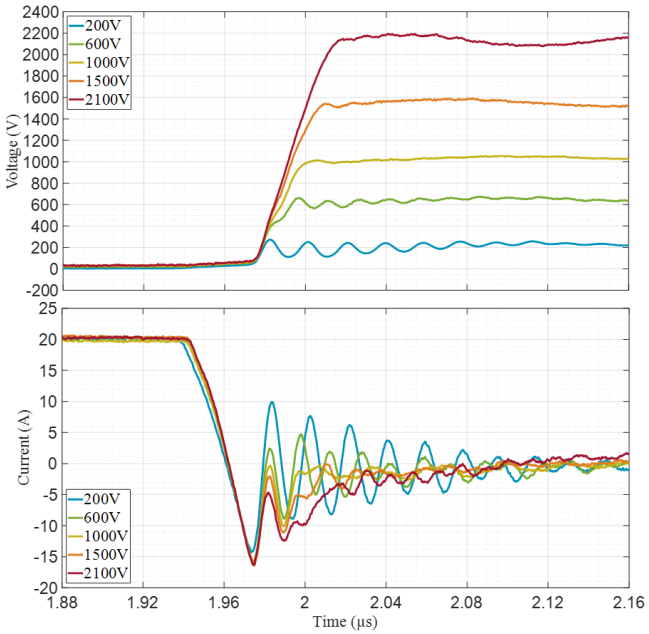

Fig. 12: Superimposed MOSFET body diode $V_{DS_{LS-D}}$ (top) and $I_{D_{LS-D}}$ (bottom) waveforms at turn-off $I_{D_{LS-D}} = 20$ A and for $T_{j_{LS-D}} = 25$ ℃.

The peak reverse recovery current ($I_{rr,max}$) is around -17 A for $I_{D_{LS-D}} = 20$ A and at $T_{j_{LS-D}} = 25$ ℃.

Figure 13 shows that $I_{rr,max}$ increases with junction temperature, reaching -27 A at $T_{j_{LS-D}} = 150$ ℃, which implies higher reverse recovery losses.

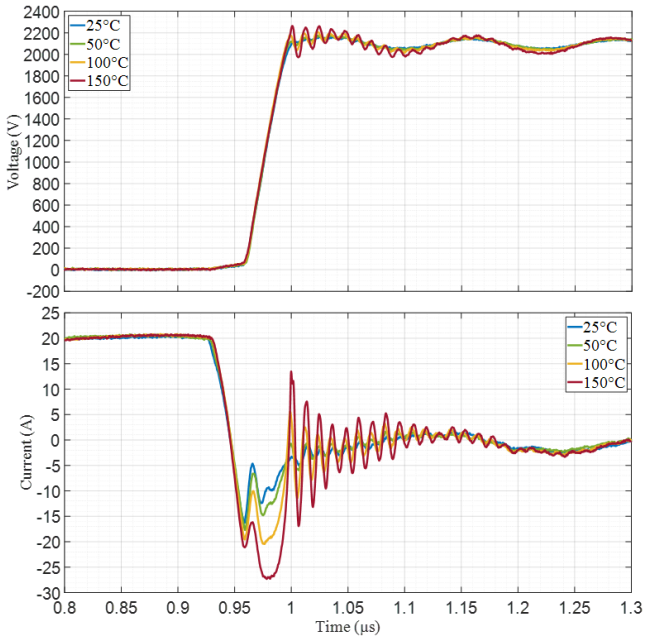

Fig. 13: Superimposed MOSFET body diode $V_{DS_{LS-D}}$ (top) and $I_{D_{LS-D}}$ (bottom) waveforms at turn-off for $T_{j_{LS-D}}$ varying from 25 to 150 ℃ at $V_{DS_{LS-D}} = 2100$ V and $I_{D_{LS-D}} = 20$ A.

4.2 Body diode reverse recovery energies

The next step to determine body diode reverse recovery energies is to extract MOSFET output parasitic capacitance (C_{oss}) contribution in recovery charges. At turn-off, total recovery charges (Q_{rr}) comes from both bipolar charges (Q_{bip}) stored in PN-diode and C_{oss} charges (Q_{oss}).

Capacitive energy E_{oss} is not dissipated within the device during body diode turn-off. On the other hand, for $3.3\,kV$ body diode, bipolar charges and then losses are not negligible, especially with high currents and temperatures conditions [10].

Then, Q_{oss} is determined by body diode turn-on behaviour. It only depends on applied voltage, i.e. $V_{DS_{LS-D}}$. Thanks to turn-off reverse recovery current waveforms, Q_{bip} is isolated from Q_{oss}. Equation (2) resumes Q_{rr} charges definition.

$$Q_{rr} = \int_{t_{rr1}}^{t_{rr2}} I_{D_{LS-D}} dt = Q_{oss} + Q_{bip} \qquad (2)$$

Figure 14 shows both contribution of Q_{rr} and Q_{oss} on reverse recovery charges. Difference between lines and Q_{oss} level corresponds to Q_{bip} charges. Q_{bip} increases with current and temperature.

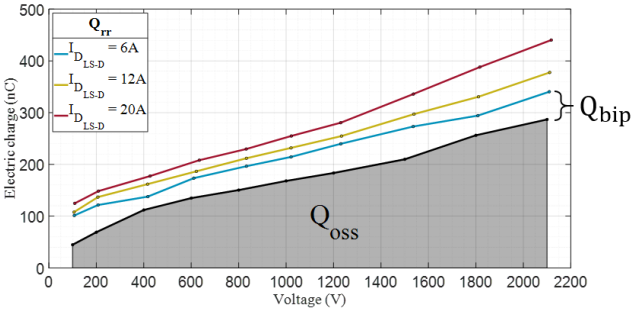

Fig. 14: Q_{rr} and Q_{oss} evolution for $I_{D_{LS-D}} = 6, 12$ and $20\,A$ and $T_{j_{LS-D}} = 25\,°C$.

Moreover, Fig. 15 and Fig. 16 show the temperature influence on bipolar charges evolution, for 6 and $20\,A$ respectively.

Figure 15 and Fig. 16 displays that at high temperature, Q_{bip} also increases with a increasing switching voltage. This effect is particularly observable at high current, here at $20\,A$.

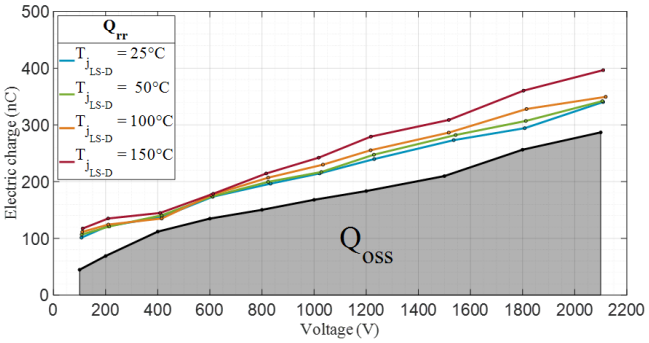

Fig. 15: Q_{rr} and Q_{oss} evolution for $I_{D_{LS-D}} = 6\,A$ and $T_{j_{LS-D}}$ varying from 25 to $150\,°C$.

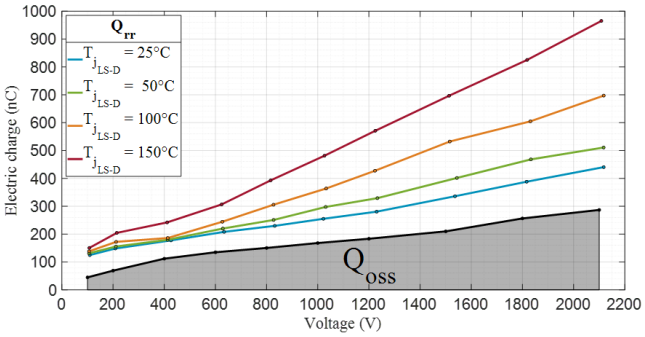

Fig. 16: Q_{rr} and Q_{oss} evolution for $I_{D_{LS-D}} = 20\,A$ and $T_{j_{LS-D}}$ varying from 25 to $150\,°C$.

As C_{oss} contribution only depends on voltage, bipolar charges Q_{bip} becomes more and more predominant in reverse recovery charges Q_{rr} with the increase of current and temperature that implies higher body diode reverse recovery energies, as developed further next.

Thus, body diode reverse recovery energy during turn-off is defined by :

$$E_{rec} = \int_{t_{rr1}}^{98\%V_{dc}} V_{DS_{LS-D}} \cdot I_{D_{LS-D}} dt - E_{oss} \qquad (3)$$

As exposed in [10], for high voltage and stray inductance (i.e. important oscillations during switching event) conditions, the upper integration limit is set at $98\,\%\,Vdc$.

To remain valid, $I_{D_{LS-D}}$ has to be very close to zero when $V_{DS_{LS-D}}$ reaches $98\,\%\,Vdc$. Both conditions has been considered to extract more precise reverse recovery energies.

Figure 17 shows the evolution of recovery energies at $T_{j_{LS-D}} = 25$ °C.

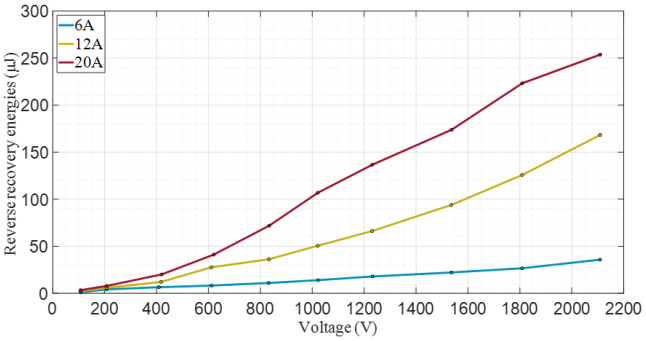

Fig. 17: Body diode reverse recovery energies for $I_{D_{LS-D}} = 6, 12$ and 22 A and $T_{j_{LS-D}} = 25$ °C.

Figure 18 shows the evolution of recovery energies for $I_{D_{LS-D}} = 6$ A, $T_{j_{LS-D}}$ varying from 25 to 150 °C.

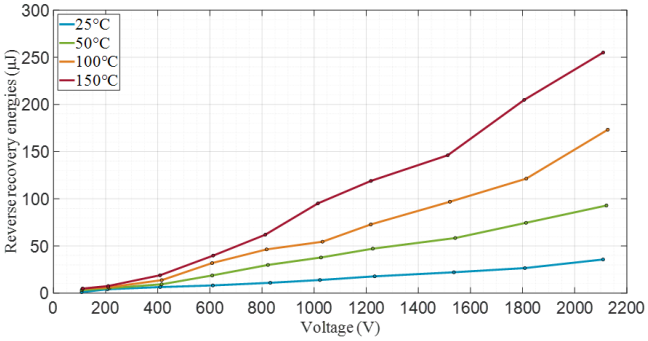

Fig. 18: Body diode reverse recovery energies for $I_{D_{LS-D}} = 6$ A and for $T_{j_{LS-D}}$ varying from 25 to 150 °C.

At last, Fig. 19 shows the evolution of recovery energies for $I_{D_{LS-D}} = 20$ A, $T_{j_{LS-D}}$ varying from 25 to 150 °C.

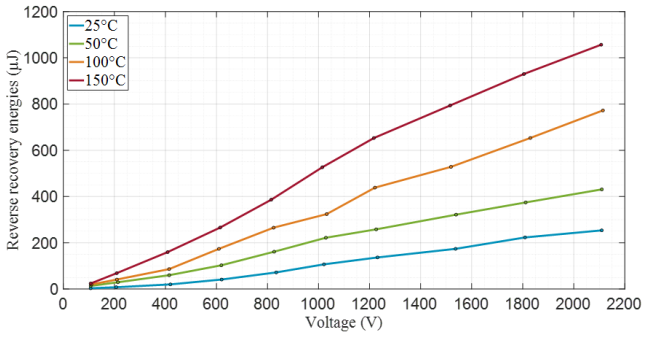

Fig. 19: Body diode reverse recovery energies for $I_{D_{LS-D}} = 20$ A and for $T_{j_{LS-D}}$ varying from 25 to 150 °C.

From two last figures, it can be noticed that increased junction temperature causes an important increasing in body diode reverse recovery energies. For any switched current value, the increase in energies is around 250 % between 25 and 150 °C.

5 Perspective of switching performances for future CSI operation

This last section purpose is to discuss about how the characterization of switching behaviour of 3.3 kV SiC MOSFET helps to better determine the future CSI operation, i.e. its performances and its limits. First, it allows to optimize switching sequence, especially when introducing synchronous rectification.

5.1 Synchronous rectification deadtime

Body diode seems to present higher conduction losses than MOSFET channel. To avoid increased conduction losses, MOSFET channel of $D_{P(1,2,3)}$ and $D_{N(1,2,3)}$ (Fig. 3) should be turned on right after the body diode is forward-biased.

However, the turn-on cannot be done at any time. With an early trigger, i.e. body diode is not completely forward-biased, a short-circuit may occur. In addition of being a safety issue, it results in increased recovery energies. A deadtime has to be established to turn-on the channel without short-circuit. This minimum deadtime (DT_{min}) value increases with current, voltage and temperature rise.

To insure a proper operation of the converter, minimum deadtime is determined for the most extreme conditions. Moreover, turn-on MOSFET channel during body diode polarization reduces reverse recovery current and voltage overshoot and then have a beneficial influence on body diode reverse recovery energies during turn-off event [11].

Figure 20 is used in order to find this minimum value. At $T_{j_{LS-D}} = 150$ °C, MOSFET gate to source voltage threshold of the opposite MOSFET device $HS-M$ is $V_{GSth} \simeq 2.5$ V, so minimal deadtime DT_{min} corresponds to the duration that begin at $V_{GS_{HS-M}}$ drop, i.e. the reception of turn-off order by gate driver, until this voltage falls below threshold (here 2.5 V).

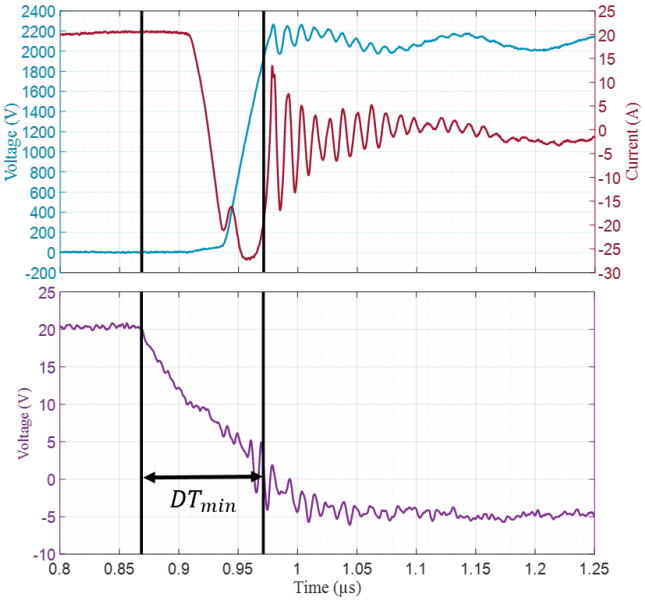

Fig. 20: MOSFET body diode voltage $\mathrm{V_{DS_{LS-D}}}$ at $2100\ \mathrm{V}$ (top - cyan), current $\mathrm{I_{D_{LS-D}}}$ at $20\ \mathrm{A}$ (top - burgundy) and $\mathrm{V_{GS_{HS-M}}}$ (bottom - purple) waveforms during LS-D turn-off at $\mathrm{T_{jLS-D}} = 150\ ℃$.

Based on observation of Fig. 20, $\mathrm{DT_{min}} = 102\ \mathrm{ns}$. This study will need to be completed by future tests to determine deadtime impact on body-diode turn-off behaviour. With a deadtime shorter than $102\ \mathrm{ns}$, a short-circuit is very likely to occur during switching event.

To verify if determined value of $\mathrm{DT_{min}}$ is accurate, reverse recovery energies should be analyzed for multiple switched voltage and current values. By $\mathrm{DT_{min}}$ definition, they should be minimal for this time duration. Thus, the following step is to try to increase deadtime and determine if an increased duration heavily penalizes body diode reverse recovery energies.

One perspective of this future study is that the reduction of body diode turn-off energy by optimized deadtime could be negligible regarding body diode reverse recovery losses ratio on global switching losses and moreover on converter losses. In this case, it could be more relevant to accept an increased deadtime in order to insure a safe synchronous rectification management. This perspective will be investigated further.

5.2 Switching losses in operational CSI

This section purpose is about to evaluate generated switching losses in the future CSI. Thanks to $3.3\ \mathrm{kV}$ characterization, future CSI switching losses can be estimated. With obtained data and using the calculation tool developed in [4], this evaluation is resumed in Fig. 21 where the evolution of switching losses for one $3.3\ \mathrm{kV}$ MOSFET device for a set switching frequency ($\mathrm{f_{sw}}$) is presented.

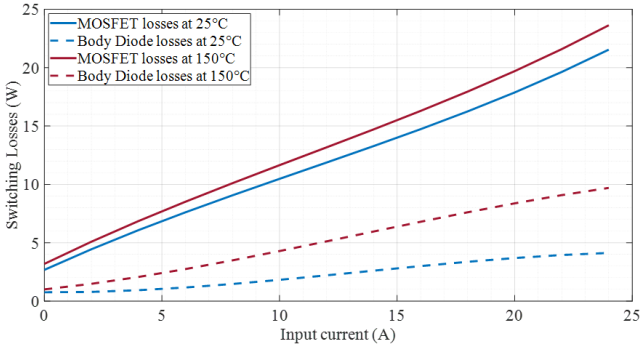

Fig. 21: MOSFET (full lines) and body diode (dashed lines) switching losses evolution depending on operating current at $\mathrm{T_j} = 25$ (blue) and $150\ ℃$ (red) for one G2R120MT33J device, switching at $\mathrm{f_{sw}} = 50\ \mathrm{kHz}$.

This figure indicates that MOSFET losses are predominant over body diode losses, but increase more slightly with junction temperature. As evoked in section 2.4, maximum current mainly depends on device package power dissipation.

Figure 21 shows that combined switching losses reach $16\ \mathrm{W}$ at $10\ \mathrm{A}$ and exceed $20\ \mathrm{W}$ at $15\ \mathrm{A}$ for $\mathrm{T_j} = 150\ ℃$. When considering conduction losses, global semiconductors losses are even more important. Therefore, maximum operating current will probably be around $10\ \mathrm{A}$, for a maximum of $150\ ℃$ junction temperature and for a $50\ \mathrm{kHz}$ switching frequency.

6 Conclusion

In this paper, $3.3\ \mathrm{kV}/120\ \mathrm{m\Omega}$ MOSFET characterization has been performed to evaluate the switching event for this particular switching cell layout for a future CSI application.

Complete switching current and voltage ranges have been investigated as for varying junction temperature. Body diode reverse recovery has been characterized in order to determine its impact on switching losses definition.

As seen before, switching event is subjected to strong constraints especially at high switching voltage and high parasitic inductance. These constraints will cause increased switching losses in the future converter. Future works will investigate deadtime influence on switching performances.

Acknowledgment

This work was partially supported by the French National Program “Programme d’Investissements d’Avenir - INES.2S” under Grant ANR-10-IEED-0014-01.

References

[1] K. Zeb, W. Uddin, M. A. Khan, Z. Ali, M. U. Ali, *et al.*, “A comprehensive review on inverter topologies and control strategies for grid connected photovoltaic system,” *Renewable and Sustainable Energy Reviews*, vol. 94, pp. 1120–1141, 2018. DOI: 10.1016/j.rser.2018.06.053.

[2] Y. Song and B. Wang, “Survey on reliability of power electronic systems,” *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 591–604, 2013. DOI: 10.1109/TPEL.2012.2192503.

[3] L. Gabriel, A. Rodrigues, J.-P. Ferrieux, J. Martin, S. Catellani, and A. Bier, “Design of a three-phase 70 kw current source inverter for photovoltaic applications using a new 1.7 kv full-sic voltage bidirectional power module,” in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–8.

[4] L.-A. Gomez, L. G. Alves Rodrigues, G. Gateau, and S. Sanchez, “On the potential of parallel multilevel current source inverter using sic devices for renewable applications,” in *2021 22nd IEEE International Conference on Industrial Technology (ICIT)*, vol. 1, 2021, pp. 1377–1382. DOI: 10.1109/ICIT46573.2021.9453689.

[5] W. Choi, S. Young, D. Son, S. Shin, and D. Hyun, “Consideration to minimize power losses in synchronous rectification,” in *8th International Conference on Power Electronics - ECCE Asia*, 2011, pp. 2899–2905.

[6] G. Lefevre, “Design of a low inductive switching cell dedicated to sic based current source inverter (csi),” in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–6.

[7] A. Kumar, K. Vechalapu, S. Bhattacharya, V. Veliadis, E. Van Brunt, *et al.*, “Effect of capacitive current on reverse recovery of body diode of 10kv sic mosfets and external 10kv sic jbs diodes,” in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 208–212.

[8] I. Laird and X. Yuan, “Analysing the crosstalk effect of sic mosfets in half-bridge arrangements,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 367–374. DOI: 10.1109/ECCE.2019.8913115.

[9] J. Yang, G. Feng, L. Huadong, and C. Suhong, “Characterization and detailed analysis of the crosstalk with sic mosfet,” in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2018, pp. 239–243. DOI: 10.1109/WiPDAAsia.2018.8734655.

[10] P. Sochor, A. Huerner, M. Hell, and R. Elpelt, “Understanding the turn-off behavior of sic mosfet body diodes in fast switching applications,” in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[11] R. Horff, A. Maerz, and M.-M. Bakran, “Analysis of reverse-recovery behaviour of sic mosfet body-diode - regarding dead-time,” in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1–8. DOI: 10.1109/WiPDA.2017.8170548.