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Hassan Hamad, Dominique Tournier, Jean-Michel Reynes, Olivier Perrotin, David Trémouilles, et al..
First results on 1.2 kV SiC MOSFET body diode robustness tests. *Microelectronics Reliability*, 2023,
151, pp.115264. 10.1016/j.microrel.2023.115264 . hal-04282544

HAL Id: hal-04282544

<https://hal.science/hal-04282544v1>

Submitted on 13 Nov 2023

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First Results on 1.2 kV SiC MOSFET Body Diode Robustness Tests

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Abstract

The paper proposes a methodology study to analyze the body diode robustness of SiC MOSFETs. Devices from different manufacturers are used to validate the analysis. Two types of stresses have been applied: a continuous conduction test (BDCT) or a pulsed conduction test, the classical half-sine surge current test applied to body diodes, BDSCT. BDCT applied current must be limited to avoid damages related to the packaging but BDSCT allows analyzing both assembly degradation and bipolar degradation.

Keywords: SiC MOSFET; Reliability; Body Diode; Surge Test

1 Introduction

Silicon carbide (SiC) is nowadays popular in the domain of power electronics. Compared to silicon (Si), its physical characteristics are advantageous [1] [2]. The maturity of SiC manufacturing makes it the best candidate to replace the silicon (Si) in the domain of power electronics, except probably for high frequency needs [3] where nitride gallium (GaN) could be further efficient.

Most of the SiC properties yield a clear advantage for SiC versus silicon power devices. However, the reliability of SiC power devices is reduced with respect to silicon ones. Reliability issues related to the gate oxide are well addressed and numerous studies have been published on the topic of threshold voltage instabilities [4] [5].

Moreover, SiC MOSFET body diodes could be used to design diodeless converters. However, more studies about their behavior, reliability and robustness have to be conducted. It is also a classical way in power electronics to use the body diode to avoid an additional external Schottky diode [6]. Body diode static and dynamic characteristics were analyzed [7]. In addition, the effect of a continuous current through the body diode was studied [8] [9]. Moreover, the body diode reliability was studied for pulsed currents [9] and for surge currents [10] [11] where bipolar degradation was shown at high current levels. In this paper, the body diode of SiC power MOSFET is studied for several device manufacturers. The comparison between continuous and pulsed tests is relatively rare in the literature. A classical negative temperature coefficient of the diode current involves a possible device temperature inhomogeneity effect when the devices are flowed with a continuous DC current. Local overheats could limit the maximum current allowed through the body diode due to package degradation [12].

So, a static characterization and temperature calibration were performed. Then, experimental tests were achieved to compare the interest of both approaches.

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Observing the diode conduction is not a standard test and little described in the manufacturer datasheets. Such a test could be described by the JEDEC Standard, high temperature forward bias (HTFB) [13], but this standard addresses diodes and how gate is biased is not specified. In this study the Body Diode Conduction Test, BDCT, already described in [8], enables to easily stress several body diodes during a long time, by applying a common and constant series current. Another classical stress is the surge current stress for diodes [14] that could be named Body Diode Surge Current Test, BDSCT for body diodes [15].

In the present study, 1.2 kV SiC MOSFET body diodes were stressed and studied to identify any aging or degradation issues in practical use cases.

The expected degradation phenomena are the metalization degradation and associated metal reconstruction [16] and the bipolar degradation [11].

The paper presents methodologies to analyze the reliability of SiC MOSFET body diodes to better know if the applications using the body diodes of power MOSFETs could be a good solution. Both continuous conduction tests (BDCT) and surge current tests (BDCST) are studied. Section 3 considers the BDCT, which has been very little treated in the literature, while section 4 examines the BDSCT. In all cases the gate voltage for which most of the current passes mainly in the diode and not the channel must be defined. This is addressed in section 2, as well as the other measurement protocol issues. Finally, as the paper target is a methodology to study the reliability issues of body diodes, in all the cases, the target is to apply the most stressing conditions, particularly for the junction temperature as it will be seen in section 3.

In this paper, SiC Power MOSFETs were studied from three different manufacturers (Table 1).

Table 1: Studied Devices. Three pins TO-247 packages were used, from 3 manufacturers. The columns include rating values. V_{FT} and V_{SGT} are defined in Table 2

Manufacturer	V_{MAX} (V)	I_N (A)	V_{GS-min} (V)	R_{DS-ON} (m Ω)	V_{FT} (V)	V_{SGT} (V)
A	1200	33	-10	75	5.58	9.98
B	1200	60	-10	40	5.17	5.77
C	1200	40	-10	80	5.64	3.19

2 Measurements and Protocols

Table 1: Main Signal Definitions

Symbol	Definition
I_N	Nominal current, i.e., the current rating as defined in the datasheet.
I_F	$I_F = -I_D$, is the current flowing through the body diode.
V_F	$V_F = -V_{DS}$, is the voltage drop across the body diode.
V_{SG}	$V_{SG} = -V_{GS}$, is the reverse gate-source voltage. V_{SG} is positive in our tests.
V_{FT}	Maximal value of V_F for a given forward current I_F . See .
V_{SGT}	Threshold value of V_{SG} where V_F reach 99% of the maximal value V_{FT} . See .
T_P	Aluminum Plate temperature, see .
V_{TH}	Threshold voltage

Devices are characterized before and after being stressed. shows body diode characteristics, i.e., I_F - V_F for varying V_{SG} . Indeed, for low V_{SG} , the channel is still conducting some current [17], [18].

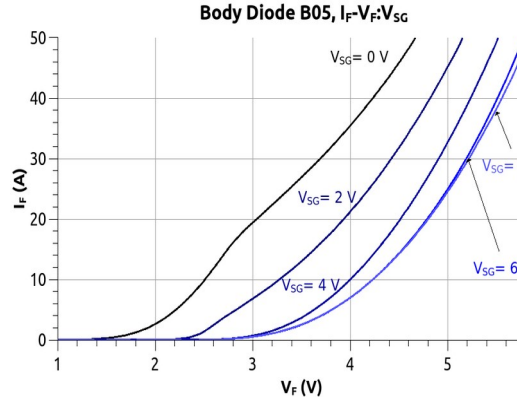


Fig. 1: I_F - V_F characteristics for device B05 and varying V_{SG} .

V_{TH} measurement is another key issue for SiC MOSFET reliability. Hysteresis and relaxation may affect the

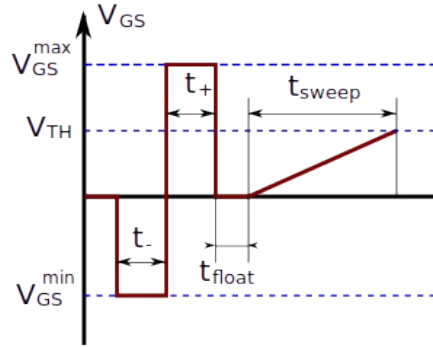


Fig. 1: V_{TH} preconditioning definitions. See

V_{TH} measurement. Applying a negative gate voltage before V_{TH} measurement was proposed in [19] for reliability studies. For Bias Temperature Instability (BTI) studies, a bipolar preconditioning, using both positive and negative gate bias before V_{TH} measurement, is presented in [20] and this is a basis of JEP184 [21].

Table 1: Definition and typical values for the SiCRET bipolar preconditioning protocol

Symbol	Definition	Typical Value
V_{GS}^{min}	Minimal applied value of the gate-source pins. This is selected to be the minimal value specified in the datasheet.	$-10\text{ V} \leq V_{GS}^{min} \leq -4\text{ V}$
V_{GS}^{max}	Maximal applied value of the gate-source pins. This is selected to be the maximal value specified in the datasheet.	$18\text{ V} \leq V_{GS}^{max} \leq 23\text{ V}$
t_-	Duration of the negative preconditioning.	80 ms
t_+	Duration of the positive preconditioning.	5 s
t_{float}	Duration before the measurement of the V_{TH}	< 1 ms
t_{sweep}	Maximal duration of the voltage sweeping	200 ms for 5V

Unfortunately, the values recommended by the JEP183 [22] are not possible with a classical semiconductor characterization tool as Keysight B1505A, because the equipment is not fast enough.

So, the **SiCRET preconditioning protocol** was developed to reach very similar values of the V_{TH} measurements. It is specified in Table 1. The measured values have been validated with respect to the JEP 183/184, bipolar preconditioning protocol, on production testers at Alter Technology (FTI 1000, from Focused Test). Moreover, the protocol has been validated to obtain very close results on two different laboratories (Ampère and LAAS) on different B1505A systems.

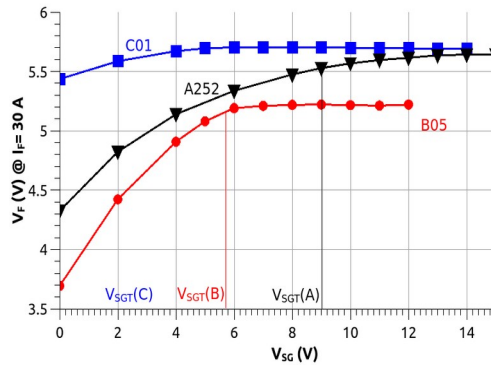


Fig. 1: V_F vs. V_{SG} at $I_F = 30$ A, showing V_{SGT} for each manufacturer, at room temperature. The selected devices for measurements are A252, B05 and C01.

The gate-source voltages to be applied were studied for the different manufacturers. displays the V_F vs. V_{SG} measurements for $I_F = 30$ A for the studied components in Table 1 curves show that for higher V_{SG} , V_F increases until it reaches a maximum value (V_{FT}) for which, the increase of V_{SG} does not affect V_F . At this threshold, V_{SGT} , only the diode is conducting and the channel is supposed to be completely blocked.

However, the manufacturers recommend limiting the negative gate-source bias. $V_{SG} = 5$ V was selected because it is not too high to limit the associated stress and in this condition most of the current flows mainly through the diode. This selected value is similar to the maximal reverse value of the source-to-gate voltage recommended by some manufacturers.

Before starting the BDCT stress, all the DUTs are calibrated for a real-time estimation of the temperature. For the calibration, the temperature is controlled using a Thermonics TE2500. The I_F - V_F characteristic is measured for temperature going from room temperature to the maximal specified temperature (200 °C for A, 150 °C for B and 175 °C for C) with a step of 25 °C, as shown in . Note that these characterizations are performed in pulsed mode to avoid the self-heating of the devices. The voltage drop across the diode could be considered as an accurate indicator for the maximal junction temperature in the device.

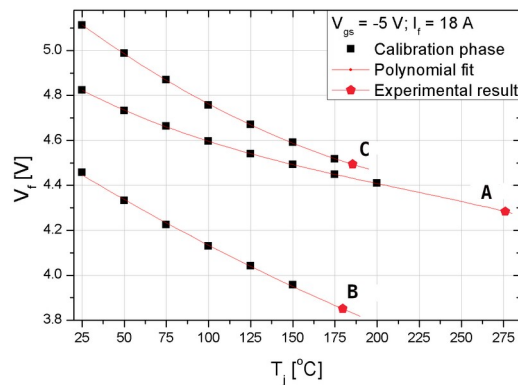


Fig. 1: Junction temperature evaluation at $I_F = 18$ A for the three manufacturers A, B and C. Experimental results were obtained during the stress in red.

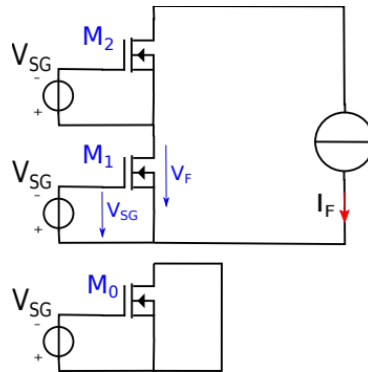


Fig. 1: Schematic of the BDCT Setup

3 BDCT

3.1 Experimental Setup

Body diode conduction tests (BDCTs) were performed on different devices and manufacturers. The schematic is shown in

For a given manufacturer, up to four devices are fixed using screws on a heat sink, i.e., a rectangular aluminum plate (length: 12 cm, width: 7 cm, height: 3 cm). The symmetrical emplacement of the devices allows almost equal temperature of their cases. Another component (M_0) serves as a reference and does not undergo any current flow, so it received HTGB conditions. A heating cartridge is put at the center of the plate as shown in . The temperature of the plate is controlled using a thermocouple fixed inside the heating plate put (8 mm) below M_1 . Up to four devices of the same manufacturer are put in series on a heat plate as shown in . The distribution of the four devices (M_1 to M_4) on the plate is symmetrical to obtain a better temperature homogeneity on the plate.

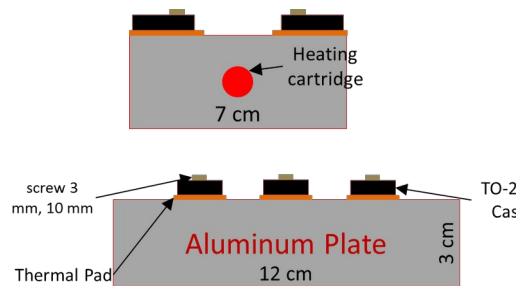


Fig. 1: Left view of the aluminum plate (top) and front view (bottom).

The experimental BDCT test bench is presented in Fig. 7. It includes all the safety devices to ensure a permanent operation, 24 hours a day, 7 days a week.

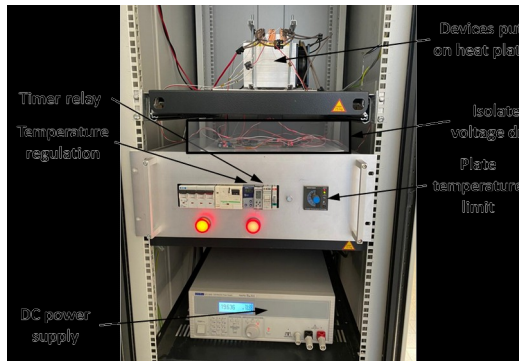


Fig. 1: Experimental BDCT test bench

3.2 First Stress Run

For a first run, the current and plate temperature have been selected to reach the maximal junction temperature specified by the datasheet. Unfortunately, the junction temperature is an estimation based on the thermal model given in the datasheet, and the power dissipation obtained by measurements ().

The stress conditions were,

Test 1: $I_F=25$ A, $V_{SG}=5$ V, $T_P=120$ °C, 4 devices flowed by I_F .

At the beginning of the stress, measured voltage drops, V_F , were significantly lower than expected to regard to the temperature calibration made before starting the stress, as shown in . However, it was decided to keep the stress conditions as they are, and at the first 20 hours, all devices were destructed or damaged.

For both manufacturers, devices have shown overheat when studying 4 devices at the same time. Indeed, it must be noticed that even for a DC current of 18 A, the average power to dissipate was about 75 W per device. Failure analyses have confirmed the overheating near the surface metalization.

3.3 Discussion on the Thermal Issue

Because of these unexpected damages, we tried to identify the source of the problem. Using a new device from manufacturer C, an oscilloscope was used to record the result shown in .

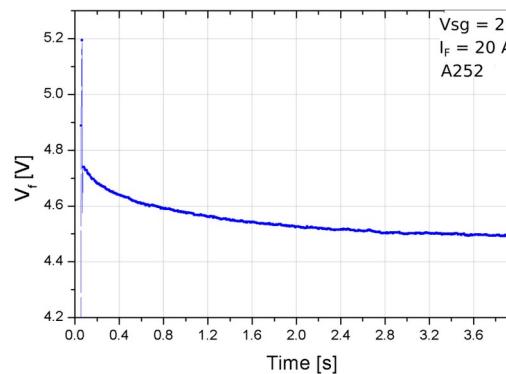


Fig. 1: Transient voltage drop across the body diode when applying a DC current through it.

It is assumed that the calibration curve in is well established, because the self-heating is negligible using the measurement protocol. Indeed, a Keysight B1505A had been used with a pulse duration of 50 μ s. However, clearly shows a self-heating phenomenon, which is probably the most original result of the paper and a warning on the BDCT difficulties. The identified time constant is about one second. It cannot be explained by the heat flow in the classical vertical thermal path, i.e., from the active region to the case and the aluminum plate in our case. In such a phenomenon, the time constant should be of about several milliseconds.

A possible explanation is the lateral diffusion of the heat generated in the active region toward the die border. In this case, the die size involves a width of some millimeters that could be compatible with a time constant of about one second.

As a preliminary conclusion, we think that the surface temperature inhomogeneity could explain the observed overheating and associated observed damages.

So, the tests were continued with a reduce power per die, and a reduced current, using approximately half of the nominal current. In all the cases to avoid any measurement issue, during the continuous current stress, the voltage drop, V_F , is measured after a delay of about 10 min to be sure to reach the steady state.

3.4 BDCT at Reduced Current Level

A new BDCT test has been conducted with a reduce current and only two devices flowed by the current. The following conditions were applied,

Test 2: $I_F = 18 A$, $V_{SG} = 5 V$, $T_p = 45 ^\circ C$, 2 devices flowed by I_F .

In such conditions, to show no clear drift during the 1000 h of the stress. Moreover, the reference device M_0 (HTGB) has similar evolution.

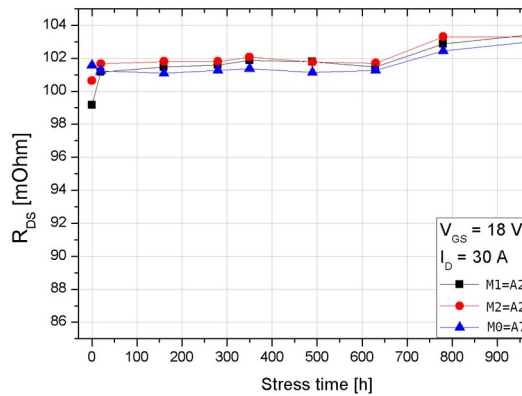


Fig. 1: Evolution of R_{DS-ON} during the BDCT stress, test 2.

So, for a reduced level of current about half the nominal current, I_N , the BDCT stress does not significantly age the DUTs.

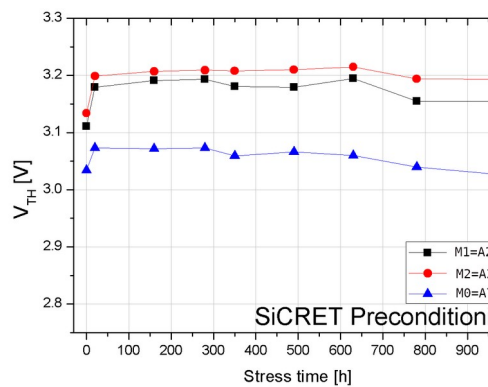


Fig. 1: Evolution of V_{TH} during the BDCT stress, test 2.

Similar results are obtained with devices from manufacturer B. The first 20 stress hours show a slight drift of characteristics: threshold voltage V_{TH} and the resistance R_{DS-ON} increase by about 1% for each manufacturer. As a preliminary conclusion, if the current is reduced, no clear degradation is observed during a BDCT test. To increase the current during the diode stress, in the following, surge current tests are applied.

4 Surge Current Test (BDSCT)

The half-sine wave pulse corresponds to a fairly standard test in the literature. It corresponds to the case of a rectifier on an alternating voltage at 50 Hz with a short-circuited load. In the latter case, the duration of the half-sinusoid is 10 ms. The case of shorter pulse duration i.e., 1 to 4 ms, corresponds to an arm with a load short circuit. The value of the arm capacitance and the wiring inductances defines the pulse duration which is almost sinusoidal.

4.1 BDSCT setup

BDSCT test is interesting to determine the current limits that the device is able to handle, however it is not possible to use this test with higher currents, so the solution is to apply current pulses.

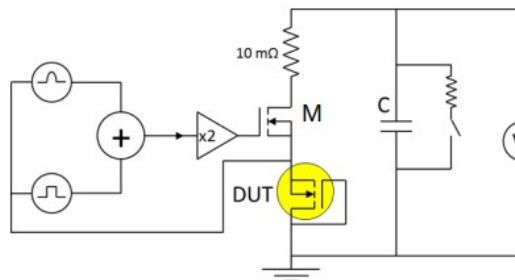


Fig. 1: Schematic of the experimental setup of the BDSCT. The control Power MOSFET, *M*, is a low voltage one (MMIX1F520N075T2, 75 V, 500 A).

and show the surge current test setup. The DUT and the power MOSFETs are placed on an aluminum plate to force the heat dissipation. Four capacitors (100 mF each) are added in parallel with the voltage source to ensure the current demand and to avoid reaching the compliance of the voltage source.

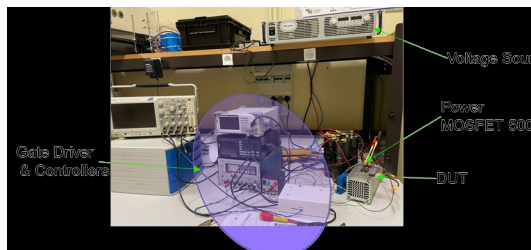
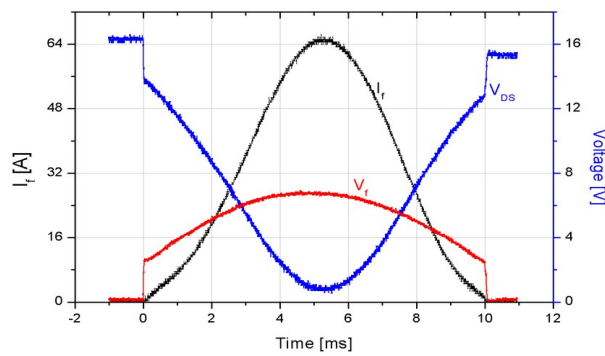


Fig. 1: Surge current test setup

The highlighted part shows the control circuit and drivers are placed inside the white box. shows the current and voltage pulse waveforms. The peak power reaches about 450 W. To avoid the self-heating of the DUT, and to recharge the capacitors properly, pulses are repeated with a period of 4 s.

For a pulse duration of 10 ms, the DUT shows significant degradation for a surge current of $2 I_N ()$. R_{DS-ON} increases by 10 %.

Fig. 1: DUT A183 voltage and current pulse shapes (I_F & V_F)



This parameter change is probably due to local overheating at the contact level leading to critical degradation of the DUT.

It was then decided to reduce the pulse duration to 2 ms: decreasing the pulse duration will lead to the decrease of energy per pulse so, surge currents could reach higher values allowing triggering another degradation mechanism.

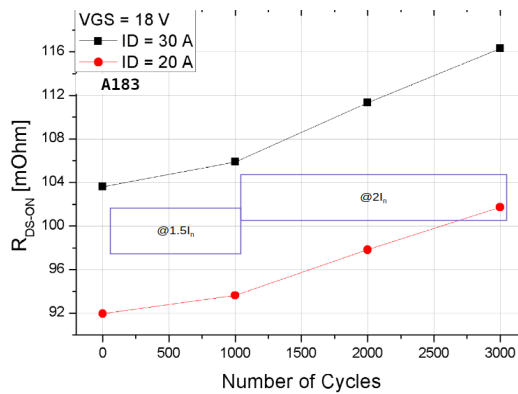


Fig. 1: Evolution of R_{DS-ON} after BDSCT up to $2 I_N$ for long pulse duration (10 ms).

shows that for a pulse duration of 2 ms and a surge current up to $4 I_N$, the DUT does not receive critical degradation. R_{DS-ON} , transfer and body diode characteristics do not drift significantly.

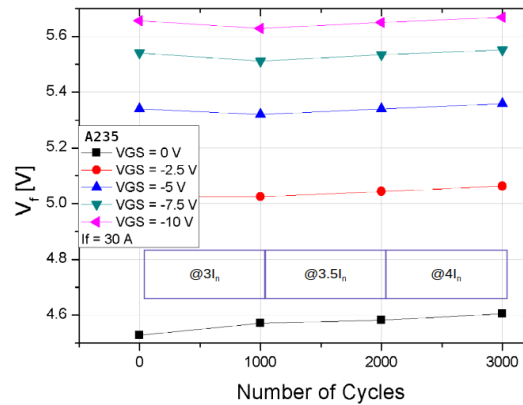


Fig. 1: Evolution of DUT parameters after BDSCT up to $4 I_n$ for short pulse duration (2 ms).

For higher surge current (at $4.5 I_n$ and $5 I_n$), degradation is seen on the device characteristics. At this stage, R_{DS-ON} increases systematically $3.1 \text{ m}\Omega/1000$ cycles (at $4.5 I_n$) and $4.9 \text{ m}\Omega/1000$ cycles (at $5 I_n$).

4.2 First Discussion

For long pulse duration, i.e. the 10 ms test in , some limited degradations are observed even at $2 I_n$. For low peak current values, the observed degradation is very limited. In both cases, that could be interpreted as a packaging issue and overheating that could damage a little, metalizations and connection wires. However, for higher applied peak current, i.e., greater than $4 I_n$, or about 1500 A/cm^2 , body diode and transfer characteristics drift significantly to the right (). These measurements could be explained by bipolar degradation [23] and is related to a high current level [24]. These results are in agreement with the ones obtained recently by Palanisamy [11], for high body diode currents, stacking faults are triggered and could be seen at high current measurements. The BDSCT does not affect the threshold voltage of the body diode and leakage currents which stay constant along the stress. Since a threshold in the current peak level, about $4 I_n$, has been observed, it is a **strong indicator** that bipolar degradation occurs in such a condition.

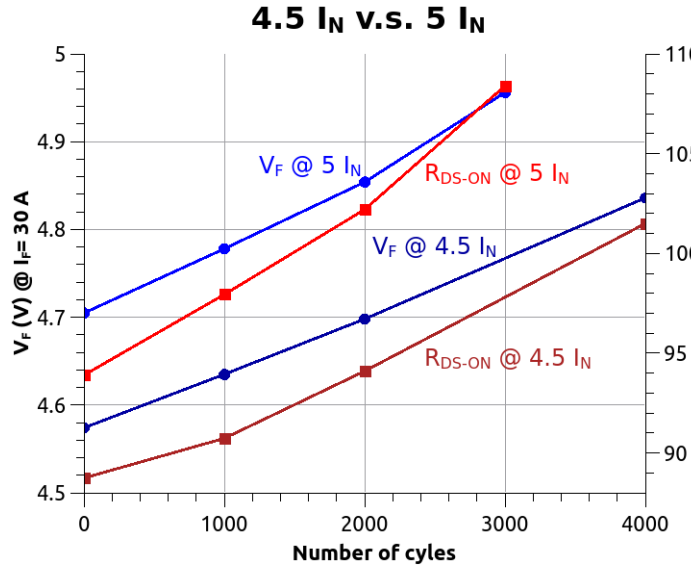


Fig. 1: Comparison for V_F and R_{DS-ON} between 4.5 and 5 I_N BDSCTs. In blue, the 5 I_N BDSCT applied for A237 and in red the 4.5 I_N BDSCT applied on A238.

5 Discussion and Conclusion

To summarize, in this paper two methods have been studied to test body diodes: the continuous conduction (BDCT) and the surge current (BDSCT). The measurement of the drop voltage across the body diode in the first seconds of the application of the continuous current, measured in , clearly shows that a self-heating phenomena occurring in the device and because of the negative current/temperature coupling, it yields to a inhomogeneity of the surface temperature and probably to some overheating locally that could damage the device. This overheating phenomenon could not be related to a vertical thermal path because in this latter case the time constant should be much lower, about tens of milliseconds. So, BDCT must be applied for a reduced current level, about the half of the nominal current. Consequently, BDCT tests have a limited interest to study the body diode reliability.

However, for a reduced current level ($\sim I_N/2$) no clear degradation was observed. One option is to apply a pulsed current stress instead of a continuous current stress, but it will be further difficult to implement, particularly for several components connected in series.

Surge current stresses or BDSCTs yield an easier way to stress the body diodes. For great time duration, i.e. 10 ms, a weak metalization degradation is observed at nominal current.

For shorted pulse duration, i.e., 2 ms, the bipolar degradation could be observed at a high current level, about five times the nominal current.

Further measurements should be performed for a deeper analysis of each technology, but the methodology is more clearly defined with BDSCTs. Moreover, a better analysis of the test condition must include an accurate electrothermal modeling of the DUT, to reach to a good estimation of the junction temperature during the stress tests. Finally, and with respect to the initial issue of the use of the body diodes, no strong degradations occur if the peak current does not exceed approximately 4 times the nominal current.

Acknowledgements

This paper was carried out in the framework of the IRT Saint Exupery project SiCRET (SiC Reliability Evaluation for Transport). We acknowledge the financial support from the SiCRET industrial, and academic members and the financial support from the French National Research Agency (ANR).

SiCRET Industrial members: Alstom, Alter Technology, Emotors, Liebherr, Nucleudes, Safran, SuperGrid

Institute, Thales, Vitesco Technologies.
SiCRET academic members: Ampère, LAAS, IES.

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