Impact of the Printed Circuit Board Geometrical Design on the AC Breakdown and Partial Discharge Activity in Air

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***Abstract* – The main objective of this paper is to study the voltage withstand characterization of Printed Circuit Board (PCB) substrates for the development of three-dimension (3D) power modules. Classical power electronics gel encapsulation is substituted by air encapsulation in order to benefit of dielectric and thermal cooling aspects. Breakdown voltage (BDV) and Partial Discharge (PD) measurements are studied for the voltage withstand characterization with different geometrical designs of the two-side metallization of PCBs. BDV measurements are performed with classical alternative (AC) voltage constraints. Next, PD Inception Voltage (PDIV) is assessed for each PCB design with an AC constraint and a classical power electronics square voltage constraint, i.e. high switching frequency and dV/dt. Experimental results showed no PCB material degradation during BDV events and underlined a breakdown path across PCB surface into the air. The increase of two-side metallization creepage distance allowed a linear increase of BDV, while geometrical PCB design is less sensitive for PDIV values.**

I. INTRODUCTION

For power electronic applications, the introduction of Wide-Band Gap (WBG) semiconductors components give the possibility to design and implement high power density converters in the range of tens of kW/L [1]. Although high power density reduces size, weight and cost of the converters, some drawbacks like thermal management and voltage withstand need to be considered as they represent the main challenges of current and future high power density converter integration [2].

Three-dimension (3D) power modules with double-side cooling and Printed Circuit Board (PCB) embedding WBG semiconductors represent one possible integration solution for higher power density [3]. PCB with embedded dies like in Fig. 1, constitute the elementary switching cell structure of power electronic converters. The PCB dielectric material (FR4) ensures the volume voltage withstand of dies potentials but the electric field constraints are reported at the edge of the PCB (area represented by the gray arrows in Fig. 1).

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Therefore, with air encapsulation of elementary switching cells and associated low dielectric rigidity, this area needs to be considered regarding voltage withstand issues.

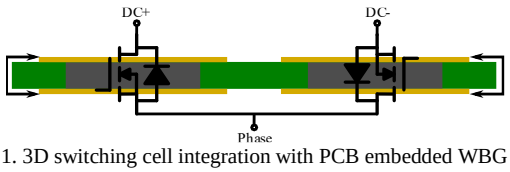

Fig. 1. 3D switching cell integration with PCB embedded WBG dies

Thus, this paper proposes to study the impact of geometrical PCB design with air encapsulation. The next section will present breakdown voltage measurements (AC BDV) of PCBs with alternative (AC) voltage constraint. Then, Partial Discharge (PD) activity of different PCBs designs will be presented with AC and square voltage constraints.

II. EXPERIMENTAL SETUP

A. PCBs Design and Test Vessel

This study is focused on the effect of copper pad to copper pad distance between two sides at the edge of the PCB. Different PCB configuration are realized for the tests (Fig. 2). Each sample consists of identical 50x40mm FR4 footprint with different double-side 35µm copper thick metallization for a total PCB thickness of 1.6mm. Three different copper pad sizes are considered to make symmetrical or asymmetrical PCB designs. Geometrical dimensions are given in TABLE I. Finally, six different PCBs are considered with respectively three specimens by design for the tests.

Fig. 3 represents the experimental test vessel. For both AC BDV and PD tests, the PCB is inserted between two 12.5mm diameter spheres electrodes respectively connected to high voltage and ground potentials.

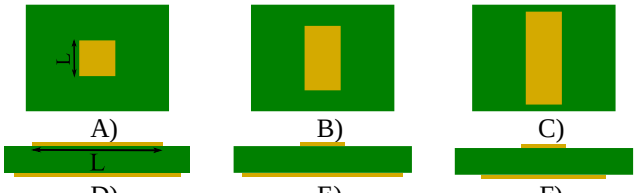

Fig. 2. PCB design with A), B), C) symmetrical (top view) and D), E), F) asymmetrical configuration (front view)

TABLE I
DIFFERENT PCB DESIGNS (ALL METALLIZATION WIDTHS = 12.5MM)

Design	A	B	C	D	E	F
Top side metallization L_T [mm]	12.5	23.5	36	23.5	12.5	12.5
Bottom side metallization L_B [mm]	12.5	23.5	36	36	36	23.5

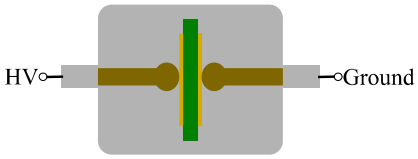

Fig. 3. BDV and PD test vessel

B. AC Breakdown Voltage Measurement

AC BDV measurements are performed with an industrial breakdown tester (BAUR DTA 100C) under 60Hz AC voltage with a 2.5kV/s rising speed. When the voltage rises, the breakdown is automatically detected and the voltage is stopped. Each PCB sample is subjected to a series of 20 consecutive BDV measurements.

C. Partial Discharges Detection with AC Waveform

PD measurements in AC are performed in compliance with IEC 60270 standard recommendations using an Omicron commercial system. The setup has been used in previous team works like in [4]. A computer-based voltage controller and an audio amplifier provide a wide range of fully reproducible voltage. The high voltage is obtained by a PD free elevating transformer that provides voltage up to 25 kV_{RMS}.

For the PD Inception Voltage (PDIV) measurement, each sample is submitted to a slowly (0.05kV/s) linearly increasing voltage until the PDIV is reached with a 10pC threshold. The measurement is repeated 6 times, with 3s waiting time between two consecutive PDIV, and the average of the last 5 represents the PDIV of the sample.

D. Partial Discharges Detection with Square Waveform

An unipolar 25kV_{max} / 10kHz square voltage is generated thanks to a half bridge as shown in Fig. 4. The chosen duty cycle is 25% and the switching speed on the device is about 10kV/µs. Due to difficulties to make a conventional PD detection with square voltages, a Photo Multiplier Tube (PMT) is used as PD detector [5]. In Fig. 5 are depicted the square voltage and the PMT signal when a PD occurs. A comparison with the electrical PD detection in AC has shown that the optical PD detection has a threshold about 10pC. This preliminary test cannot be used as a calibration test, but it gives a sensitivity to the optical measurement. The PDIV measurement is performed like in AC, with a slow increase of the maximum value of the voltage until a PD occurs. The measurement is repeated 6 times and the average of the last 5 represents the PDIV of the sample.

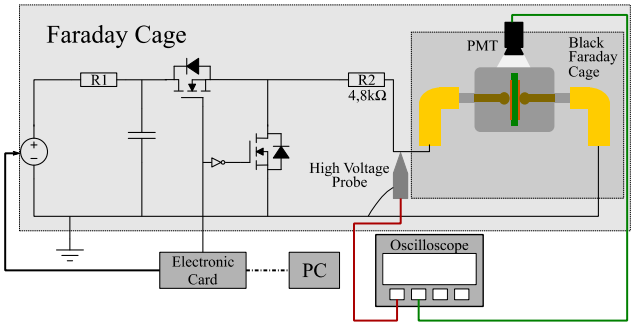

Fig. 4. Experimental test bench for PD activity measurement with square power electronics constraint

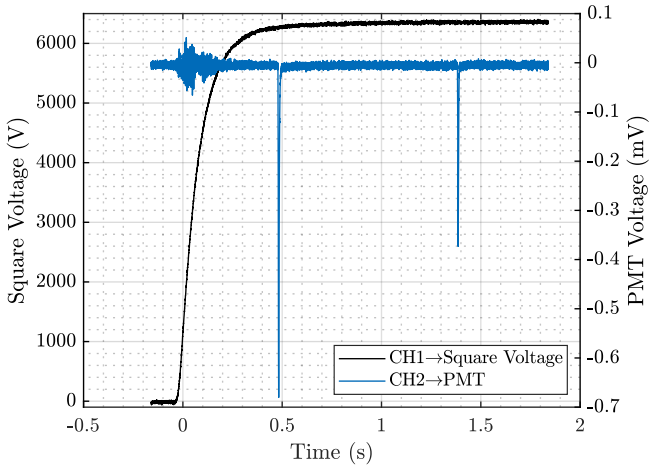

Fig. 5 : PMT signal and square voltage waveform

III. BREAKDOWN VOLTAGE MEASUREMENTS

AC BDV experimental results are represented in Fig. 6 for the different PCBs designs of TABLE I. It can be seen that no decrease trend is observed on every 20 consecutives BDV measurement. Therefore, in case of fast fault current stop (10µs switch off time), it can be stated that breakdown always occurs in air, i.e. with atmospheric conditions and with no PCB surface degradation.

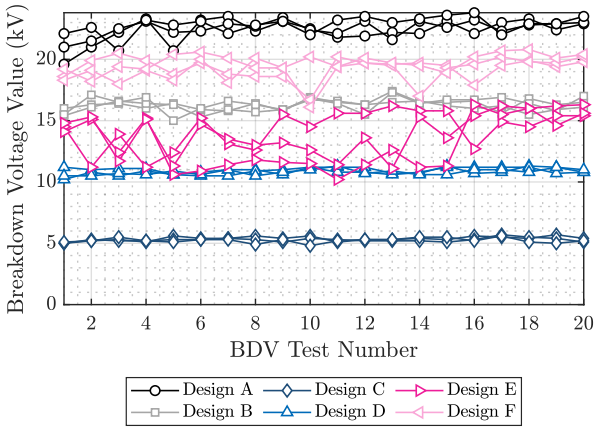

Fig. 6. Consecutive BDV measurements of all PCB designs (one curve represents one specimen of each design)

To enable comparison, the overall mean values over the 60 BDV measurements per design (20 BDV of 3 specimens per design) are considered. For each design, the length between copper pads constitutes the creepage distance. The lowest obtained breakdown value is 5.2kV for 5.5mm and the highest one is 22.6kV for 29 mm. In Fig. 7 is depicted the evolution of the average BDV results (with the standard deviation) of each design and point out a global linear behavior as a function of the creepage distance.

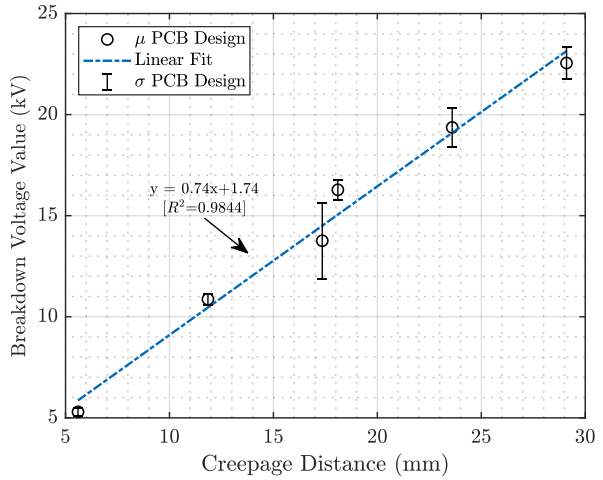

Fig. 7. Breakdown voltage as a function of the creepage distance and associated linear regression

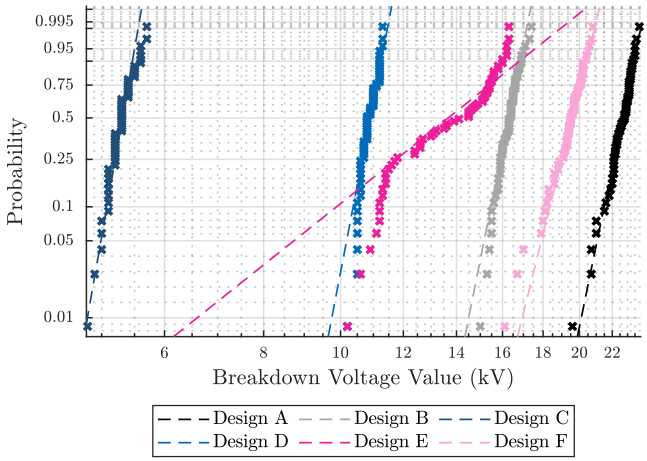

Fig. 8. Weibull distribution of all PCB designs BDV measurements

As far as converter design rules are concerned, breakdown must be avoided. Thus, experimental BDV results can be fitted with the Weibull distribution to obtain BDV values especially at low probability levels [4]. Fig. 8 represents the Weibull fit results for all designs and TABLE II summarizes the BDV values at different probability levels, i.e. 0.1%, 1% and 63.2%. From the results it can be noticed that: a) design E does not fit well the Weibull distribution, b) except for design E, all the fit curves have similar slopes suggesting a linear dependency of the BDV with the creepage distance for all the risk levels, c) the high value of the slopes underlines the relatively small difference in the BDV between all the risk levels (depending on the design, minimum 16% and maximum 21% decrease between 63.2% and 0.1% risk level).

TABLE II
BDV AT DIFFERENT RISK LEVELS FOR ALL DESIGNS

Design	Creepage Distance [mm]	BDV [kV]		
		Risk Level		
		0.1%	*1%*	*63.2%*
A	29.1	18.83	20.1	22.9
B	18.1	13.63	14.5	16.5
C	5.6	4.54	4.8	5.4
D	11.85	9.18	9.77	11
E	17.35	4.44	6.6	14.6
F	23.6	15.68	16.9	19.8

IV. PARTIAL DISCHARGE ACTIVITY

A. *AC Partial Discharge Experimental Results*

Fig. 9 shows the rms value of the mean PDIV at 10 pC for each design specimens. Remember that the creepage distance decreases from design A to C and increases from design D to F. In preliminary tests with samples immersed in a dielectric fluid, the absence of PDs under an AC voltage above 5kV showed that PDs always occur on the PCB surface. Due to the disparity between each specimen, it is impossible to consider the overall mean values per design like for the AC BDV comparison. However some trends can be underlined: a) no evidence of the PDIV dependence on the creepage distance, b) the sample design (symmetrical vs asymmetrical) plays the main role on the PDIV, c) the PDIV is generally lower for asymmetrical design than symmetrical ones.

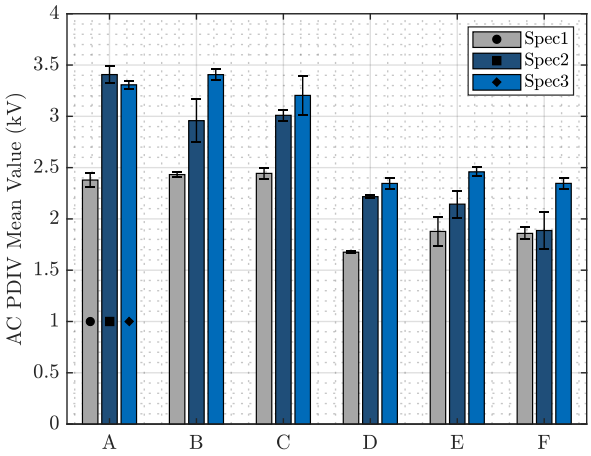

Fig. 9. AC PDIV mean value of each design specimens

B. *Square Voltage Partial Discharge Experimental Results*

Experimental PDIV detection results of unipolar square voltage constraint are depicted in Fig. 10. With an increase of only 5% for a factor 5 on the creepage distance, symmetrical designs PDIV are faintly sensitive to the metallization distance. The same observation can be made for asymmetrical designs but with a lower value of the PDIV.

With the results of Fig. 9 and Fig. 10, PDIV for both AC and unipolar square voltage constraints can be compared with peak-peak amplitude as mentioned in [5]. This comparison is summarized in TABLE III.

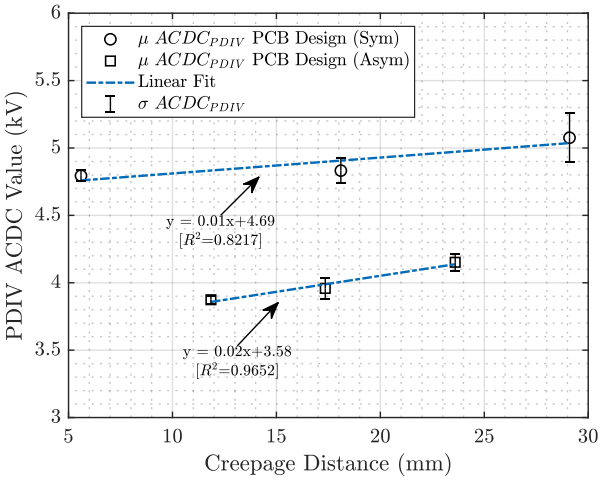

Fig. 10. Square voltage PDIV detection results as a function of the creepage distance and associated linear regressions

TABLE III
AC AND SQUARE VOLTAGE PDIV COMPARISON BASED ON PEAK-PEAK VALUES (CONSIDERING *SPECI* OF EACH DESIGN)

Designs	Square PDIV [kV]	Peak-Peak AC PDIV [kV]	Differences (Square VS AC)
A	5.08	6.73	- 25%
B	4.83	6.88	- 30%
C	4.79	6.91	- 31%
D	3.87	4.74	- 18%
E	3.96	5.31	- 25%
F	4.15	5.26	- 21%

Results show that in the experimental context and with the protocol previously defined, the PDIV is higher in AC compared to square waveform with a difference comprises between 18% and 31%.

V. DISCUSSIONS

From both AC and square PD measurements it can be observed a major PDIV dependence on the design (symmetrical/asymmetrical) than the creepage distance. This can be due to the back-side PCB metallization effect on electrical field configuration. Indeed, as the PD activity is largely dependent on field amplitude at triple point localization, modification of geometrical design at this location can totally change PDIV behavior. Authors of [6] have studied this effect with the modification of the offset metallization (Top and Bottom side triple point distance) on Direct Bonded Copper (DBC) substrates and found an impact on PDIV behavior. Future numerical simulations with PCB structure need to be carried out to explain these trends.

VI. CONCLUSION

In this paper, the impact of the PCB geometrical design on the breakdown voltage was studied with an AC voltage constraint. Experimental results have shown that breakdown path always occur in the air with no PCB material degradation. An increase of 5 times the creepage distance between the metallizations leads to an increase of 4 times the BDV value. A linear behavior of BDV with creepage distances is deduced at different risk level according to experimental results and Weibull distributions.

PDIV detection in AC and square voltage constraints was also discussed. PDIV is less sensitive to the creepage distance, with slight sample differences, than to the relative position of the triple points. A grounding metallization surface higher than the high voltage metallization seems to lower the PDIV.
Electrostatic simulations are therefore required for deeper analysis.

Finally, it was observed that increasing the creepage distance has a greater relative impact on BDV than on PDIV. However, as BDV characterizations were made with AC constraints, further work is required with square voltage constraints and the need for a dedicated experimental test bench.

ACKNOWLEDGMENT

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