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SiC integrated circuits for smart power converter

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Abstract.

The limits of the current electronic solutions based in silicon, restrict the use in harsh environments especially in high temperature (>300 °C). SiC is a material, which allows exceeding these physical constraints. For this purpose SiC integrated circuits based on lateral MESFET have been developed. First steps of the development of smart integrated driver circuit dedicated to harsh environment are presented. Three functions: amplifier, ring oscillator and comparator have been designed, manufactured and characterized.

Keywords: SiC, Integrated circuits, MESFET

1. Introduction

This article is an extended version of a paper presented at IEEE CAS 2017 [1]. A power electronic technology able to operate in harsh environment and especially at high temperature (> 300 °C) is more and more important mainly in the fields of drilling, transports and aerospace. Present solutions based on the silicon technology are limited at temperature higher than ~200°C. This is due to the low bandgap of silicon (1.12 eV) which is responsible for the rapid increase of leakage currents with temperature. A solution is the use of technology based on Wide Bandgap semiconductor such as silicon carbide (SiC). The ability of SiC devices for operating in high temperature environment has been already demonstrated, and limitations of unipolar controlled switches due to the thermal runaway have been discussed [2, 3]. Some research laboratories work on SiC integrated circuits in the purpose to develop specific circuits working at high temperature and/or other harsh environments. The NASA has tested a 4H-SiC circuit based on JFETs up to 961 °C [4]. Some other technologies as BJT and CMOS have respectively operated at 500 °C [5] and at 300 °C [6]. The different demonstrators concern analog and logic functions, which in general are not dedicated to integrated power circuits. The purpose of this paper is to present a SiC technology for a smart integrated power driver, which could operate at high temperature. This driver will be entirely fabricated in SiC, to be co-integrated with the power device. The driver will add several smart functions as logical control, stage of power for feeding the current gate, electrical protections, sensing and monitoring functions. Fig. 1 presents the concept of this smart driver.

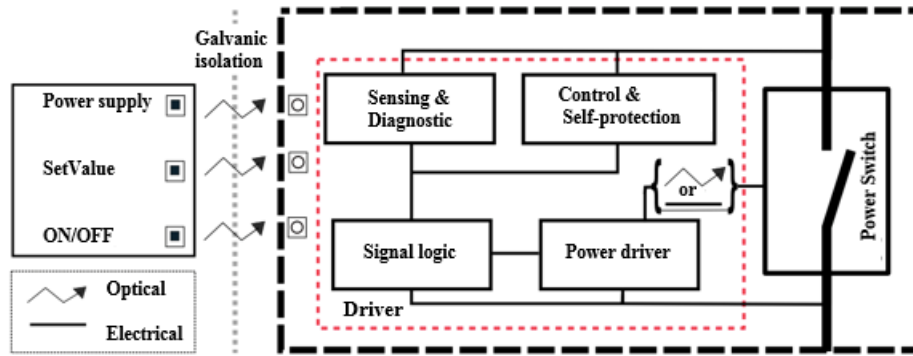


Fig. 1. Concept of the smart integrated power driver in SiC for harsh environment.

2. SiC integrated circuit technology

AMPERE laboratory have designed and characterized a SiC integrated circuit technology based on lateral dual-gate MESFET (Fig.2) [7]. The device is driven by two gates labeled G_1 and G_2 . G_1 is a Schottky gate and G_2 is a bipolar gate. Two layers (N and P) constitute the MESFET on a semi-insulating layer. A N layer, which has a doping level at $N_d \sim 10^{17} \text{ cm}^{-3}$ and a P layer at $N_a \sim 10^{15} \text{ cm}^{-3}$. This topology allows to consider the control of the MESFET by three ways: G_1 , G_2 and G_1 - G_2 .

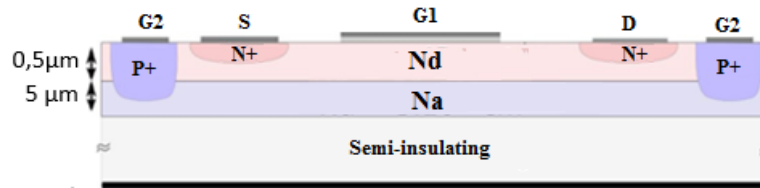


Fig. 2. Cross-view of a lateral dual-gate MESFET topology, which has been used for the integrated circuit technology in SiC.

A Spice model has been established for the sizing of the MESFET devices. Three types of MESFET have been designed, fabricated and characterized. Fabrication of the 4H-SiC prototypes has been at the National Center of Microelectronics of Barcelona [8]. Experimental results have shown that these devices are operational. Each type of MESFET is dedicated to a range of electrical power (signal, buffer and power circuits). The aim purpose is the development of an integrated power circuit entirely in SiC. Based on this technology, a hybrid medium power converter and its driver have been designed as demonstrator [9] and is shown in Fig. 3. This demonstrator is designed for a power of 40 W. The boost converter is composed of a logic-control part and a power-one. All components, except the passive elements are integrated on the same SiC substrate. D_1 , D_2 , D_3 and D_4 are lateral Schottky diodes. The power diode is a lateral Schottky structure designed for a direct current of 660 mA. The driver SiC is based on MESFET structures used for the two stages: signal and buffer. The power device of the converter is the Power MESFET. The topology of the dual-gate Power-MESFET allows to apply a parallel signal to regulate the power system.

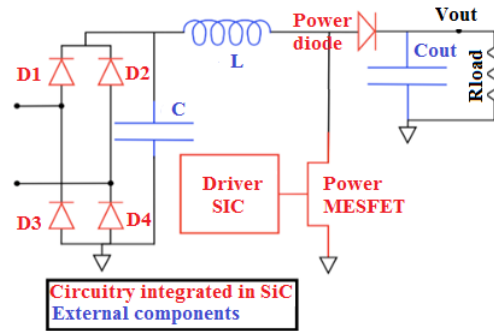


Fig. 3. Hybrid boost converter considered for the demonstrator of the SiC technology.

The technological innovation of this SiC process resided in the interconnections of the metallization for the lateral devices. For example, Fig. 4 presents the electrical schematic (high) and a cross section (low) of a common source amplifier designed from the IC-SiC technology. This circuit is constituted by a n-type resistor R (labels: A-D, Fig. 4) and by a lateral MESFET M (labels: D-G-S, Fig. 4). The metallization interconnection located close to the label D (cross view, Fig. 4) is one key for the IC-SiC process. If the amplifier is working, it will mean that the interconnection is efficient and the technological principle is validated.

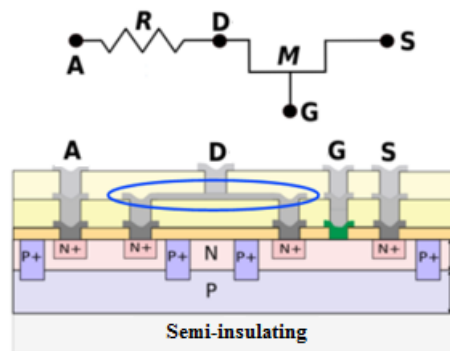


Fig. 4. Electrical schematic and cross section for a common source amplifier circuit manufactured with the SiC process for integrated ic and cross section for a common source amplifier circuit manufactured with the SiC process for integrated circuits.

3. Design and simulation of the electronic SiC functions

A demonstrator based on the concept of Fig. 3 has been designed (Fig. 5). To realize this demonstrator several elementary functions were necessary to be considered (Table 1). The design for these electronic functions has been established from specific Spice models developed for the SiC lateral MESFET. The description of this Spice model is detailed in [7].

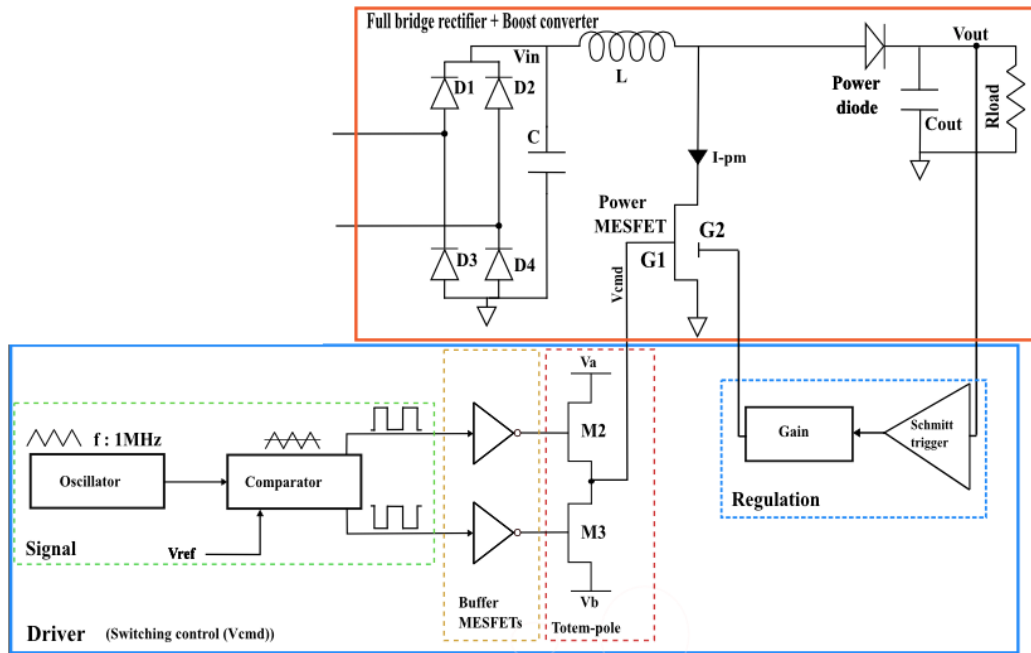


Fig. 5. Synoptic of the considered demonstrator based on IC in SiC. The bottom block is the driver circuit. The top block is the power circuit.

Table 1. Synthesis of the main functions based on the lateral MESFET technology for the demonstrator.

<i>Electronic function</i>	<i>Role in the integrated circuit</i>
Comparator	Set the duration of the control signal
Amplifier	Use for voltage gain
Oscillator	Generate the clock of the system
VCO	Change the frequency of a signal in function of the input voltage (for the regulation)
Schmitt-trigger	Set two voltage thresholds. Useful for the regulation of the current and the output voltage
Totem-pole	Current gain for supplied the gate of the power device

The design of these electronic functions is complex because the used lateral MESFET is only available in n-type channel conduction and it is a normally-on device. It means that a negative voltage between the gate and the source of the MESFET is needed to block the device. This constraint involves the development of electronic functions, which are adapted for the normally-on MESFET topology. The design of the oscillator, the comparator and the Schmitt-trigger have been presented in [9]. The experimental measurements and analysis of the amplifier, the ring oscillator and the comparator will be presented in this article in the next part.

4. Experimental results

A. The amplifier circuit

The design of the amplifier is based on the serial association of a resistor (R_{1o}) and a MESFET. The topology is the amplifier common source circuit (Fig. 6).

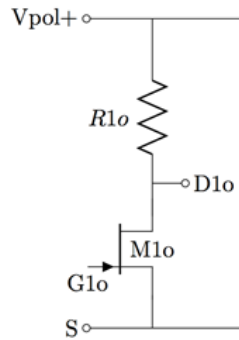


Fig. 6. Electrical schematic of the the common amplifier source based on the normally-on MESFET, with the integrated resistance $R_{1o} = 18 \text{ k}\Omega$.

The experimental values are presented in Fig. 7. V_{pol} is set at 20 V and a sinusoidal signal with an offset of -3V, an amplitude voltage of 2 V and a frequency of 4 kHz is applied on the gate of the MESFET. The circuit can be considered as operational because the drain voltage D_{1o} presents the expected signal form. The measured gain is ~ 0.2 , which is far lower than the predicted value 10. This difference can be easily explained by the electrical characteristic of the signal MESFET [6]. The experimental measurements have shown that the contact resistance of the MESFET was more important ($\# 5 \text{ }\Omega/\text{mm}$) than expected and the threshold voltage (V_{TH}) much higher (14 V) than those of the preliminary fabricated batch (10 V). These differences involve a shift of the bias point outside the linear area of the signal MESFET. The gate-source voltage (V_{G1o}) must be between -8 V and -10 V according to the spice simulation (Fig. 8) or the circuit cannot work for a V_{G1o} less than -6 V. This shift explains the low value of voltage gain. These technological parameters of the MESFET could be easily improved for the next manufactured batch by the optimization of the contact resistance and a reduction of the height of the n-type epitaxy layer (reducing the V_{TH}). Thus, the circuit would present expected electrical performance near of those intended by the design.

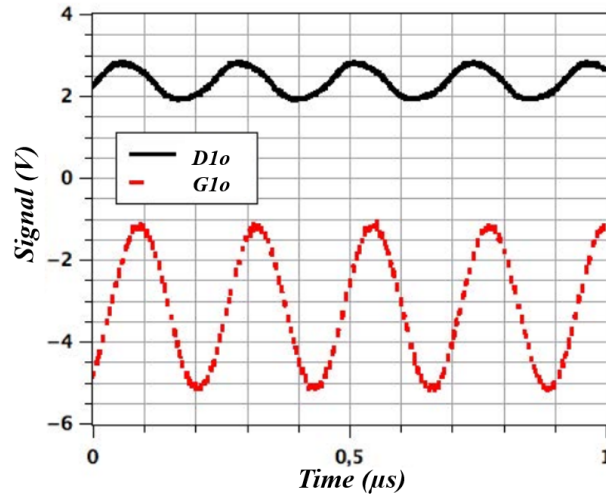


Fig. 7. Experimental measurements of the amplifier circuit, the red dotted line represents the input signal apply on the gate $G1o$ and the continuous black line is the output signal located at $D1o$.

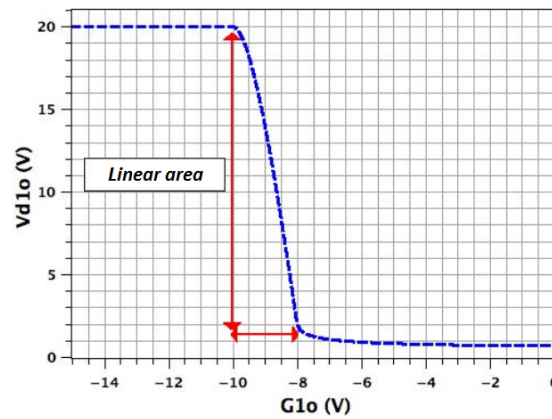


Fig. 8. Spice simulation used for the sizing of the amplifier circuit with the integrated resistance $R_{1o} = 18 \text{ k}\Omega$ in function of the voltage $G1o$ applied on the gate G_1 of the MESFET.

In conclusion, the common amplifier source is working that means that the electrical interconnection between the resistor and the MESFET is performed (Fig. 4). These experimental results validates the principle of the SiC integrated circuit technological process. However, the technological process must be improved to optimize the performance of the circuit.

B. The ring oscillator

The ring oscillator is made of three MESFETs (Fig. 9). The design of this function and the preliminary results have been presented at CIPS [9]. For this first oscillator, the used SiC MESFETs were discrete devices. The current oscillator is based on three integrated transistors. Fig. 10 presents the manufactured integrated ring oscillator. The circuit has been designed with five MESFETs and five drain resistances for redundancy.

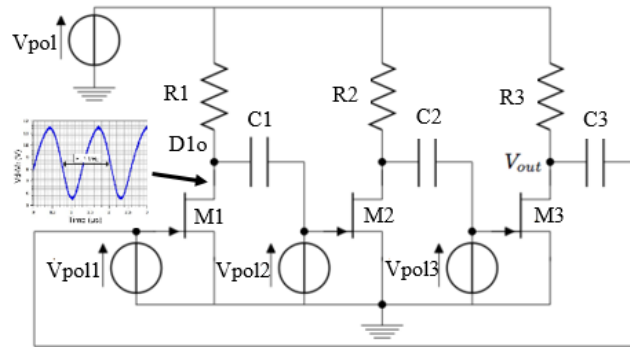


Fig. 9. The ring oscillator functions with 3 N-MESFETs, $R_i = 18 \text{ k}\Omega$, $C_i = 33 \text{ nF}$, $V_{pol} = 20 \text{ V}$, $V_{pol1} = -9 \text{ V}$, $V_{pol2} = -9 \text{ V}$ and $V_{pol3} = -9 \text{ V}$

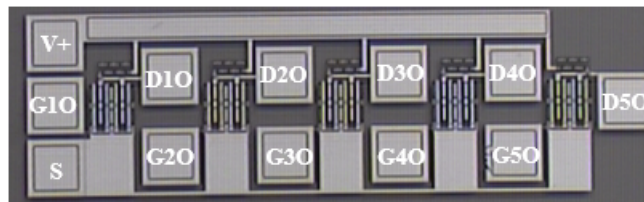


Fig. 10. The manufactured ring oscillator with five MESFETs and five drain resistances. “V+” is the common bias pad of the circuit. “S” is the common source pad.

Fig. 11 shows the integrated function, which has been manufactured, has been inserted on a package DIL24 with silver lacquer attachment. Gold bonding wires with a diameter of $50 \mu\text{m}$ have been used for the electrical connections. The circuit is working at the expected frequency (Fig. 12 – 1 MHz). The circuit was polarized with $V_{pol} @ 20 \text{ V}$ (drain of the MESFETs) and V_{pol1} , V_{pol2} , $V_{pol3} @ -9 \text{ V}$ (gate-source of the MESFETs).

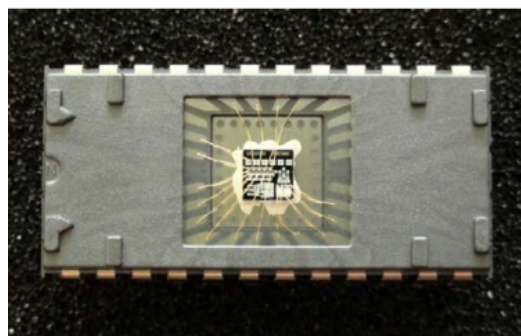


Fig. 11. Picture of the integrated ring oscillator with bonding wires on a package DIL24.

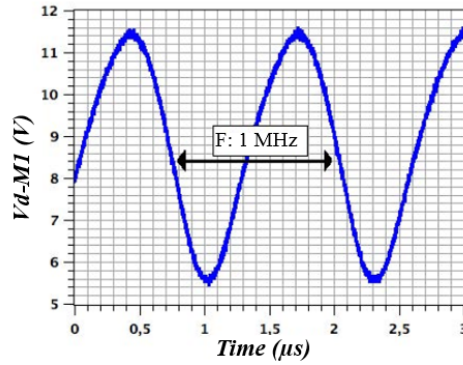


Fig. 12. Experimental measure of the ring oscillator. The V_{d-M1} is the voltage of the drain for the MESFET M_1 (Fig. 8).

The MESFETs have a topology with a dual-gate. This topology gives a particularity to the ring oscillator because it is possible to control the oscillating frequency from the voltage applied on the second gate of the MESFETs (G_2). The behavior between the frequency and the voltage is linear between 750 kHz and 1 MHz. It means that with this dual gate, the ring oscillator can be used as a Voltage Control Oscillator (VCO) circuit (Fig. 13).

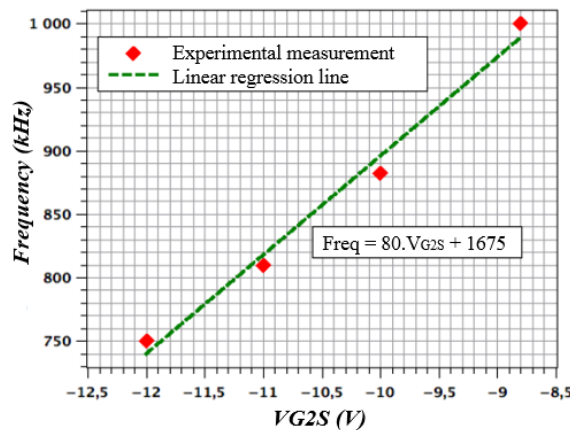


Fig. 13. Variation of the oscillating frequency depending on the polarized voltage, which is applied on the gate G_2 of the MESFETs.

This specific property of the ring oscillator is related to the topology of the dual-gate MESFET (Fig. 2). Indeed, the MESFETs are controlled by the voltage which is applied on the gate G_1 and the source. This voltage modulates the channel of the transistor by the presence of a space charge region (SCR). Increasing the voltage V_{G1S} will increase the SCR area layer is the space charge area (Fig. 14).

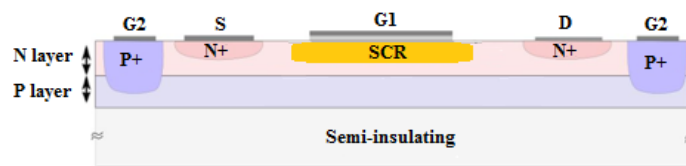


Fig. 14. Cross-view of the dual-gate MESFET, which presents a space charge region (SCR) related to the voltage applied between the gate G_1 and the source.

The MESFETs can be also controlled by the gate G_2 . It is not possible with this gate to block the MESFET but it is possible to modulate the space charge area of the channel. The control of the voltage V_{G2s} allows to modulate the channel thickness thanks to the buried P layer. The decrease of the channel thickness involves a decrease of the threshold voltage V_{TH} for blocking the MESFET. The decrease of V_{TH} reduces the time required for blocking transistors, which leads to a decrease in the frequency of the oscillator (Fig. 15).

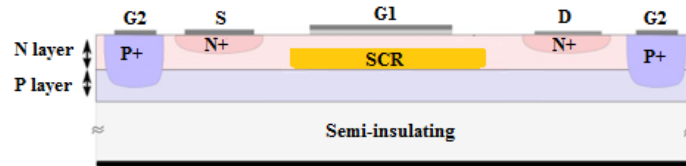


Fig. 15. Cross-view of the dual-gate MESFET, which presents a space charge region related to the voltage applied between the gate G_2 and the source.

In conclusion for the ring oscillator, this function is working and can be used as a VCO thanks to the polarization of the gate G_2 .

C. The comparator circuit

As indicated in the design part, the working of this circuit has been already presented [9]. Here after we present the principal elements in order to compare them with the characteristics of the others presented functions. This comparator circuit is based on MESFETs differential pair ($M1_{tr}$ and $M2_{tr}$), $M3_{tr}$ and $R3_{tr}$ are a current sink circuit for supplying a constant current ($360 \mu A$) to the differential pair. $M4_{tr}$, $M5_{tr}$, $R1_{tr}$, $R2_{tr}$, $R4_{tr}$, $R5_{tr}$ are designed for imposing a drain current on each branch of the differential pair circuit. Fig. 16 and Fig. 17 present respectively the electrical schematic of the comparator and the manufactured circuit.

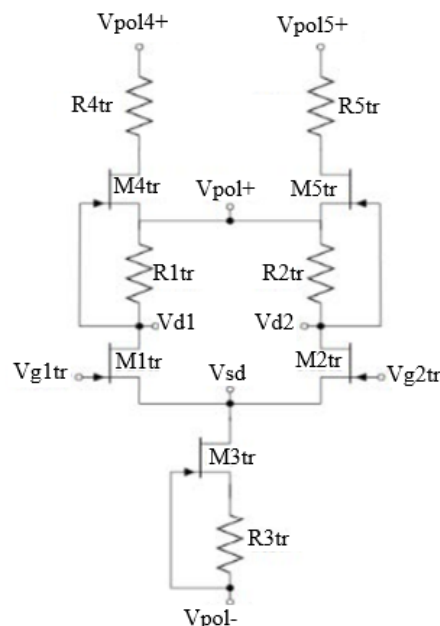


Fig. 16. Electrical schematic of the comparator circuit made of five signal MESFETs and five integrated resistors, whose the value is $10 \text{ k}\Omega$.

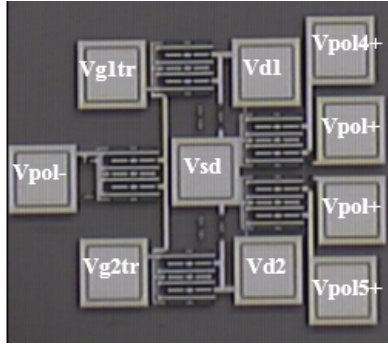


Fig. 17. Manufactured circuit of the comparator circuit made of five signal MESFETs.

The electrical characteristics of this circuit have been measured from a system using a probe card presented in the Fig. 18. The probe card has been designed according to the geometry of the photolithography mask levels used to fabricate the comparator circuit. The classical power supply generates the bias (V_{pol+} , V_{pol-}) and the reference signal (V_{ref}) applied on the gate V_{g2tr} . The input signal (V_{in}) is generated by a Low Signal Generator (LSG) and applied on the pad V_{g1tr} . Finally, the output signal is displayed on the oscilloscope thanks the measures of the pad V_{d1} and the pad V_{d2} .

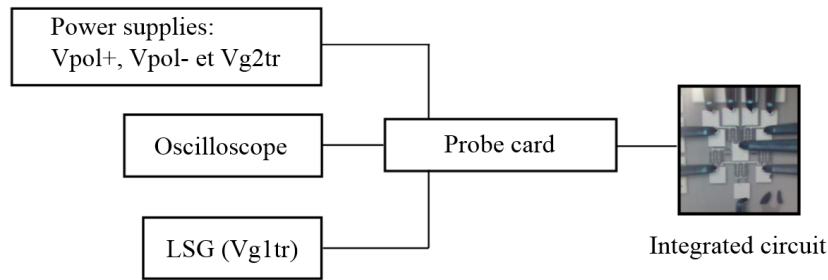


Fig. 18. Synoptic of the experimental bench for the electrical characteristics of the comparator circuit. The measurements are directly performed on the wafer thanks the probes card.

The Spice simulation of the comparator is presented in Fig. 19. The output signals switch (V_{d1} and V_{d2}) when the signal V_{in} becomes higher or lower than the signal V_{ref} . The signal of the outputs are complementary. If V_{d1} is high then V_{d2} is low and vice versa. The circuit has the typical behavior of a comparator.

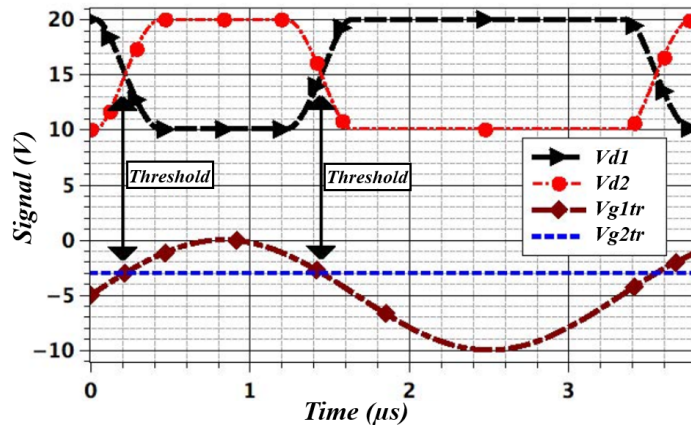


Fig. 19. Spice simulation of the comparator circuit.

The experimental results are indicated on the Fig. 20. From the results it appears that, the circuit has the capacity to compare the both input signals. However, as for the amplifier circuit, the output signal does not match with the expected signal from the spice simulation. Two hypotheses can be considered to explain the result.

The first hypothesis is in the same way than for the amplifier, where the technology parameters of the MESFETs influence the bias point by shifting. Moreover as indicated, the threshold voltage of the device is more important (-15 V against -10 V). This parameter is important because it means that the MESFETs are not totally blocked for the initial V_{TH} voltage. The no blocking of the devices involves a bad balancing between the drain current for the MESFETs of the differential pair. A spice simulation with the parameter V_{TH} at -15 V shows a signal form, which is near of the experimental we measured (Fig. 21).

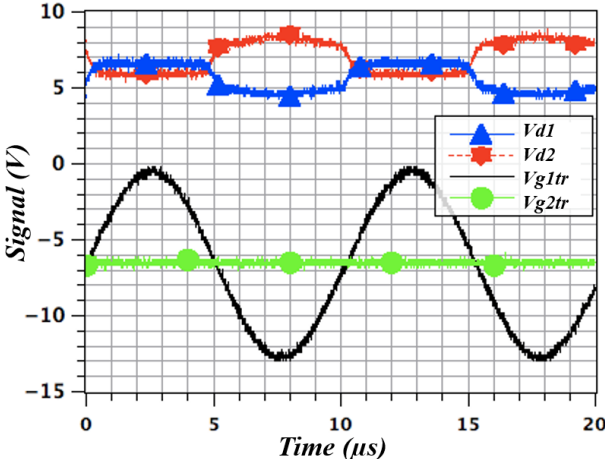


Fig. 20. Electrical characterizations of the comparator by the comparison of sinusoidal signal with a constant voltage.

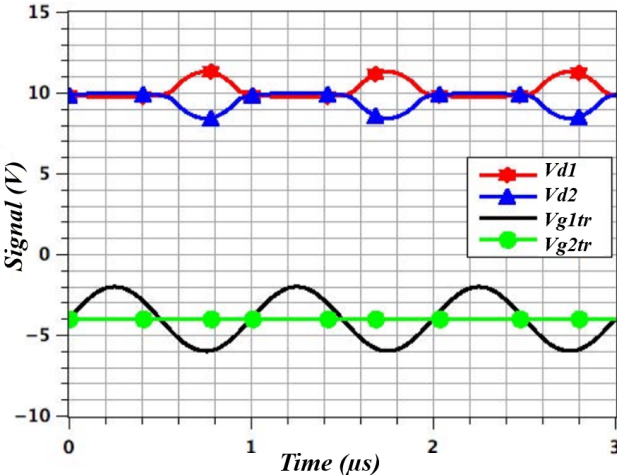


Fig. 21. Spice simulation with the parameter V_{TH} of the MESFET model at the value of -15 V.

The second hypothesis would be related to the delivered current sink circuit (Fig. 22), which was not constant and at the expected value of 360 μ A, directly involving the working behaviour of the circuit.

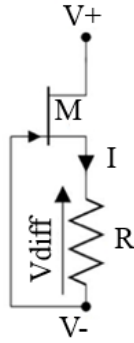


Fig. 22. Electrical schematic of the current sink source used for the comparator circuit with $R = 50 \text{ k}\Omega$.

This hypothesis has been validated by the display of the voltage signal of current source. The signal is represented on the Fig. 23. The value of the V_{diff} voltage and the resistance give an estimated value of the current sink with a magnitude of $220 \mu\text{A}$ (37 % with the expected value).

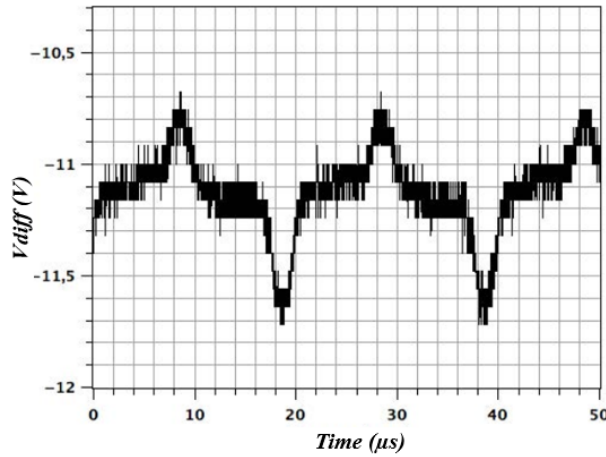


Fig. 23. Experimental measurements of the current sink circuit.

In summary, the topology of the comparator is operational but it needs to be optimized before the fabrication of new device batches. Our investigations pointed the ways as the improving of the technology parameters of the MESFETs: V_{TH} at -10 V by decreasing the channel thickness and optimization of the ohmic contacts. The study of an optimized topology for the current source is a main step for the working of the comparator. When the comparator circuit will be overall operational, it would be also possible to have a Schmitt trigger circuit based on the comparator circuit.

5. Synthesis of the IC-SiC functions

Table 2 synthesizes our results about the considered integrated SiC functions. The common source amplifier, the ring oscillator and the Totem-pole [7] are working but the contact resistance must be improved in the process for reaching the expected performances. As indicated, the comparator presents an operational behavior but it is necessary to optimize the ohmic contact, the threshold voltage (V_{TH}) of the MESFET and the current sink to maintain a constant current in the comparator circuit. The Schmitt trigger is based on the comparator circuit. Because of the poor electrical performance from the comparator, this circuit could not

be currently tested. The synthesis is good thus the principle of integrated circuit with this process has been demonstrated and many functions are working.

Table 2. Synthesis of the main IC-SiC functions, V: “validated”, I: “in progress” and X: not validated.

Function	State	Improvement	Stabilization	Design references	Experimental data references
Common source amplifier	V	-Resistors		[10]	[10]
Ring oscillator	V	-Resistors		[9]	[9]
Comparator	I	-Resistors -Threshold voltage V_{th}		[9]	
Schmitt trigger	X		-Comparator	[9]	
Totem-pole	V	-Buffer MESFET		[7]	[7]
Spice model of the MESFET	V	-Contact resistance -Accuracy of parameters -Integration of the thermal effect		-Buffer MESFET	-Buffer MESFET

6. Conclusion

Integrated functions in SiC have been designed, manufactured and characterized in the purpose to elaborate a smart power driver. The experimental results have shown that the main electronic functions are operational, but it appears that these circuits must be technologically optimized for the next batches in order to adjust electrical parameters of the MESFETs such as the threshold voltage (V_{TH}) and the ohmic contact. Indeed, the value of the contact resistances must be also decreased for reaching the expected values in the polarization of the electronic functions. The availability of these optimized circuits will allow to consider a first demonstrator. The following step will be the test of these functions at high temperatures (> 200 °C). Nevertheless, this working research has permitted to demonstrate the technology feasibility of an integrated power circuit in SiC, which could operate in harsh environments.

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