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Study of interleaved PWM strategies applied to two back-to-back three-phase full bridges

Nicolas Patin · Zakaria Chmeit · Georges Salloum · Rita Mbayed

Abstract The aim of this study is to evaluate the impact of interleaved PWM strategies on the RMS current flowing through the DC link capacitor associated to two back-to-back three-phase Full Bridges (FB). Indeed, this value is usually the key-parameter for the sizing of this (or these) component(s), far above the capacitance, especially for aluminum electrolytic capacitors. Interleaving technique is applied on two different strategies: Unified Double Carrier PWM (dedicated to reduction of the RMS current for a single FB) and a classical (single carrier) space-vector PWM strategy.

1 Introduction

In the literature, different Pulse Width Modulation (PWM) strategies based on a double carrier have been developed in order to reduce the current in the DC link capacitor within the context of a single three-phase full bridge in comparison with classical (single carrier space vector PWM strategies). These techniques have presented in [1], [2] and [3]. The last one can be easily implemented on a DSP and is efficient for all practical operating points (for all modulation indexes and all usual power factors both in motor and generator modes). **The most recent papers like [4] about the DC link capacitors are currently focused**

on multi-phase converters. It has been shown in [5] that the reduction of the RMS current is of key importance for the reduction of the size of DC link capacitors (or the reduction of their stress), especially in low voltage high currents applications where they represent an important part of the overall volume of the converter. Indeed, in practice, the DC voltage ripple is never the tightest constraint for the design of the converter and, as a consequence, the capacitance is not the key parameter for the choice of aluminum electrolytic capacitors used within this context.

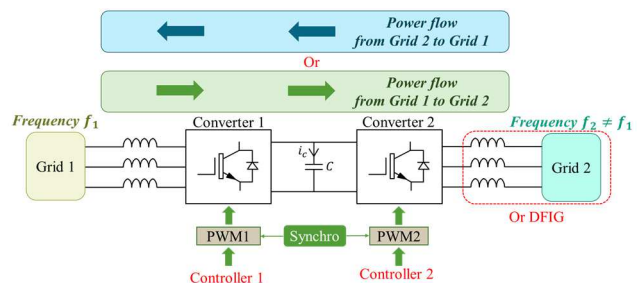


Fig. 1 Two back-to-back converters

All these studies have been performed in the case of an inverter fed by a battery (in an electric or hybrid vehicle) for instance. **However, other important cases that can be investigated are parallelized converters [5-6] and another interesting configuration (studied in the this paper)** is the back-to-back topology (as shown in Fig. 1) which can be found in various applications such as Doubly-Fed Induction Generators (DFIG) used as Variable Speed Constant Frequency Generators (wind mills [8], small hydropower [9], etc..). With two separate converters connected to a common point (DC link), an interleaved PWM technique is usually adopted (e.g. Voltage Regulation Modules dedicated to microprocessors) because it allows us to increase the effective frequency of the

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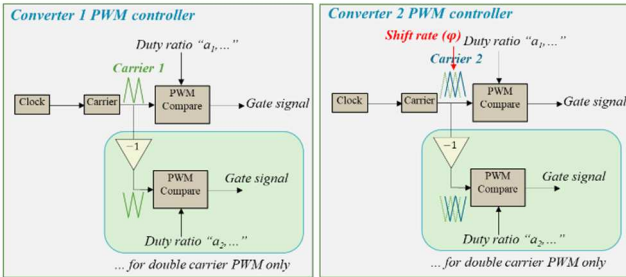
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current in the capacitor in comparison with the switching frequency applied to the active components in the converters. **This solution has been adopted in [5] and [6] and the objective in [5] is clearly focused on DC capacitor current. The aim of our study is also the reduction of the RMS current in this capacitor and the impact is evaluated for two different PWM strategies:**

- Classical Space-Vector PWM (SVPWM) with one carrier per converter
- Unified Double Carrier PWM (Uni-DCPWM) with two opposite carriers per converter

Indeed, even if the Uni-DCPWM has better performance than a SVPWM strategy for a single converter, this result has to be proved in the case of two back-to-back converters. So, the innovating aspect of this work is to compare the performance of both strategies in the context of interleaving of carriers. Then, it will be shown that the needed interleaving rate has to be dynamically tuned in order to reach the optimal performance and a simple tracking technique is tested in simulation.

In both cases, a shift rate $\psi = 100 \cdot \Delta t / T_s$ [in %] is applied between carriers of both converters, where T_s [in s] is the common switching period and Δt is the delay [in s] introduced between carriers as shown in Fig. 2.



Phase shift control:

$$\psi = 2\pi \cdot \Delta t / T_s \text{ [en rad]}$$

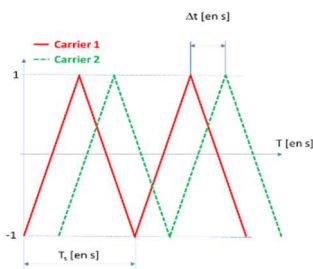


Fig. 2 PWM Carriers interleaving principle

Since this study is only focused on interleaving effects, the controllers are not detailed in this paper even if a DC voltage regulation is needed (and achieved with a controller 1 based on a classical AC currents inner loop and a DC voltage outer loop). The carriers used in this

paper are symmetric triangles (a complementary study with a sawtooth waveform could be easily done).

Grid frequencies f_1 and f_2 are usually different and in practice (with a DFIG), f_2 is much lower than f_1 . As a consequence, results presented in this paper are given with $f_1 = 50$ Hz and $f_2 \in [-15; +15]$ Hz]. Moreover, phase shift between voltages and currents are neglected on grid 1 and grid 2 in this paper where the study is limited to active power transfer.

In section 2, the instantaneous model of a three-phase inverter is presented and then, assumptions about splitting of low and high frequencies of the DC current are recalled in order to justify results already published in the cases of SVPWM and Uni-DCPWM strategies about the capacitor RMS current and recalled in section 3.

In section 4, the simulation of the interleaving impact is detailed and the complete system is briefly described.

In section 5, simulation results for SVPWM and Uni-DCPWM are analyzed and compared. A spectrum analysis also completes this study in order to evaluate the possibility to choose another technology of DC link capacitors.

In section 6, a real-time control is developed. It is based on a tracking technique. It aims to dynamically tune the interleaving rate when the operating point is modified in order to achieve optimal results. We finally conclude about the interest of Uni-DCPWM within this new context and on an optimal interleaving strategy in the case of a unity power factor operating mode of both converters.

2 Instantaneous model of a three-phase inverter

In the case of a three-phase inverter connected to a balanced three-phase load, the AC voltages can be expressed as a function of the DC voltage v_{dc} and switching functions c_x (where $x = a, b$ or c) as defined in equation (1). It shall be noted that this same model can be applied to a rectifier connected to a balanced three-phase grid.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{v_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \cdot \begin{bmatrix} c_a \\ c_b \\ c_c \end{bmatrix} \quad (1)$$

This “voltage” model should be completed by using the Kirchhoff’s current law which leads to (2):

$$i_{dc} = [c_a \quad c_b \quad c_c] \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

Using the “abc-to- $\alpha\beta$ ” transform, recalled in (3), equations (1) and (2) can be reformulated as in (4) and (5) respectively.

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}}_{C_{32}} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2v_{dc}}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} c_a \\ c_b \\ c_c \end{bmatrix} \quad (4)$$

$$i_{dc} = \frac{2}{3} [c_a \quad c_b \quad c_c] \cdot \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (5)$$

Where $[v_\alpha \ v_\beta]^t$ and $[i_\alpha \ i_\beta]^t$ are the $\alpha\beta$ components associated to the actual "abc" voltages and currents respectively.

Based on (4), the dot product occurring in (5) can be rewritten as in (6):

$$i_{dc} = \frac{1}{v_{dc}} [v_\alpha \ v_\beta] \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (6)$$

Therefore, the instantaneous DC current can be graphically identified in the $\alpha\beta$ reference frame as shown in Fig. 3 whatever the PWM strategy.

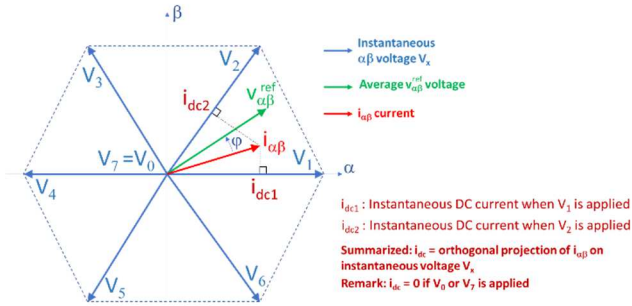


Fig. 3 PWM Carriers interleaving principle

The aim of the Uni-DCPWM technique is to limit the duration of application of zero vectors (V_0 and V_7) that lead to significant current ripples at the input of the inverter. Indeed, this ripple is of great interest in the dimensioning of DC link capacitors due to splitting of DC and AC components induced by the DC link filter as shown in Fig. 4a.

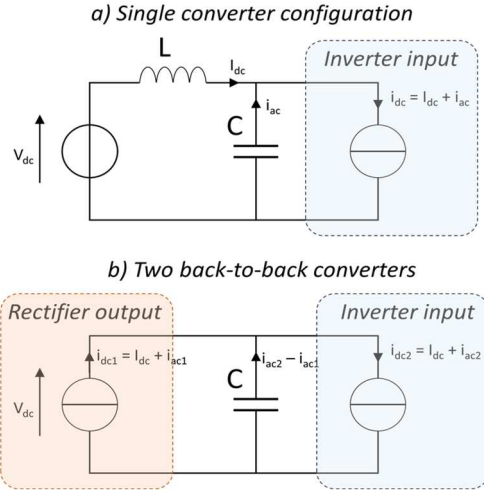


Fig. 4 DC link decoupling models with one converter (a) or two converters (b)

Due to the interaction of two converters in configuration 4b, the situation is much more complex. Indeed, the result about RMS capacitor current is not trivial even if the PWM controllers associated to the converters are synchronized (*i.e.* with the same carrier) because constructive and destructive "interference" can occur due to different spectrum distributions of i_{ac1} and i_{ac2} linked to different operating points of the rectifier and the inverter (even if the DC components remain the same for both converters).

As a consequence, it is not possible to conclude about the effectiveness of a PWM strategy in this back-to-back topology on the basis of the performances obtained in a single converter configuration (see results in section 5).

3 Studied PWM strategies

3.1. Space Vector PWM

Many PWM strategies can be used for the control of a three-phase full bridge due to the available degrees of freedom such as zero sequence component on the AC side. This study is limited to constant frequency PWM strategies.

Within this context, a logical choice is to analyse the widely used Space Vector PWM (SVPWM) technique which can be seen as a single carrier intersective PWM using a specific zero sequence v_z component added to sinusoidal references:

$$v_z = \frac{1}{2} \begin{cases} v_a & \text{if } |v_a| = \min(|v_a|, |v_b|, |v_c|) \\ v_b & \text{if } |v_b| = \min(|v_a|, |v_b|, |v_c|) \\ v_c & \text{if } |v_c| = \min(|v_a|, |v_b|, |v_c|) \end{cases} \quad (7)$$

It leads to a low distortion of the AC voltages with a maximal available amplitude of fundamental voltages ($V_{dc}/\sqrt{3}$) without overmodulation but :

- all leg switches two times per switching period,
- zero voltages V_0 and V_7 are both used per switching period.

These drawbacks correspond to non-optimal switching losses and sub-optimal RMS value of the AC component i_{ac} of the input current i_{dc} . It must be noticed that the RMS current in the DC link capacitor has been analytically expressed as in (8).

$$i_{c-rms} = I_{max} \sqrt{\frac{m\sqrt{3}}{4\pi} + \left(\frac{m\sqrt{3}}{\pi} - \frac{9m^2}{16}\right) \cos^2 \varphi} \quad (8)$$

where I_{max} , φ and m are respectively, the amplitude of AC currents, the phase shift between AC voltages and currents and m is the modulation index.

Moreover, this result is not only limited to the SVPWM but also applied to the basic sinusoidal PWM and more generally to all strategies using only two adjacent vectors (including active and zero vectors) during a switching period.

These issues (**sub-optimal switching losses and RMS current in the DC link capacitor**) are both addressed by the Uni-DCPWM strategy. However, **no analytical result (similar to equation (8)) has been established in the literature for double carrier PWM strategies [1-3]. For this purpose, numerical analysis has been used and the same methodology can be applied here with two converters as exposed in the following paragraph.**

3.2. Uni-DCPWM

The Uni-DCPWM is derived to a single carrier discontinuous PWM technique called GDPWM [9] which consists in adding a zero sequence component clamping a leg to one rail of the DC bus during a complete switching period. The interest of such a behaviour is the limitation of switching losses and as those losses are proportional to the switched current, the decision of the algorithm is based on the actual currents (absolute value) measured in the potentially clamped legs (either the one with the maximal requested duty ratio - without zero sequence component - or the one with the minimal duty ratio).

Then, the Uni-DCPWM only uses two opposite carriers for modulation of non-clamped legs. The interest of a double carrier strategy (as shown in [1, 2, 3]) is that it avoids or at least it limits the use of zero voltages V_0 and V_7 which dramatically increase ripples of the input current. According the assumption presented in Fig. 4a (total AC component flowing through the capacitor), the Uni-DCPWM significantly reduces the RMS current in the capacitor of a single converter as shown in Fig. 5.

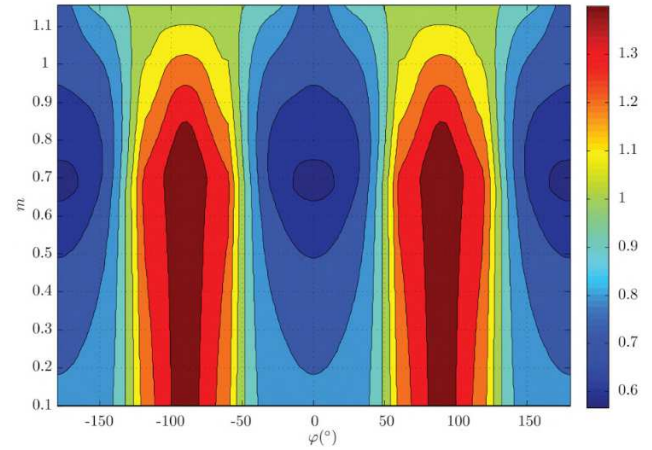


Fig. 5 Ratio between RMS current for Uni-DCPWM and SVPWM strategies as a function of the phase shift φ of the AC load (X-axis) and of the modulation (Y-axis).

Unfortunately, in the literature, no explicit function has been derived from double carrier techniques such as the original DCPWM presented in [1], Uni-DCPWM [3] or even the intermediary solution so-called Ext-DCPWM presented in [3]. This is mainly due to the non-linear behavior of such kinds of PWM strategies which calculate duty ratios (and select one carrier or its opposite) not only on the basis of voltage references but also on measured AC currents.

However, the calculation of the RMS capacitor current can be based on idealized currents waveforms since high frequency ripples can indeed be neglected in practice. Thus, on the basis of equation (6) and since the DC components of i_{dc1} and i_{dc2} must be the same in steady state operation (in order to achieve the stability of the DC bus voltage), a script-based analysis of the behavior of PWM strategies in steady-state operating mode can quickly (less than 0,1 s per operating point and approximately 30 s for a cartography like those presented in figures 8 to 10) confirm results obtained with transient simulations.

Such an analysis allows us to check the impact of all key parameters :

- independent AC frequencies for both converters (f_1 and f_2)
- Independent power factors for both converters (in this study, for converter 1, a unity power factor is assumed to be reached but this parameter could be easily modified),
- Delayed carriers between these two converters.

The only parameter which has to be initialized at the beginning of the analysis is the V_{dc} reference. Thus, if voltage drop across grid side inductors is neglected, it gives:

$$m_1 = \frac{2V_{1max}}{V_{dc}} \quad (9)$$

where V_{1max} is the amplitude of grid voltages (325 V in this study).

Finally, indexes m_1 and m_2 applied to PWM controllers (of both converters) are linked by the following equation:

$$\begin{aligned} m_1 \cdot I_{1max} \cos \varphi_1 &= m_1 \cdot I_{1max} \\ &= m_2 \cdot I_{2max} \cos \varphi_2 \end{aligned} \quad (9)$$

Thus, for a given φ_2 phase shift, the amplitude of grid currents in rotor windings of the DFIG are linked. As a consequence, the characterization of DC link capacitor RMS current for cascaded converters is similar to the one applied to a single converter (except a new degree of freedom which is the delay introduced between carriers for both converter).

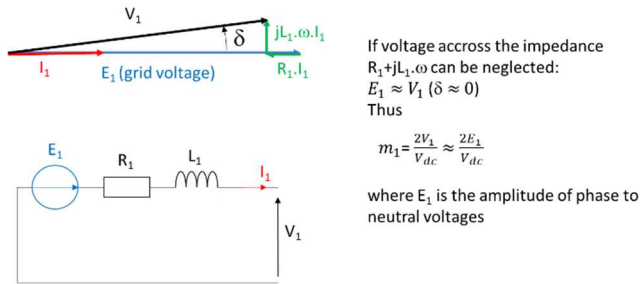


Fig. 6. Grid voltages vector diagram

Remark: On the grid side, $\varphi_1 = 0$ is equal to zero in this study but if a static reactive power compensation is needed, it could be modified as needed. In such a case, the current in the DC-link capacitor is significantly increased but a dependence on interleaving remains.

4 Virtual testbench

4.1. Description

The analysis of the DC capacitor stress with both PWM strategies is performed with two back-to-back converters as shown in Fig. 1. A classical application of such a topology is the control of a Doubly-Fed Induction Generator. However, in order to simplify the simulation model (**implemented in Matlab/Simulink**), one converter (converter 2) is connected to a simple (balanced) three-phase RL load. All parameters of this system are summarized in Table 1.

Table 1 System parameters

Parameter	Value
Switching frequency	10 kHz
Grid 1 frequency	50 Hz
Grid 1 voltage (L-N)	230 V

Grid 1 inductances	1 mH
Grid 1 resistances	1 m Ω
DC bus voltage reference	722 V
Load inductance	10 mH
Load resistance	35 Ω
Load frequency	0-15 Hz

The control of converter 1 is based on an inner dq-current loop included in a DC voltage regulation loop allowing us to maintain the DC bus voltage to a constant reference (722 V). During all simulation, this voltage is initially regulated before the activation of converter 2.

Then, the output current of converter 2 is regulated in a dq-reference frame with different references from 1 to 10 amperes, requiring a variation of the modulation index in a wide linear range (from 0 to 1).

4.2. Validation waveforms

The satisfactory operation of the system can be checked with two key indicators (see Fig. 6):

- Regulation of DC bus voltage,
- AC output currents (converter 2).

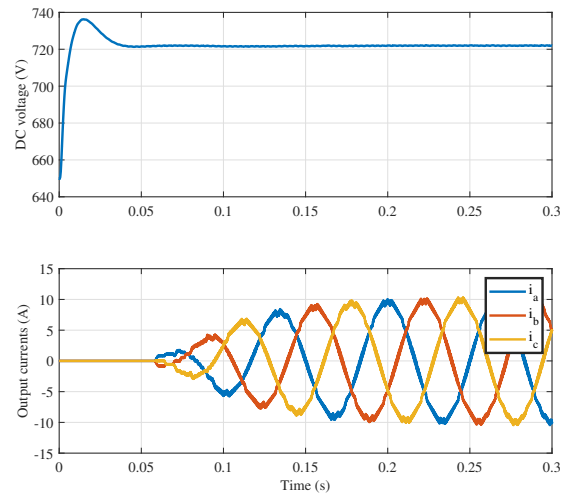


Fig. 6 Single simulation: DC link voltage and AC output currents waveforms.

This figure also shows that steady state operation is reached in less than 0.3 s (which is the duration of all **transient** simulations). Since this study is performed with two different strategies on an extensive amount of operating points (see Table 2 : shift rates between carriers applied to PWM controllers of converters 1 and 2, output current references with different amplitudes and frequencies), all scripted simulations must be verified by checking these two indicators which guarantee the stability of regulations in all cases.

Table 2 Tuning ranges of key parameters

Parameter	Range
Shift rate (%)	[0 ; 90] - step: 10%

d-axis current reference	[1 ; 10] - step: 1 A
(conv. 2 output) - Amperes	
Output frequency F_{out}	0 ; 5 ; 10 ; 15 Hz

5 Interleaving effect and comparison of PWM strategies

In Fig. 7, it can be seen that the interleaving (for SVPWM) has an effect essentially at high modulation indexes applied to converter 2 (linked to the output current reference) when the output frequency is 0 Hz. Moreover, the "intuitive" optimal shift rate of 50% can be verified for all modulation indexes.

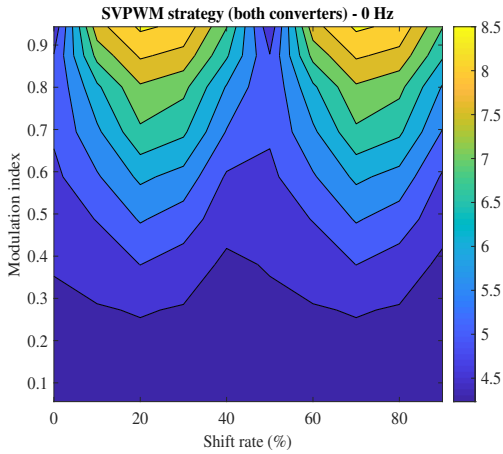


Fig. 7 Interleaving effect @ $F_{out} = 0$ Hz on the RMS capacitor current for a SVPWM strategy.

In Fig. 8, this result is presented for the same operating conditions with the Uni-DCPWM strategy. And, in this case, we can see that the RMS current in the DC link capacitor is lower with this PWM technique than with the SVPWM one. However, it seems that the optimal shift rate is slightly higher than 50% and should probably be adapted to the modulation index. This result is coherent with the one obtained in the case of a single inverter.

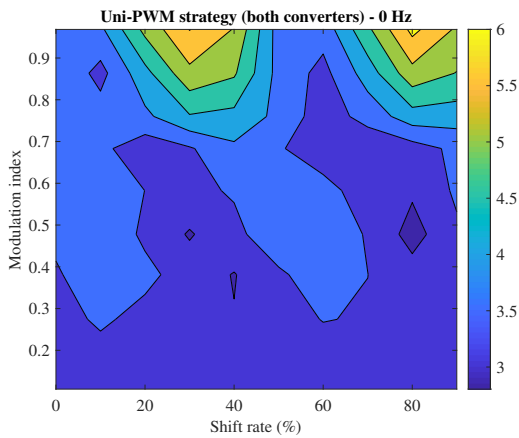


Fig. 8 Interleaving effect @ $F_{out} = 0$ Hz on the RMS capacitor current for a Uni-DCPWM strategy.

This comparison is illustrated in Fig. 9 by the ratio of RMS currents (Uni-DCPWM/SVPWM) in both cases for all operating points. When the ratio is greater than 1, it means that the Uni-DCPWM is less efficient than the SVPWM. Thus, it can be noted that it is **never** the case for **any** observed operating points.

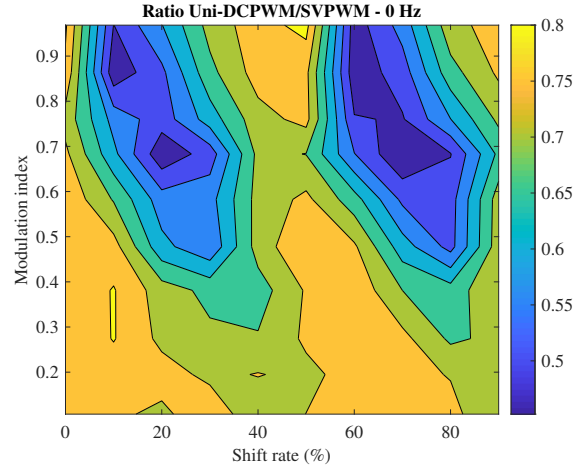


Fig. 9 Comparison between Uni-DCPWM and SVPWM strategies @ $F_{out} = 0$ Hz.

The same result can be observed in Fig. 10 when the output frequency is set to 15 Hz. Other simulations at other frequencies (5 and 10 Hz, not presented in the article) have also led to the same result.

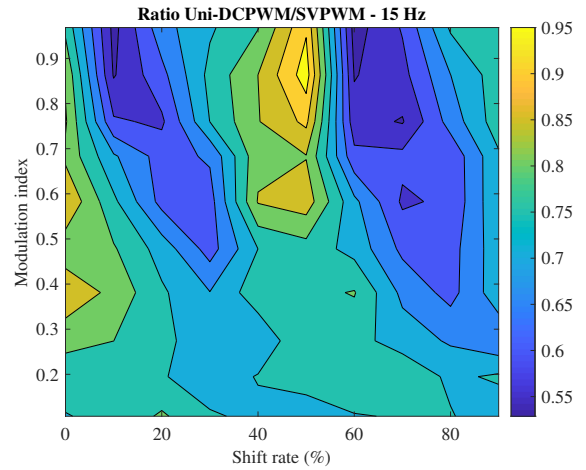


Fig. 10 Comparison between Uni-DCPWM and SVPWM strategies @ $F_{out} = 15$ Hz.

It should be noted that the gain at 15 Hz is lower than at 0 Hz. Moreover, it can be seen in Fig. 10 that the optimal shift rate (applied to the Uni-DCPWM) is not 50% and must vary according to the operating point (*i.e.* modulation index).

Finally, in Fig. 11, the capacitor current spectra for SVPWM and Uni-DCPWM show that the interleaving does not clearly increase the apparent frequency of the current on DC side. Indeed, significant harmonic components appear around the switching frequency

(10 kHz) even if the most significant terms of the spectrum are located at 20 kHz. This result is quite similar to the one obtained with a single converter and in such a situation, the most valuable capacitor technology remains the aluminum electrolytic one.

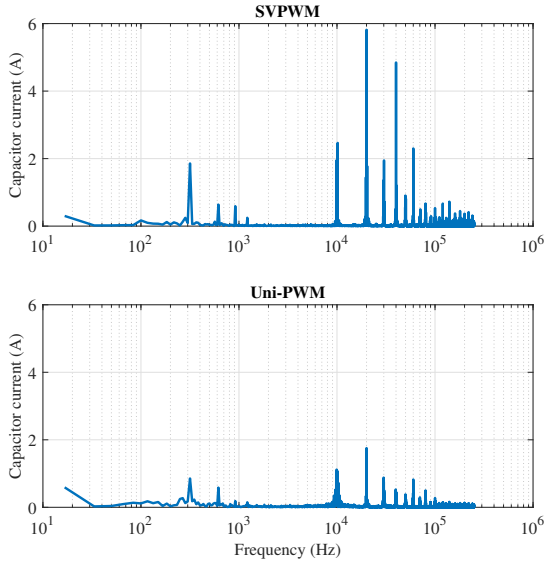


Fig. 11 Comparison of capacitor currents spectra in both cases.

6 Real-time interleaving control

6.1. Preliminary analysis

Since the impact of the interleaving of carriers is proved for both strategies and as it is shown the best performance for RMS DC link capacitor current is achieved with the Uni-DCPWM technique, it is clear that an adapted real-time control is required. Indeed, with this PWM strategy, as it is shown in Fig. 8, the interleaving rate needs to be dynamically tuned when the operating point is modified for achieving optimal results.

However, this closed-loop control cannot be based on a classical reference-based controller because the objective is a minimisation of the RMS current in the DC link capacitor and not a regulation at a given value. Thus, a good choice for this purpose is to use a tracking technique similar to the one used in MPPT (Maximal Power Point Tracking) strategies applied to photovoltaic converters as in [10].

6.2. Structure and start-up sequence

The global structure of the controller used for both converters is presented in Fig. 12. The key element studied here is the "tracking block". However, in order to obtain a proper behaviour of the complete system, the following start-up sequence is necessary (**flowchart presented in figure 13**):

1. Activation of the converter 1 (converter 2 is inhibited) with its dedicated control loops **in order to reach the DC link voltage reference (720 V here)**
2. When the DC bus voltage reference is reached, converter 2 is activated with an initial interleaving rate equal to 50 %. Simultaneously, the associated AC currents control loop is activated with given dq references
3. Then, the tracking algorithm is used in order to reach the minimal RMS current in the DC link capacitor.

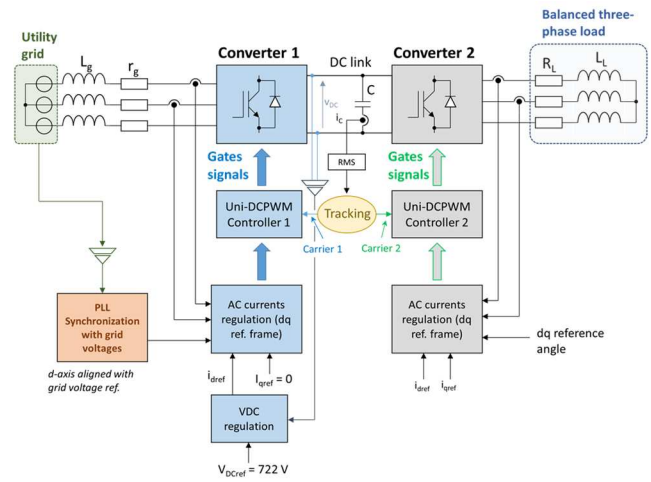


Fig. 12 Global control scheme

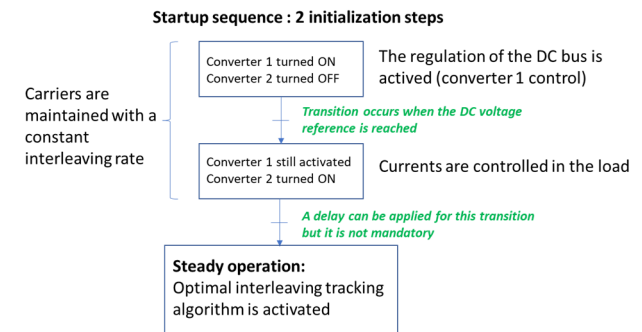


Fig. 13. Startup flowchart

Since the RMS current is measured through a 1st order low pass filter with a cut-off frequency equal to 200 Hz, its time constant is lower than 1 ms. As a consequence, a sampling period of 1 ms can be used for the reconfiguration of the interleaving rate resulting in a significant evolution of the estimated RMS current (ICRMS).

Then, the sensitivity of this current according to the interleaving rate (ILR) which is observed in the cartography observed in Fig. 8, the variation step used in the controller is equal to 2 %. The (simple) algorithm applied in this study can be illustrated by the flowchart shown in Fig. 14.

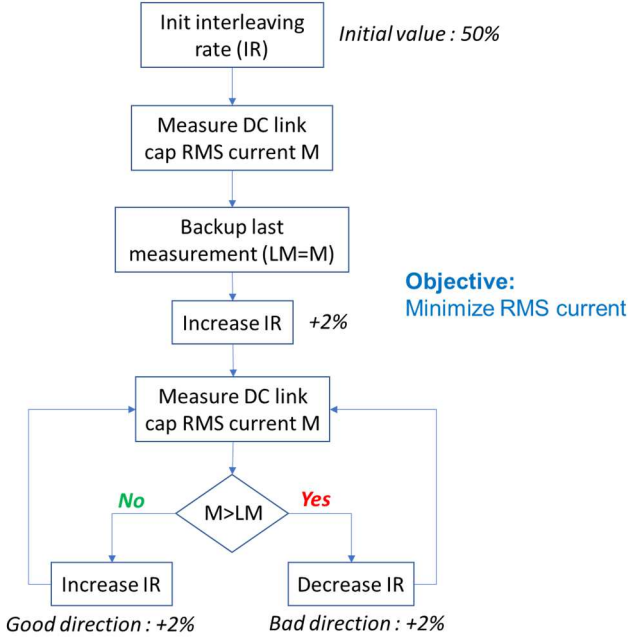


Fig. 14. Optimal interleaving tracking algorithm

6.3. Simulation results

Simulations have been performed using the methodology detailed in the previous paragraph. The obtained results are presented in **Fig. 15**.

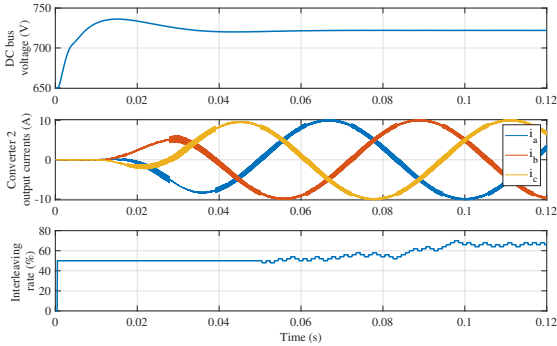


Fig. 15. Dynamic interleaving tuning

In this simulation, we can see that the DC bus voltage is precharged at 650 V. This result can be obtained in practice when the gate signals are inhibited since, in such a case, converter 1 operates as a three-phase full-bridge diode rectifier. The associated controller (activated @ $t = 0$ s) allows us to reach the voltage reference and, as a consequence, converter 2 is activated @ 10 ms with a ramp applied to the i_d current reference (reaching a steady-state value equal to 10 A @ $t = 30$ ms). The actual currents (their amplitude) reach this value 10 ms later.

Finally, the algorithm dedicated to the tracking of the optimal interleaving rate is started @ 50 ms as we can see in **Fig. 15**: before this instant, the interleaving rate is constant (50 %) and then, variations can be observed with a "steady-state" after $t = 100$ ms. It can be seen that the

optimal interleaving rate found by the algorithm is greater than 50% (more precisely between 66 and 68 %). Finally, from $t = 0.05$ s to 0.12 s, the RMS current in the DC link capacitor can be seen in **Fig. 16**.

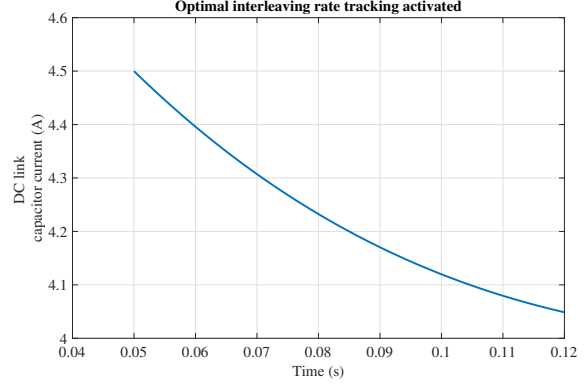


Fig. 16. Reduction of the capacitor RMS current due to the optimal interleaving rate tracking

Even if this kind of control scheme does not give a quick response, it should be noted that the aim of this tracking is to limit losses in the DC link capacitors. More precisely, it is well known that aluminum electrolytic capacitors are very sensitive to their internal temperature, it plays a direct role in their lifetime. Thus, the minimization of the "instantaneous" RMS current is not as crucial as its minimization on a large time span and within this context, a convergence in few tens of milliseconds is perfectly satisfying in comparison with the thermal time constant of several hundreds of seconds even for small capacitors [11].

As it can be seen in **Fig. 17**, the capacitor current waveform is significantly modified by the operating point (including the interleaving rate) with three different configurations. More particularly, it can be noticed that, even the interleaving allows to reduce the RMS value of currents, peak value can be very high due to narrow spikes as it can be seen for the third operating point presented in this figure (for a modulation index $m_2 = 1$, an output frequency $f_2 = 10$ Hz and with an output phase shift $\phi_2 = 0$ rad).

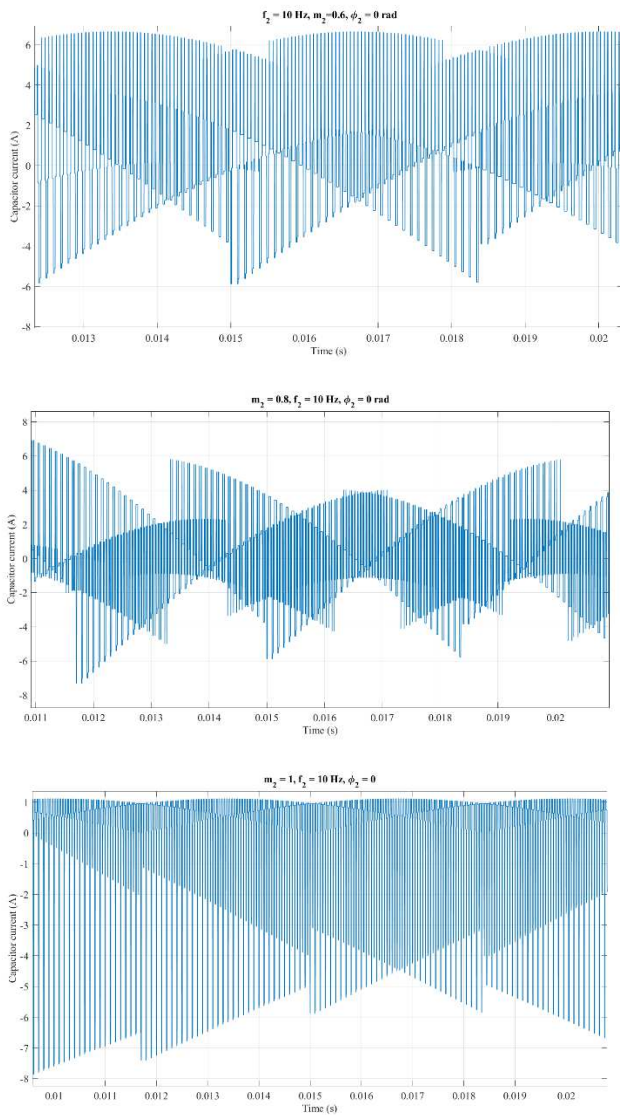


Fig. 17. Instantaneous capacitor current waveforms (for three different operating points)

7 Conclusions

This article shows that the use of two interleaved PWM controllers is of great interest in the context of two back-to-back converters, since it can significantly reduce the RMS current in the DC link capacitor, especially at high (output - *i.e.* converter 2) modulation index. Moreover, the Uni-DCPWM seems to be the most adapted strategy within the context of a converter connected to the rotor of a DFIG with a limited range ($\pm 30\%$) around the synchronous speed (corresponding to ± 15 Hz if the grid frequency is equal to 50 Hz). For a larger output frequency range, the SVPWM could be more efficient under the condition of a dynamic adaptation of the shift rate between carriers. Therefore, a real-time interleaving control is elaborated based on a

tracking technique. Its application yields to minimize the losses in the DC and as a consequence, their internal temperature.

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