Study on Measurement Discontinuity during On-wafer TRL Calibration of 28FD-SOI Devices upto 110GHz

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***Abstract* — This study analyses the effect of test structure design for on-wafer TRL calibration of 28nm FD-SOI MOSFETs upto 110 GHz. Two different calibration kits are designed with and without continuous ground plane and their effect on the extracted transistor parameters are studied in terms of the measurement discontinuities encountered. Measurement results are discussed in conjunction with electromagnetic co-simulations, which use the small-signal equivalent circuit model of transistor along with the 3D models of the probes and test structures. The electric field coupling between the probes is visualised in each case and conclusions are drawn.**

***Keywords* — RF characterization, 28FD-SOI, on-wafer TRL, small signal model, electromagnetic simulation**

I. Introduction

Millimeter waves find tremendous applications in the present-day world, owing to its remarkable advantages such as high data rates, large available bandwidth and smaller device sizes, leading to a profound interest in the ongoing research in millimetre wave devices and technologies. Major application domains of these devices are in high-speed communication systems such as 5G, high resolution imaging for radars or medical application, Internet of Things (IoT) and so on. Fully Depleted Silicon on Insulator (FD-SOI) transistors with maximum reported f_T/f_{MAX} values above 300 GHz [1][2][3] are an excellent choice for circuit applications [4] in these frequencies. This technology also exhibits lower parasitic capacitances and lower power consumption [5]. For efficient circuit design at millimeter wave frequencies, it is imperative to be able to perform reliable characterization of these transistors to obtain accurate device models.

The device characterization can rely on either off-wafer or on-wafer calibration. The fundamental disadvantage of off-wafer probe-tip calibration such as SOLT is due to the change of substrate between calibration standards and the DUT, resulting in measurement errors especially at higher frequencies above 200 GHz [6]. On the other hand, on-wafer TRL calibration [7], which sets the calibration reference plane at the beginning of access lines, is accepted as the calibration of reference for microwave measurements [8]. The S-parameters obtained after TRL calibration have a reference impedance equal to the characteristic impedance of the Lines. Therefore, an impedance correction is carried out as in [9] and [10] to reference the S-parameters to the standard value of 50 ohms.

The design of the on-wafer standards can affect the measurement accuracy. The spatial arrangement of the neighboring on-wafer structures around the DUT can also influence the results and this can be minimized by using a diagonal checkerboard pattern [11] (see also Fig 2 a and b). Then, the nature of the reflect standard has minor effects on the error terms as discussed in [12]. Finally, inaccuracies in the calibrated S-parameters can also result from incorrect probe positioning on the RF pads [13]. The effects of measurement environment, specifically the choices of RF probe and the calibration type, have been discussed in [14]. It is suggested in [15] that the calibration kit designed with a continuous ground plane below all the test structures can reduce multimode propagation and eliminate slot modes. The benefit of such a design using test structures from STMicroelectronics BiCMOS 55nm technology has been demonstrated in [16].

In this paper, dedicated to FD-SOI technology, an on-wafer TRL calibration kit designed with a continuous ground plane and pad shields is compared with an on-wafer TRL calibration kit without these, focusing on measurement discontinuities study. In the frequency range of 1-110 GHz, two LINE standards are inevitable to cover this wide band. Therefore, the measurement discontinuity at the frequency limit (point where the line change is made during calibration) is studied with the aid of Electromagnetic (EM) simulations, providing insights into the origin of the discontinuity.

II. Design of Test Structures for On-wafer TRL Calibration

The test structures for on-wafer TRL have been designed using the 10ML BEOL stack of a 28nm FDSOI technology [17]. They consist of the following elements:

i) Thru: a 50 Ω microstrip transmission line in the topmost Aluminium metal layer (LB) (Fig.1a).

ii) Reflect: Four different reflect standards are designed to allow comparison. Pad Open (Fig. 1b) and Pad Short are the Open & Short structures at the reference plane of the RF pad, whereas Open LB (Fig. 1c) & Short LB are the reflect standards with reference plane at the inner edge of the access lines. These standards can be used to remove the distributed effects of the access lines during the TRL calibration step.

iii) Lines: The calibration kit designed in this paper uses Lines of 3 different lengths to cover different frequency ranges: Line_110G (660 µm) for 13-110 GHz, Line_300G

(300 µm) for 30-300 GHz and Line_500G (180 µm) for 70-500 GHz measurements.

iv) Pad Load: For impedance correction to 50Ω. [9][10].

In this work, two different on-wafer TRL calibration kits have been fabricated. The test structures in both kits are the same, the only difference being that the second one (hereafter termed Block2) has a continuous ground plane for all the test-structures, meaning that all the ground pads are connected together, and DUTs with pad shields, which consists of an extension (all metal layers below aluminum) of the ground pads surrounding the signal pad. The ground plane in Metal1+Metal2 is discontinuous in the first case (Block1) between each structure on the wafer as in Fig. 2a.

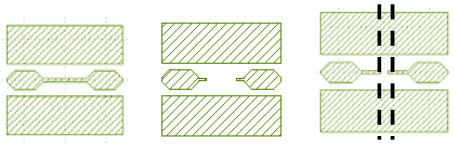


Fig. 1. Test structures for on-wafer TRL (a) Thru (b) Pad Open (c) Open LB

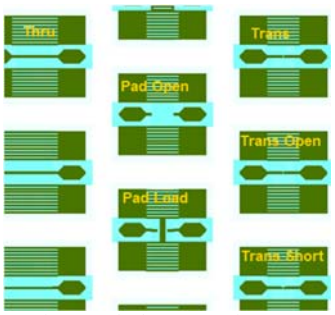


Fig. 2a. Block1: No continuous ground plane

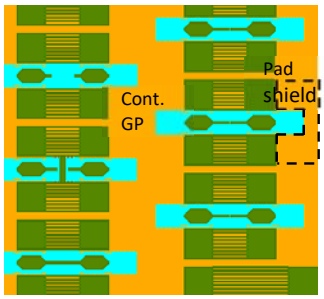


Fig. 2b. Block2: With continuous ground plane

III. Measurement and EM Simulation Setup

The measurements were performed from 1 to 110 GHz using Agilent E8361 PNA, with frequency extenders for the 67–110 GHz frequency range. Picoprobe RF probes were used for the measurements. A single Line does not cover the entire frequency band, therefore the LINE110G is used for TRL upto 70 GHz, the LINE300G is used from 70-110 GHz. The raw (uncalibrated) S-parameter measurements are first performed on all the test structures. Calibration is then applied on this data using the TRL algorithm [7], followed by the impedance correction. The on-wafer TRL calibration performed in this work uses OpenLB as the reflect standard, such that the reference plane after calibration is set just above the BEOL interconnects (see Fig.1c). In other words, this step removes the parasitic effects due to the measurement equipment, the RF probes, the RF pads and the access lines. In order to shift the reference plane to the actual device terminals at M1 metal layer, a Short-Open de-embedding is performed on the calibrated data, to remove the parasitic effects of the BEOL stack. The measurement results are discussed in the following sections. The DUT is a NMOS transistor with gate length of 30nm and gate width of 20µm distributed over 40 gate fingers.

EM simulations were performed from 1-110 GHz using the commercial FEM solver Ansys HFSS. The layout of each structure is imported into HFSS to form a 3D model by mapping each layer to its respective properties. A complete EM simulation is performed by including the RF probe models in the simulation. The tomographic 3D model of the RF probes as described in [18] are used for this purpose. All TRL test structures and the Transistor Open & Transistor Short are simulated in this manner. For the simulation of the transistor, an EM co-simulation [19] is performed, which combines the EM simulation of the passive parts of the transistor with the simulation of the small signal equivalent circuit (SSEC) (see Fig. 3) of the transistor. The data thus obtained from the EM solver is also calibrated using the TRL algorithm and de-embedded. The resulting S-parameters are now equivalent to those from the measured setup (after calibration & de-embedding) and provides a mean of validating the measurements.

IV. Results & Discussion

The passive DUTs are first calibrated to extract the parasitic capacitance of the Transistor Open and the parasitic inductance and resistance of the Transistor Short. These parasitics extracted from measurements on Block 1 (B1) and Block 2 (B2) are plotted in Fig. 4 and compared with those from the EM simulation of these structures with the probes. Comparing the plots from B1 & B2, there exists a better continuity in the measurements from B2 It is also observed that the EM simulations well reproduce the Open measurements. Regarding the Transistor Short, the agreement is quite satisfying in spite of the 1-2 pH difference which can be due to the probe positioning errors. The good agreement between the measurement results and the EM simulations confirms the accuracy of the simulations used. These parasitics are then subtracted from the on-wafer TRL calibrated S-parameters of the transistor during the de-embedding step, after which the transistor parameters can be extracted.

Two important figures of merit of RF transistors are the transit frequency f_T and the maximum oscillation frequency f_{MAX}. These are extracted as in (1) and (2) below and plotted in Fig. 5, where the orange curves correspond to Block1 and the green ones correspond to Block2. The measurement results are represented by symbols and the EM co-simulation results by solid lines. These are also compared to the simulated small signal model of the transistor (black curves).

$$f_T = |H_{21}|.f \quad (1)$$

$$f_{MAX} = f.\sqrt{U} \quad (2)$$

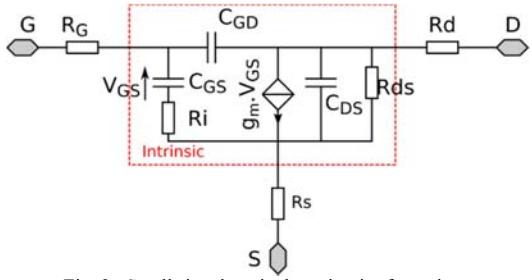


Fig. 3. Small signal equivalent circuit of transistor

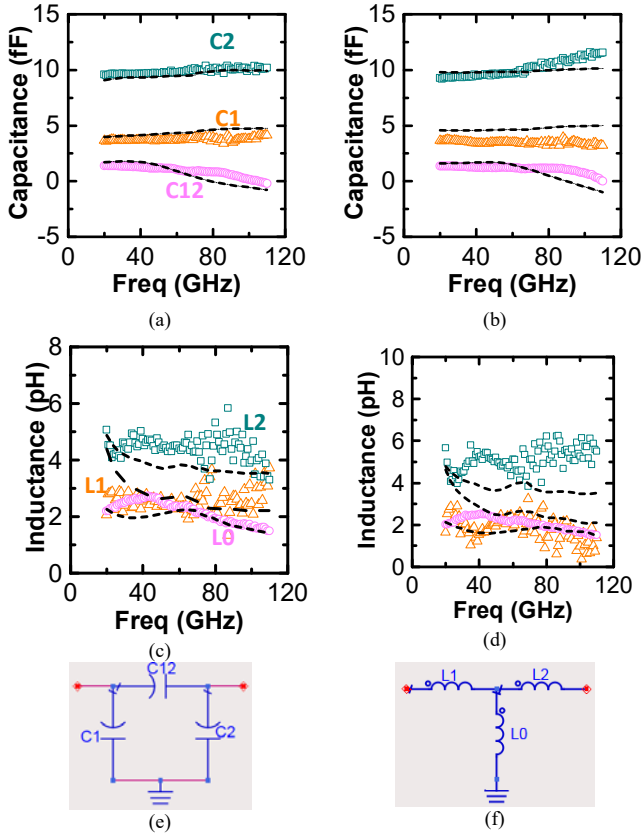


Fig. 4. (a) Capacitance of Transistor Open (Block1) (b) Capacitance of Transistor Open (Block2) (c) Inductances of Transistor Short (Block1) (d) Inductances of Transistor Short (Block2) (e) Equivalent circuit of Open (f) Equivalent circuit of Short

It can be observed from Fig. 5a that when comparing the small signal model to EM co-simulation, a difference in both f_T and f_{MAX} appears, which indicates that the applied on-wafer TRL calibration and Short-Open de-embedding procedure are not able to correct completely the measurement of DUT from its environment. Furthermore, the measured f_T extracted from both blocks is 330 GHz and is very similar. However, we see a small bend in the f_T curves from EM simulation. This can be attributed to the material properties used in the RF probe models for simulation, as it may not be exactly representative of the actual material properties used by the probe manufacturer. In the f_{MAX} plot (Fig. 5b) as well, it is seen that both blocks give similar results. Nevertheless, we see a small discontinuity at 70 GHz (it is the frequency point where the Line used for TRL calibration is changed from LINE110G to LINE300G) on the curves obtained from Block1 (barely visible in simulation, more pronounced in measurements). This effect in Block1 can be explained by visualizing the E-field distributions in the LINES in each block. It is to be pointed out here that the E-field coupling between the probes is chiefly due to two contributions, the first one through the air above the structure and the second through the substrate below the ground plane. However, the second contribution is much higher owing to the higher permittivity of the substrate. Thus the $\varepsilon_{r,eff}$ is the result of these two contributing factors. This probe-to-probe coupling effect is not corrected in the TRL algorithm.

The complex magnitude of electric fields in the different structures at 70 GHz is presented in Fig. 6. Fig. 6a-6c represent the E-fields in the LINES in Block1, and Fig. 6d-6f represent the same in Block2. Comparing these, it can be seen that the E-field patterns are not identical. The probe-to-probe coupling (represented by the E-field) between Port1 and Port2 is strongest for the shortest Line (LINE500G). Moreover, on comparing the similar Lines of B1 and B2, we can see that there is a significant penetration of the E-field into the substrate in B1 only.

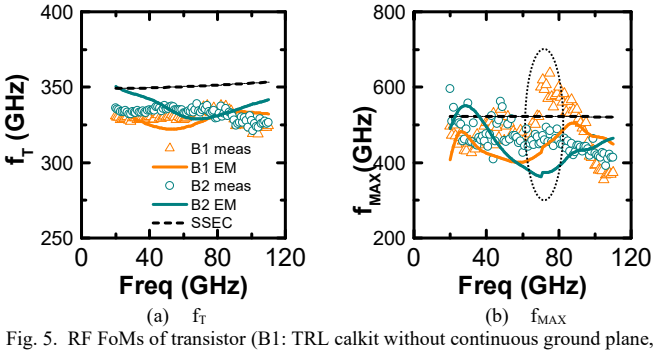


Fig. 5. RF FoMs of transistor (B1: TRL calkit without continuous ground plane, B2: TRL calkit with continuous ground plane)

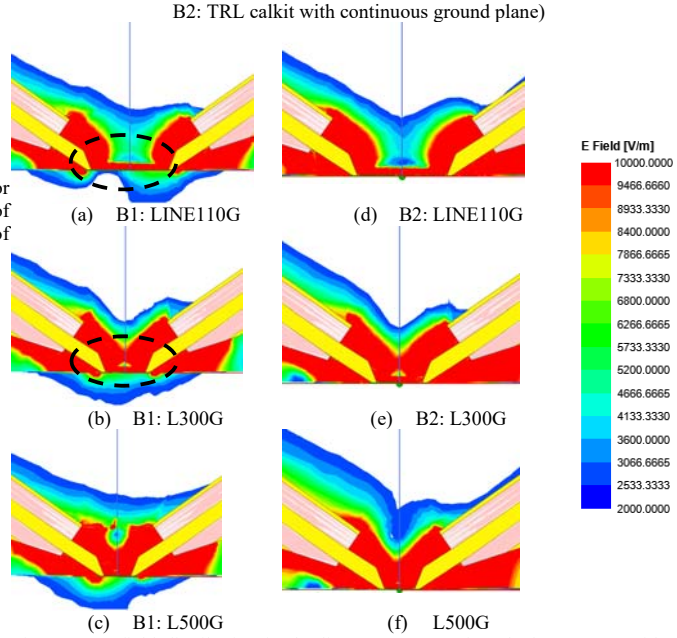


Fig. 6. EM field distribution in the lines at 70 GHz for Block1 (a to c, without continuous ground plane) and Block2 (d to f, with continuous ground plane)

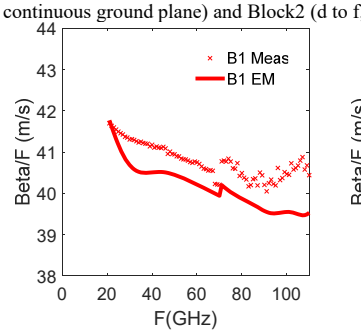


Fig. 7a. Normalized Beta extracted from on-wafer TRL calibration on Block1 (measurement and co-simulation)

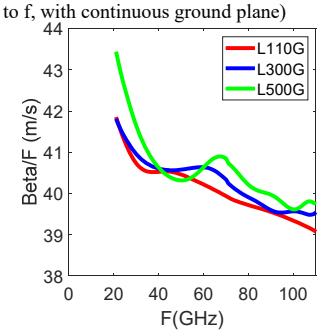


Fig. 7b. Normalized Beta of each LINE in Block1 after on-wafer TRL calibration (co-simulation)

As a result of this E-field difference between LINE110G and LINE300G, there exists a small difference in the line phase constant (β) extracted during the TRL algorithm before and after 70 GHz, thereby resulting in the discontinuity at this frequency point as plotted in Fig. 7a for Block1. This figure also points to the fact that there exists a difference in the effective dielectric constant ($\varepsilon_{r,eff}$) before and after 70 GHz and it increases at 70 GHz.

The absence of field penetration below the ground plane of the test structures and into the substrate when we have a continuous ground plane as in Block2 means that the coupling between probes in Block1 is higher than in Block2, resulting in a relatively larger percentage of error in Block1 at 70 GHz, due to the higher $\varepsilon_{r,eff}$. For a comparable probe geometry, this effect is expected to be more pronounced at higher frequencies (above 110 GHz).

This discontinuity can be visualized through other transistor parameters as well, for example, the gate resistance (R_{gg}) and transconductance (g_m) as shown in Fig.8, extracted using (3) and (4). However, in the measured curves of these parameters, the level of discontinuity is comparable to the noise variation level which makes it difficult to distinguish between the noise and the discontinuity. Nevertheless, this effect is clearly apparent in the curves from EM simulation.

$$R_{gg} = real((Y_{11})^{-1}) \quad (3)$$

$$g_m = real(Y_{21} - Y_{12}) \quad (4)$$

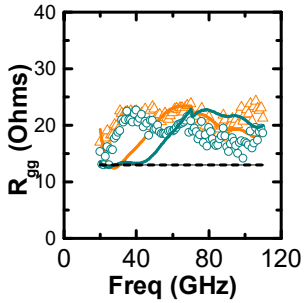


Fig. 8(a). Gate resistance of transistor

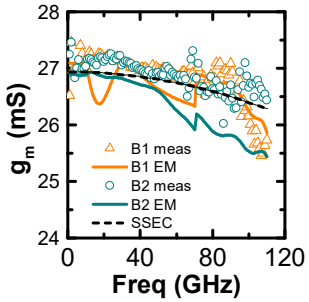
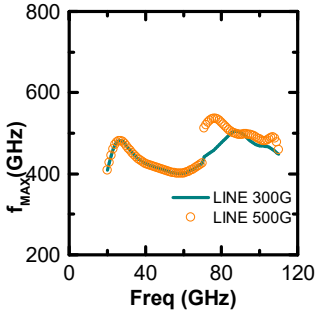


Fig. 8(b). Transconductance of transistor



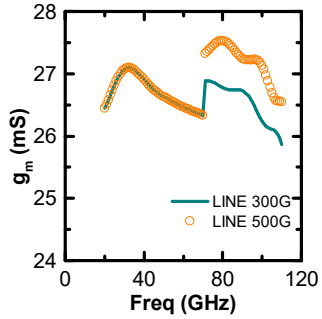


Fig. 9. f_{MAX} and g_m of transistor extracted from TRL calibration (EM simulation) using different lines after 70 GHz in Block1

This on-wafer TRL calibration has also been repeated on Block1 by replacing the HF line standard, LINE300G by the LINE500G which is much shorter, in order to be able to perform calibration for a larger range of frequencies (upto 500 GHz). However, this replacement causes the discontinuity at 70 GHz to increase in magnitude (refer Fig. 9) because there is now a significantly larger difference between the E-field distributions in the LINE110G and LINE500G than in the previous case (Fig. 7a-7c). This change in E-field also causes the $\varepsilon_{r,eff}$ of LINE500G to be slightly higher than that of LINE300G as seen in Fig.7b due to the increased coupling between probes (only simulation results are presented for better visualisation). As a result, the magnitude of error in computing the line propagation constant during TRL is now larger beyond 70GHz. Therefore, although a shorter a line standard provides the advantage of being able to calibrate the device for a larger bandwidth, it brings in a considerable error in the results in the form of the discontinuity. In other words, it is advisable to use lines with similar field distribution (or line lengths just matching the required frequency range for calibration) when multiple lines are to be used for TRL calibration.

V. Conclusion

On-wafer TRL measurements have been performed on 28nm FDSOI MOSFET transistor. The effect of the existence of a continuous ground plane has been studied by comparing the measurement results with and without a continuous ground plane and investigated using EM simulations. It has been observed from the simulations that the E-field penetration into the substrate and thus the coupling between the probes is reduced in the presence of a continuous ground plane, thereby reducing the measurement discontinuities. Further, it can also be concluded that when multiple lines are used during the TRL calibration, it is preferable that the line lengths are closer so as to have similar field distributions, although this reduces the bandwidth of TRL calibration.

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