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Exploring Compact Modeling of SiGe HBTs in Sub-THz Range with HICUM

Soumya Ranjan Panda, *Member, IEEE*, Thomas Zimmer, *Senior Member, IEEE*, Anjan Chakravorty, *Member, IEEE*, Nicolas Derrier, and Sebastien Fregonese

Abstract—This study delves deeper into the high-frequency behavior of state-of-the-art sub-THz silicon-germanium heterojunction bipolar transistors (SiGe HBTs) fabricated with 55 nm BiCMOS process technology from STMicroelectronics. Using measurement data, calibrated TCAD simulations, and compact model simulations, we present a comprehensive methodology for extracting several high-frequency parameters (related to parasitic capacitance partitioning and non-quasi-static effects) of the industry standard model, HICUM. The parameter extraction strategies involve thorough physics-based investigation and sensitivity analysis. The latter allowed us to precisely evaluate the effects of parameter variations on frequency-dependent characteristics. The accuracy of the finally deployed model is tested by comparing the model simulation with measured small-signal two-port parameters of SiGe HBTs up to 330 GHz.

Index Terms—SiGe HBT, High-frequency characterization, HICUM, Parameter extraction, THz Device, NQS effects.

I. INTRODUCTION

THE exponential growth of the communication market fueled the research in the area of devices and circuits capable of operating in the millimeter wave (mmW) and THz range. In this frequency range, cutting-edge technologies such as CMOS, BiCMOS, and InP HBT/HEMTs have been employed to develop transceiver (TRx) systems. For instance, advanced CMOS nodes have been utilized to fabricate a 300 GHz-Band Single-Chip CMOS Transceiver achieving a data rate of 80 GB/s [1]. Additionally, a 300 GHz wireless TRx supporting data rates exceeding 100 Gb/s has been successfully realized with InP-HEMTs [2], where a 200 GHz Direct-Conversion LO-Phase-Shifted Transmitter/Receiver has been fabricated with InP HBT [3]. Recently, significant advancements have been made, including the design of fully integrated wideband IQ transmitter and receiver circuits featuring on-chip antennas operating at 240 GHz, with data rates reaching up to 100 GB/s, all using an SiGe BiCMOS technology [4]. Within this cutting edge technologies, Silicon Germanium (SiGe) heterojunction bipolar transistor (HBT) is one of the

major contributors towards the mmW and THz applications. SiGe HBTs became popular mainly because of the underlying BiCMOS technology that allowed a low-cost integration with the already available CMOS technology [5]. From the perspective of high-frequency (HF) applications, BiCMOS technology is proved to be superior to its CMOS counterpart in terms of performance, cost, and functional integration. Eventually, the SiGe BiCMOS found its applications in high-speed communication (like personal and local area networks to space and inter-satellite communication), automotive radar (from long-range radar (LRR) to industrial distance measurement and 3D scanning), and imaging (low-cost computed tomography (CT) to genetic screening), etc. [6] [7].

The state-of-the-art bipolar-only SiGe HBT fabricated using 130 nm technology from IHP offers $f_T/f_{max}/BV_{CEO}/\text{gate-delay}$ of 505 GHz/720 GHz/1.6 V/1.34 ps [8]; similarly, the SiGe HBT fabricated using 55 nm BiCMOS technology from STMicroelectronics delivers $f_T/f_{max}/BV_{CEO}/\text{gate-delay}$ of 325 GHz/375 GHz/1.5 V/2.34 ps [9]. In addition, studies by Schroter et al., [10] [11] revealed that the f_T/f_{MAX} values of SiGe HBTs in the near future will approach the THz range. Utilizing the potential of this promising technology lies in enabling a reliable circuit design that improves the possibility of first-pass success, thereby saving fabrication costs and time. This can be achieved by ensuring an accurate high-frequency SPICE model of such devices.

Prior to predicting the high-frequency behavior, a SPICE model is supposed to be accurate as far as the static (DC) and quasi-static behavior of the device is concerned. For SiGe HBTs, DC and quasi-static models are widely reported. Even investigation of non-quasi-static effects of devices fabricated using relatively older technologies are available in the literature; e.g., see [12] [13] for a detailed discussion. However, reports on the very high-frequency behavior of modern SiGe HBTs with very high f_T and f_{MAX} detailing their modeling challenges are limited [14] [15]. This may be caused partly by limited facilities available for very high-frequency measurements beyond 110 GHz, and/ or limited access to such devices capable of exhibiting f_T/f_{max} values beyond 300 GHz, and/ or lack of technology information and expertise. Instead, in most of the reported works, the modeling results are either compared with measurements carried out at low frequency or with TCAD results [16]. In this paper, we present an in-depth investigation of the high-frequency behavior (up to 330 GHz) of SiGe HBTs from the perspective of SPICE modeling that

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required us to overcome most of the limitations mentioned above.

With very high operating frequency, devices exhibit delays due to the onset of distributed effects. It is well known that the high-frequency operation of SiGes are made possible only at high current densities where f_T and f_{MAX} show their peaks. At high current densities, a substantial amount of minority carriers are diffused, and at this operating condition, if the devices are excited with a very high-frequency signal, the stored minority charges show delayed response to the input excitation. This delay in the stored charge is reflected in both the input and output terminal characteristics, constituting vertical input and output non-quasi-static (NQS) effects. These NQS effects are essentially linked with a 1-D intrinsic transistor. On the other hand, if the emitter width is significant, the DC emitter current crowding effect gives birth to AC current crowding or lateral NQS effect at high-frequency operation. This lateral NQS effect is a phenomenon occurring within the base where the majority holes exhibit a delay while travelling within the internal base region. Although the emitter widths of the modern SiGe HBTs are significantly scaled-down and therefore, DC emitter current crowding effects are hardly observed, the lateral NQS effect cannot be avoided due to very high frequency of operation. Such delays are a phenomenon confined to the internal transistor. As the frequency of operation increased with technological advancement, such delays became prominent, and model developers were provided with suitable solutions. However, for modern SiGe HBTs, the actual internal transistor is so much scaled down that various RC delays of the bulky external transistor structure tend to mask the internal transistor delays. Once the frequency of operation becomes very high, the vertical and lateral NQS delays are visibly observed.

The RC delays of the external transistor structures correspond to the distributed effects arising at high frequency in the access or parasitic regions of the transistor. As the dimension of the access region from the device terminals (base, emitter, collector, substrate) to the internal transistor increases, such delays become prominent. Base-to-emitter (BE) and base-to-collector (BC) access regions are physically partitioned across the external base resistance. Therefore, accurate partitioning of these parasitic capacitances are important to capture the distributed effects occurring in the access regions. Additionally, the substrate parasitic region also requires to be modeled appropriately in order to capture the distributed effect originating from the substrate guard ring p^+ contact, the deep-trench resistive access, peripheral capacitance, and PN -junction substrate capacitance [17].

This paper is organized as follows. Actual measurement procedure, TCAD calibration, and quasi-static modeling using HICUM have been demonstrated in the next section. In section III, the definition and extraction flow of the high-frequency related parameter is described, and in section IV, the parasitic capacitance parameter extraction is presented. Lateral NQS parameter extraction, including the sensitivity analysis of the parameters, and vertical NQS parameter optimization are demonstrated in section V. Finally, the paper is concluded by comparing the measurement data with the model considering

updated high-frequency parameters derived in this work.

II. HIGH-FREQUENCY CHARACTERIZATION AND TCAD CALIBRATION

Understanding the device behavior at a very high frequency requires an appropriate characterization setup. Although s -parameter measurements till 40 GHz is mostly available in academia and industry, now-a-days 110 GHz setup has also become common [18]. However, a measurement facility up to 330 GHz is not only rare, but setting up such a facility is quite challenging since it requires many additional equipment and care. For generic model development at an initial stage, TCAD simulation serves as a reference where calibration is not so critical. However, for model deployment of specific technology till very high frequency, if one has to understand the behavior of various structural contributions of a specific device (e.g., external and internal parts of SiGe HBTs), a calibrated TCAD simulation and subsequent investigation are necessary.

A. Characterization up to 330 GHz

We have carried out the s -parameter measurements up to 330 GHz in both cold bias conditions and the active operation range. The junction capacitance results are obtained from cold s -parameter measurement [19] [20]. In cold measurement, the transistor operates at a reverse bias to a very low forward bias with minimum carrier injection across the junctions [13]. Measurements were performed at three different bands to cover the frequency range from 1 GHz to 330 GHz. Agilent's E8361A VNA with extenders above 67 GHz is used for the 1 GHz to 110 GHz range. Measurement benches with 4-port Rohde and Schwarz ZVA24 VNA paired with extenders ZC220-ZC330 for the 140-220 GHz and 220-330 GHz frequency bands [21]. The power is maintained below -30 dBm at the ground-signal-ground probe tips across the entire frequency range, and the intermediate frequency band is set to 10 Hz. Cascade Infinity RF probes with 100 μm pitch are used for frequency range below 110 GHz, and 50 μm pitch is used above 110 GHz. We apply on-wafer TRL calibration with an impedance correction, followed by short-open de-embedding [22] [23]. The measurement data shown throughout this article are the results obtained from s -parameter characterization using the above-described setup at suitable bias conditions for SiGe HBTs with four different transistor geometries ($A_E = 0.2 \times 5\mu\text{m}^2$, $0.2 \times 10\mu\text{m}^2$, $0.3 \times 5\mu\text{m}^2$, and $0.42 \times 5\mu\text{m}^2$). Four different emitter geometries are chosen in order to be able to distinguish the lateral NQS delays from the overall transistor delays at high frequency.

B. TCAD Calibration

The SiGe HBT corresponding to the B55 process of STMicroelectronics is emulated (ref. Fig. 1) in commercially available Sentaurus TCAD environment [24]. All dimensions, including shallow trench isolation (STI), deep trench isolation (DTI), and doping profiles, are reproduced in TCAD simulation deck with approximately identical dimensions of the actual devices [25] [26]. During calibration, all physics-based

effects are accounted by including appropriate device models suitable for RF devices [27] [28]. The substrate region doping that plays a key role in the HF behavior of the device, is also appropriately calibrated [20].

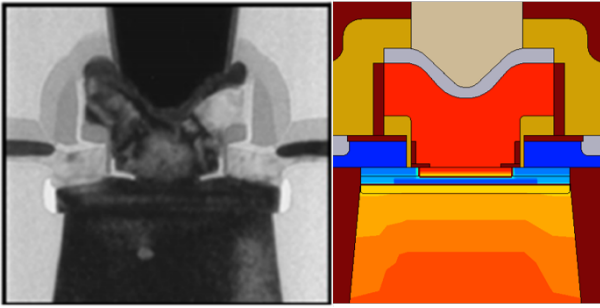


Fig. 1: TEM image of the SiGe HBT device (left) in the discussed technology, (right) mimicked TCAD Structure.

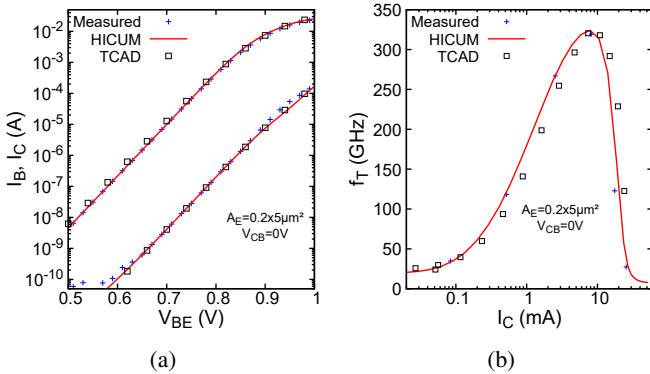


Fig. 2: TCAD and quasi-static HICUM model calibration for the device $A_E = 0.2 \times 5 \mu\text{m}^2$ at a bias condition of $V_{CB} = 0\text{V}$: (a) Gummel plot comparison, (b) collector current (I_C) dependent f_T extracted at a spot frequency of 64 GHz.

To solve the transport equations, the Hydrodynamic model is used. The Slootboom band gap narrowing model has been used to adjust the carrier concentration at heavy doping. Caughey-Thomas models with tuned parameters are used for considering the mobility effects. SRH and Auger models for recombination effects and the Lackner model for high-field effects are considered during calibration. The Gummel plot and extracted transit frequency (f_T) at $V_{CB} = 0\text{V}$ are shown in Fig. 2 to demonstrate the precise calibration of TCAD with measurements. In [29], a detailed explanation of the calibration procedure is reported, and the additional figures-of-merits (FoMs), including junction capacitances and f_{MAX} , are also demonstrated.

III. COMPACT MODELING USING HICUM

The compact model simulation has been carried out using HICUM L2/V2.3. Fig. 3(a) presents the large-signal equivalent circuit HICUM model for SiGe HBTs. As shown in Figs. 3(b) and (c), HICUM accounts for input and output NQS effects by including delays in excess stored charge (using an RC sub-circuit) and in transfer current (using another second-order

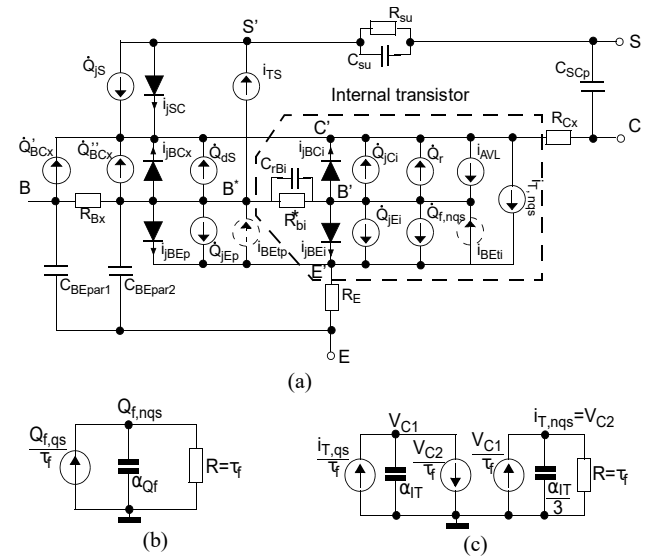


Fig. 3: (a) Large signal equivalent circuit of HICUM L2 compact model, (b)(c) adjunct networks for vertical NQS effects [13] [30].

RC sub-circuit with controlled sources), respectively [30]. The delayed stored charge and transfer current obtained from the sub-circuits are fed back to the main model equivalent circuit. On the other hand, the internal base resistance R_{Bi} (see Fig. 3(a)) takes care of the DC current crowding effect, and additionally the capacitance C_{RBi} placed in parallel to this R_{Bi} attempts to capture the delay caused by the lateral NQS effect at high operating frequency [30] (ref. Fig. 3(a)). This approach works well under small-signal operation [30] [31]. Indeed, C_{RBi} has been added to support accurate small-signal amplifier design. As long as the signal level generates low harmonic content, the use of C_{RBi} can be very useful. To additionally consider large-signal transients and preserve the accuracy of the small-signal high-frequency model, one needs a dynamic charge partitioning across R_{Bi} , on which the HICUM model developer is working presently (private communication with M. Schroter [32]). Other approaches use a multi-finger network to model the lateral NQS effect more accurately, as demonstrated in [33], or a two-section model that partitions the charge across the internal base resistance that shows relatively better accuracy both in small and large signal modeling [16] [34]. However, these approaches may not be preferred in HICUM implementation [33] due to increased simulation time and potential convergence issues. Besides the internal transistor structure, HICUM also includes the structural effects of the external transistor on the terminal electrical characteristics by including appropriate circuit elements in the overall equivalent circuit model. In Fig. 3(a), the elements within the dashed box correspond to the internal transistor, whereas all other elements represent the external transistor structure. Noticeably from the input or base terminal, the four elements C_{BEpar1} , C_{BEpar2} (base-to-emitter side) and Q'_{BCx} and Q'_{BCx} (base-to-collector side) across the external base resistance (R_{Bx}) can play crucial roles to contribute to the

overall RC delays in the terminal characteristics. Additionally, the delay contribution from R_{su} , C_{su} and C_{SCp} (from the substrate side) play a significant role in the high-frequency behavior of the transistor as was reported in [35].

Prior to the investigation at high-frequency, the junction capacitances, DC, and low-frequency model parameters of the HICUM model are extracted following the already available extraction recipe available in literature [36] [37]. A high-level model agreement is demonstrated in Fig. 2 in comparison with calibrated TCAD and measurement data. This is crucial before determining the high-frequency effects related parameters. The high frequency related parameters originating from the internal transistor are the so called vertical input NQS parameter **alqf** catering the delay in the stored minority charge, Q_f and vertical output NQS parameter **alit** to consider the delay in the transfer current, I_T . The lateral NQS parameter, **fcrbi** acts as a factor to the overall internal transistor capacitances appearing across the internal base resistance R_{Bi} to account for the lateral delay of the hole transport within the internal base region. The determination of these parameters requires one to simulate the intrinsic 1-D and internal 2-D transistors separately. From the perspective of measurements, these delays tend to be masked by the bulky external transistor. This is especially true for modern SiGe HBTs, where the internal transistor is scaled down significantly. The model parameters of interest relating to the external transistor are the partitioning factors, **fbepar** responsible for the partitioning of external B-E capacitance across the external base resistance, R_{Bx} and **fbepar**, partitioning the external B-C capacitance across R_{Bx} . Traditionally, the first-hand estimate of these partitioning factors is made from the geometry information of the device, and they may not play such a crucial role at not so high frequency as long as the overall external B-E and B-C capacitances are determined with considerable accuracy. To our experience, these factors play crucial roles when model accuracy is tested at a sufficiently high frequency. Since the external transistor will have a first-hand effect on the overall delay partially masking the delays originating from the internal transistor, in the following sections, we first investigate various ways to determine the parameters **fbepar** and **fbepar** prior to investigating the effects of **fcrbi**, **alqf** and **alit** on the overall high-frequency characteristics. We took the help of a calibrated TCAD deck, analytic equations, equivalent circuit models for device sections, and some sensitivity analysis methods to determine reliable values for the above-mentioned parameters.

IV. HF DELAY FROM EXTERNAL TRANSISTOR: PARASITIC CAPACITANCE PARTITIONING FACTORS

To our experience, the parameters, **fbepar**, and **fbepar**, are crucial for accurately modeling the high-frequency behavior of SiGe HBTs, especially beyond the 100 GHz frequency range. For these parameters, no reliable extraction procedure exists in the literature based on measurement data. Thus, using calibrated TCAD device analysis, **fbepar**, and **fbepar** are to be extracted. The extraction of **fbepar** has already been presented in [38], and the obtained value is 0.93 for this given technology. However, there are some issues with the

reported **fbepar** extraction. In the next section, we present the extraction of **fbepar** following calibrated TCAD simulation.

A. Determination of **fbepar** from TCAD simulation

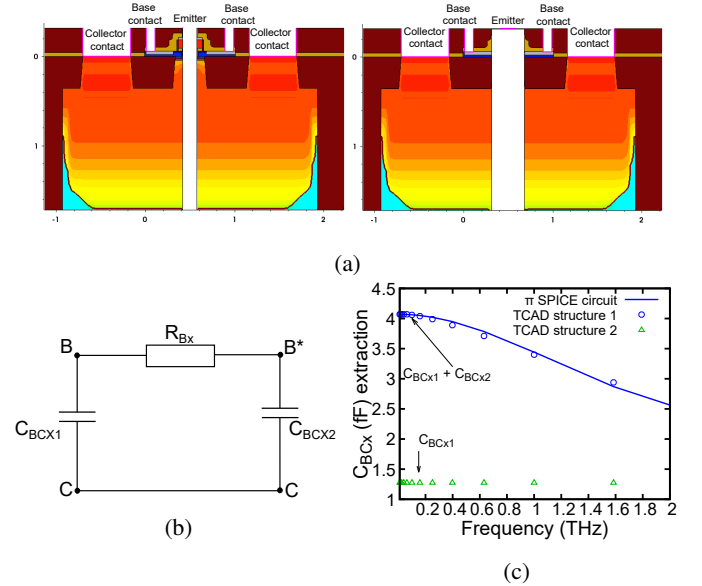


Fig. 4: (a) Customized TCAD structure for **fbepar** extraction (left) TCAD structure 1, (right) TCAD structure 2, (b) corresponding RC - equivalent circuit representing (a), and (c) frequency-dependent capacitance (C_{BCx} extracted from $\frac{-\text{imag}(y_{12})}{2\pi f}$) characteristics for **fbepar** extraction.

In HICUM, the total extrinsic BC-capacitance (C_{BCx}) originates from the charge components, Q'_{BCx} and Q''_{BCx} . The corresponding capacitance components are C_{BCx1} and C_{BCx2} , respectively (cf. Fig. 3). Each of these capacitance components is further divided into two parts: (i) the bias-dependent external BC junction capacitance (C_{JCx}) and (ii) the bias-independent parasitic BC capacitance ($C_{BC,par}$). In order to estimate the contribution of the $C_{BC,par}$, the TCAD structure corresponding to the device has been customized in two different patterns representing only the perimetric base-collector portion (ref. Fig. 4(a)). The first TCAD structure (Fig. 4(a) left) excludes the intrinsic transistor along with the emitter. This structure takes the form of a π -equivalent network consisting of extrinsic base resistance (R_{Bx}) and two partitioning capacitances C_{BCx1} , C_{BCx2} , as shown in Fig. 4(b). The capacitance could be obtained from the TCAD simulated y -parameters of this structure at $V_{BC}=0$ V. This capacitance shows a decreasing behavior with frequency (ref. Fig. 4(c)). From the low-frequency limit, the sum $C_{BCx1}+C_{BCx2}$ is directly obtained.

The second TCAD structure (Fig. 4(a) right) removes the device part at the end of the silicidation, resulting in negligible R_{Bx} . Doing so, this part of the structure represents only the contribution of C_{BCx1} . A frequency-dependent TCAD simulation of this structure shows that the capacitance associated with this region is constant up to several THz and thus confirms a negligible associated resistance. Therefore, this part can be

modeled by a simple capacitance C_{BCx1} of 1.2 fF (ref. Fig. 4(c)). Combining both the results, the values of $\mathbf{fbcpar} = C_{BCx2}/(C_{BCx1}+C_{BCx2})$ is calculated as 0.8 for this given technology.

Since R_{Bx} is dominated by the base link profile, the TCAD structure-2 (Fig. 4(a) right) almost removes R_{Bx} and C_{BCx2} . This helped us having a better estimate of \mathbf{fbcpar} . It was not the case in [34] where an attempt has been made to split the bias-independent oxide capacitance from the junction capacitance. With the new structure, we directly determine C_{BCx1} and C_{BCx2} at low frequency, reducing the overall uncertainty. This also removes any requirement of fitting the capacitance curve at a very high frequency. In [38], \mathbf{fbcpar} was 0.65, while here, we obtain 0.8.

B. Optimization of \mathbf{fbcpar} from HF Measurements

In the absence of any calibrated TCAD simulation, a backup solution for getting a value of \mathbf{fbcpar} requires one to optimize this parameter against the measured $\Re\{y_{12}\}$, as it is strongly correlated with the collector-base region. Notwithstanding the observed noise in measurement due to very low values of $\Re\{y_{12}\}$, an estimation is still possible. Moreover, this procedure is applied at cold conditions ($V_{BE}=V_{BC}=0$ V) to simplify the equivalent circuit model by canceling the diffusion charges altogether and thus accentuating the bias-independent parasitic BC capacitances. To confirm the sensitivity of $\Re\{y_{12}\}$ on \mathbf{fbcpar} values, the measurement and simulation with the standard model of STMicroelectronics are compared in Fig. 5 at $V_{BE}=0$ V and $V_{BC}=0$ V for three different \mathbf{fbcpar} values. We observe that $\Re\{y_{12}\}$ is quite sensitive to a variation of the \mathbf{fbcpar} value.

C. Extraction Using Analytical Model

A direct extraction method for \mathbf{fbcpar} and \mathbf{fbepar} parameters is presented here. This procedure is performed in two steps as presented in Fig. 6. Step-1 assumes a cold measurement configuration. Under this situation, the following simplifications can be made to the small-signal counterpart of the HICUM model. The small-signal transferred collector current element is replaced by an open, diffusion capacitance C_{DE} , C_{DC} are set to zero, implying that $C_{R_{Bi}}$ can also be neglected. As a final approximation, the emitter resistance, R_E is assumed negligible for the calculation. The resulting small-signal equivalent circuit of the transistor is presented in Fig. 7. At this point, we consider that some of the parameters are already obtained using conventional parameter extraction methods as described below for clarity.

- (i) The total BE capacitance (C_{BE}) is extracted from cold s -parameters measurements. To simplify the analysis in this step-1, we consider that all the external BE capacitance is gathered on the intrinsic transistor side (equivalent to $\mathbf{fbepar} = 1$). This approximation simplifies the following numerical analysis and avoids multiple solutions. To our experience we found that a simultaneous extraction of \mathbf{fbcpar} and \mathbf{fbepar} leads to unreasonable values.

- (ii) The intrinsic BC junction capacitance (C_{JCi}) and the total peripheral capacitance ($C_{BCX1} + C_{BCX2}$) are extracted from cold s -parameters and geometry scaling.
- (iii) The base resistance and its sharing between extrinsic (R_{Bx}) and intrinsic (R_{Bi}) components are extracted using tetrode structures having a different geometry [39].

The high-frequency analysis is always convenient using y -parameters. Thus, the detailed derivation of the y -parameter from the inner shell (y_i) to the outer shell (y_{iXX}) (as marked in Fig. 7) can be straightforwardly carried out by adding circuit elements after each step. The analytic expression for each component of the y -parameter matrix can be derived from the equivalent circuit. We are interested in y_{12} , since it is sensitive to \mathbf{fbcpar} parameter. The derived y_{12} -parameter reads

$$y_{12xx} = \frac{\frac{-j\omega C_{JCi}}{1+j\omega R_{Bi}C_J} - j\omega C_{BCX2}}{1 + R_{BX} \left(\frac{j\omega C_J}{1+j\omega R_{Bi}C_J} + j\omega C_{BCX2} \right)} - j\omega C_{BCX1} \quad (1)$$

where $C_J = C_{JEi} + C_{JCi}$, $C_{BCX} = C_{BCX1} + C_{BCX2}$, $C_{BCX2} = C_{BCX2} + C_{BEX2}$, $C_{BCX2} = \mathbf{fbcpar}C_{BCX}$, and $C_{BCX1} = (1 - \mathbf{fbcpar})C_{BCX}$. As observed from the extraction flow in Fig. 6, a prior information of C_{BE} , C_{JCi} , C_{BCX} and measured frequency-dependent y_{12} can be sufficient for one to solve (1) numerically and obtain \mathbf{fbcpar} . This numerical solution is obtained using Python.

Step-2 is executed after Step-1 with a reasonable value of \mathbf{fbcpar} in hand, as mentioned in Fig. 6. Now we can extend the equivalent circuit of Fig. 7 by considering total C_{BE} capacitance where along with the already included intrinsic component C_{JEi} , two more extrinsic components C_{BEX1} and C_{BEX2} are included on the two sides of R_{BX} as shown in Fig. 8. The extrinsic capacitors $C_{BEX1,2}$ are composed of a peripheral component C_{JEp} and C_{BEPar} . The capacitance partitioning factor \mathbf{fbepar} shares the parts of $C_{JEp} + C_{BEPar}$ at the two sides of R_{BX} as C_{BEX1} and C_{BEX2} (see Fig. 8). Again, a y -parameter expression can be obtained assuming this new equivalent circuit. As a result, one obtains $\Re\{y_{11}\}$ and $\Re\{y_{12}\}$ as

$$y_{11xxx} = \frac{\frac{j\omega C_J}{1+j\omega R_{Bi}C_J} + j\omega C_{BEX2}}{1 + R_{BX} \left(\frac{j\omega C_J}{1+j\omega R_{Bi}C_J} + j\omega C_{BEX2} \right)} + j\omega C_{BEX1} \quad (2)$$

$$y_{12xxx} = \frac{\frac{-j\omega C_{JCi}}{1+j\omega R_{Bi}C_J} + j\omega C_{BEX2}}{1 + R_{BX} \left(\frac{-j\omega C_J}{1+j\omega R_{Bi}C_J} + j\omega C_{BEX2} \right)} - j\omega C_{BCX1} \quad (3)$$

where $C_{BEX1} = (1 - \mathbf{fbepar})(C_{JEp} + C_{BEPar})$ and $C_{BEX2} = \mathbf{fbepar}C_{BCX}$. Other variables used in (2) and (3) are already defined after (1). Again, with a prior information of a few parameters and the contributions of BE capacitance components (C_{BEPar} , C_{JEp0} , C_{JEi0}), one can optimize \mathbf{fbepar} value by using both (2) and (3).

In order to verify the procedure, we use HICUM simulated with a set of predetermined input parameters. We choose a set of parameters with radically different values of (\mathbf{fbepar} , \mathbf{fbcpar}) as $\{(0.8, 0.2) (0.6, 0.6)\}$. A zero-bias y -parameter

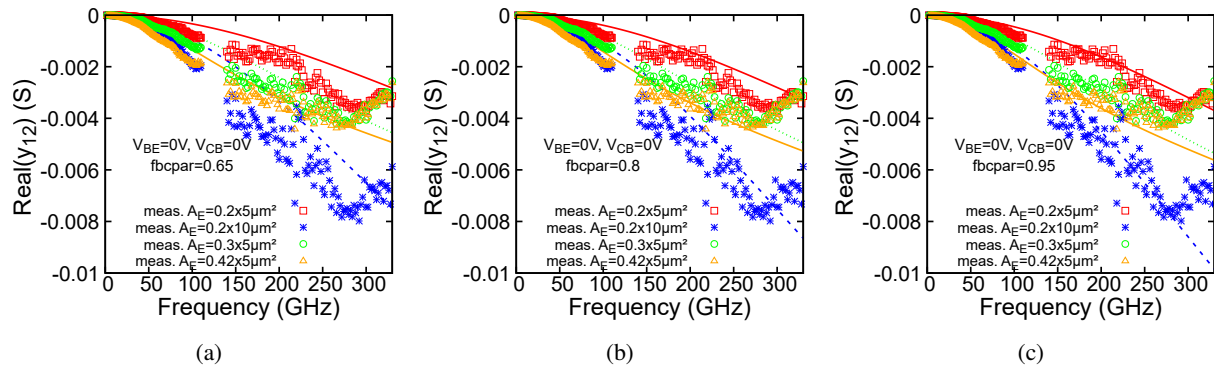


Fig. 5: $\Re\{y_{12}\}$ as a function frequency for four different device geometry, measurement data are represented by symbols, and the simulation data represents STMicroelectronics parameters set with (a) **fbcpair** = 0.65, (b) **fbcpair**= 0.8 (c) **fbcpair** = 0.95.

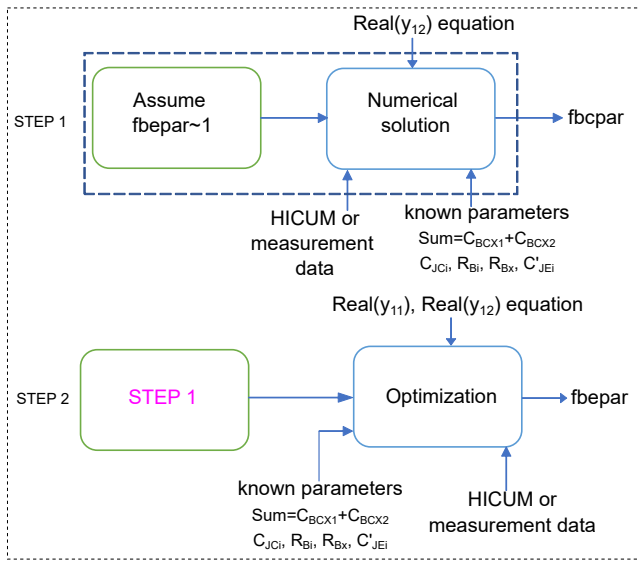


Fig. 6: Extraction flow for **fbepar** and **fbcpair**.

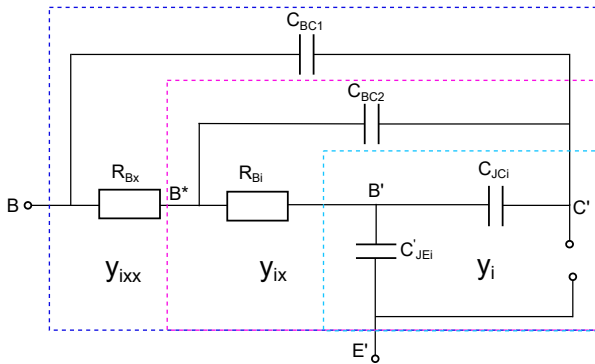


Fig. 7: Small-signal circuit schematic for **fbepar** extraction in step 1.

simulation is carried out, and the corresponding results are plotted in Fig. 9 for the two sets of parameters. The extraction of **fbepar** and **fbcpair** is quite straightforward and shows that the results are within 5 to 20% error depending on the frequency.

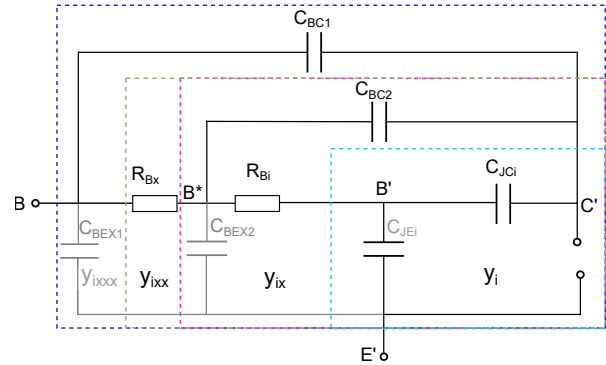


Fig. 8: Extended small-signal circuit schematic for **fbepar**, **fbcpair** extraction in step 2.

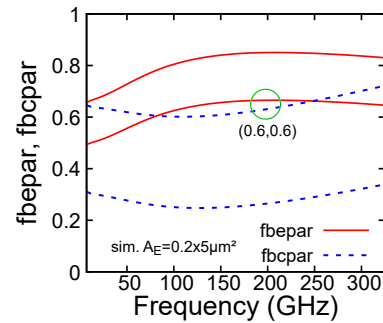


Fig. 9: Extraction of (**fbepar**, **fbcpair**) ((0.8, 0.2),(0.6,0.6)) for the $0.2 \times 5\mu\text{m}^2$ device using the extraction flow in Fig. 6. applied to HICUM simulation data for extraction procedure verification.

The same procedure is applied to the measurement data obtained from the SiGe HBT with $A_E = 0.2 \times 10\mu\text{m}^2$. This device is having the narrowest emitter width; hence it presents a smaller intrinsic part compared with the significant extrinsic part. Such a device is supposed to be more sensitive to the peripheral part leading to a higher sensitivity to **fbepar** and **fbcpair** parameters. On the other hand, this device is having the longest emitter length for which the noise and measurement inaccuracy are supposed to be relatively low. However, one has to be careful about measurement-related issues, especially at

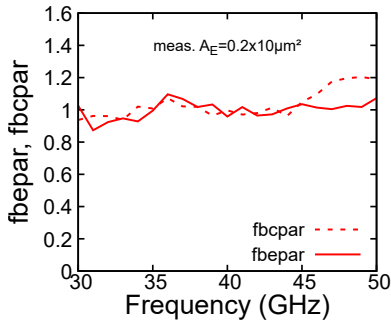


Fig. 10: Extraction of both **fbcpar** and **fbepar** from the measurement data for $0.2 \times 10\mu\text{m}^2$ device following the procedure described in Fig. 6.

high frequency. In this case, we found that due to measurement limitation, the outlined method works well up to 50 GHz (ref. Fig. 10) showing **fbcpar** and **fbepar** values above 0.9.

Thus, from all three methods presented so far (namely the ones using TCAD simulation, direct extraction, and optimization with measured $\Re\{y_{12}\}$ and $\Re\{y_{11}\}$ data), the values of **fbcpar** and **fbepar** converge within a range of 0.8 to 1. Overall we propose the following. If the model engineer has a TCAD tool with a well-calibrated structure, this method is relatively quick and safe to implement. Unfortunately, most of the time calibrated TCAD may not be available. In this case, we recommend a direct extraction as the first step for a quick result. Please note that the approach involves several approximations, and it is therefore advisable to optimize the parameters by finally fitting the to $\Re\{y_{12}\}$ and $\Re\{y_{11}\}$ characteristics.

V. HF DELAY FROM INTERNAL TRANSISTOR: NQS PARAMETERS

A. Lateral NQS Parameter Extraction

The distributed nature of the internal base region gives rise to the delay in lateral hole-flow, giving rise to the AC current crowding or the so-called lateral NQS effect at high-frequency operation [40]. The input impedance appearing at the base node can be considered as an open RC -transmission line. An equivalent circuit approximation is shown on Fig. 3 where an additional capacitance C_{RBi} shunting the DC resistance R_{Bi} is used to take care of this lateral NQS effect. This R_{Bi} - C_{RBi} network is in series with the total intrinsic vertical impedance and thus directly correlates all capacitance contributions to the internal base node.

To effectively model the lateral NQS effect, the **fcrb** parameter is introduced in HICUM as $fcrbi = C_{RBi}/(C_{JEi} + C_{JCi} + C_{DEi} + C_{DCi})$. All the capacitances mentioned here correspond to the junction and diffusion charge elements within the intrinsic 1-D transistor marked in Fig. 3. Here, C_{JEi} and C_{JCi} are the junction capacitances, and C_{DEi} and C_{DCi} refer to the diffusion capacitances of the intrinsic transistor. This section discusses the derivation of the accurate value of the associated NQS parameter **fcrb**. In view of the complexity of HICUM, in order to treat the problem analytically, it is

necessary to work with a simplified model for the extraction of **fcrb**.

Kloosterman *et al.* [41] used a simplified equivalent model to extract the internal base resistance as shown in Fig. 11(a). Now to introduce the lateral NQS effect, the same model and its corresponding equations can be modified, where the base resistor (R_B) has been replaced by an extrinsic base resistor (R_{Bx}) in series with the parallel combination of an internal series base resistor (R_{Bi}) and a capacitance C_{RBi} (ref. Fig. 11(b)). From the small signal equivalent circuit (ref. Fig. 11(a)), one can relate the total base resistance R_B with the small-signal hybrid h_{11} parameter as

$$Kh_{11}^* = \frac{1 + R_B \left(\frac{1}{r_\pi} + j\omega(C_\pi + C_\mu) \right)}{\frac{1}{r_\pi} + j\omega C_\pi} \frac{C_\pi}{C_\pi + C_\mu}, \quad (4)$$

where h_{11}^* is the corrected h_{11} and is defined as $1/(y_{11} + y_{12})$; K is defined as $\frac{C_\pi}{(C_\pi + C_\mu)}$. The capacitances, C_π and C_μ are extracted using the well known relationships, $C_\pi = \frac{g_m}{\omega} \Im \left(\frac{y_{11} + y_{12}}{y_{21} - y_{12}} \right)$ and $C_\mu = \frac{g_m}{\omega} \Re \left(\frac{y_{12}}{y_{21} - y_{12}} \right)$, respectively. The transconductance, g_m , can be extracted either from the low frequency y_{21} -parameter or from the DC measurement.

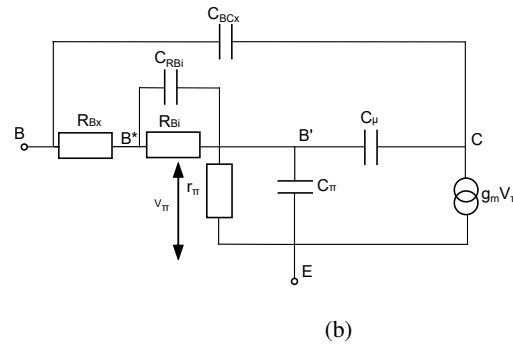
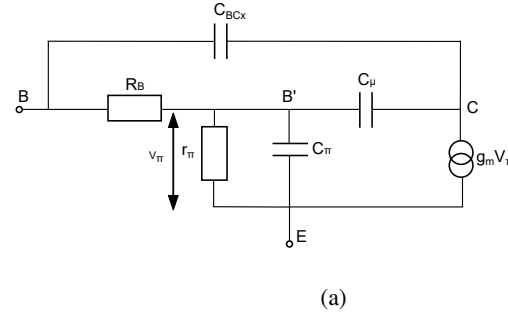


Fig. 11: (a) Small-signal equivalent schematic proposed in [41] for the extraction of the intrinsic and extrinsic base resistance, (b) Modified small signal equivalent schematic including the NQS effect for the extraction of C_{RBi} and **fcrb** parameter.

Multiplying the complex conjugate term in the denominator of eq. (4) yields $Kh_{11}^* =$

$$\frac{\frac{1}{r_\pi} + R_B \left(\frac{1}{r_\pi^2} + \omega^2 C_\pi C_{\pi,\mu} \right) - j\omega \left(\frac{R_B}{r_\pi} C_\pi + C_\pi \right)}{\frac{1}{r_\pi^2} + (\omega C_\pi)^2} X_R, \quad (5)$$

where $C_{\pi,\mu} = C_{\pi} + C_{\mu}$ and $X_R = \frac{C_{\pi}}{C_{\pi,\mu}}$. At frequencies greater than 10 GHz, we can neglect few terms in (5) since $\frac{1}{r_{\pi}^2} \ll (\omega C_{\pi})^2$, $\frac{1}{r_{\pi}^2} \ll \omega^2 C_{\pi} C_{\mu}$, $\frac{R_B}{r_{\pi}} \ll 1$ and the resultant simplified equation reads

$$Kh_{11}^* = \frac{[R_B(\omega(C_{\pi} + C_{\mu})) - j]}{\omega C_{\pi}} \frac{C_{\pi}}{C_{\pi} + C_{\mu}}. \quad (6)$$

Now following the equivalent of Fig. 11(a) given in Fig. 11(b), it is necessary to replace R_B in (6) with $R_{BX} + R_{Bi}/(1 + j\omega R_{Bi} C_{RBi})$.

Considering the imaginary part of the modified eq.(6) at high frequency, $(\omega C_{RBi} R_{Bi})^2 \gg 1$, C_{RBi} can be extracted from the measurement data. In order to fulfill this condition, it requires C_{RBi} to be large enough; therefore, it is necessary to bias the transistor at least in the medium to high injection regime ($0.8 \geq V_{BE} \leq 0.9$) while isolating the impact of both the emitter and collector access resistance and self-heating. Moreover, the chosen frequency must be higher than a few hundred GHz for the discussed technology, depending on the geometry of the transistor. Thus, at high frequency where the condition $(\omega C_{RBi} R_{Bi})^2 \gg 1$ is valid,

$$C_{RBi} \approx \frac{1}{\left(\frac{C_{\pi}}{C_{\pi} + C_{\mu}}\right) \left(\omega \text{Imag}(h_{11}^*) + \frac{1}{C_{\pi}}\right)}. \quad (7)$$

Until now, only the capacitance C_{RBi} is extracted. In order to extract the parameter **fcrbi**, we use the equations of the HICUM model [42], because of its relatively attractive simplifications for extracting the parameter. Thus, the complete equation is given as

$$fcrbi = \frac{C_{RBi}}{C_{JE} + C_{JC} + \frac{i_{TF}}{V_T} \tau_{f0} + \frac{i_{TR}}{V_T} \tau_r}. \quad (8)$$

1) *Application on Synthetic and Measurement Data:* To evaluate the robustness of the procedure, this method is applied to HICUM model where the parameter **fcrbi** is varied from 0.2 to 0.8 for two different devices with the widest emitter geometries (i.e., $0.3 \times 5\mu\text{m}^2$, and $0.42 \times 5\mu\text{m}^2$) where the impact of R_{Bi}/C_{RBi} is quite significant. The chosen bias point is $V_{BE}=0.85\text{V}$ and $V_{CB}=0\text{V}$, which is a trade-off to get a strong diffusion capacitance C_{DE} and so a large C_{RBi} value, while maintaining reasonably low self-heating and access resistors effects. It can be observed from Fig. 12(a) that for the device with $A_E = 0.3 \times 5\mu\text{m}^2$, lateral NQS starts to appear at a frequency around 600 GHz, which made the extraction procedure practically impossible with our measurement (limited up to 330 GHz). Also, we can observe that the curve does not show any plateau or convergence. However, applying the same procedure to the widest available device with $A_E = 0.42 \times 5\mu\text{m}^2$, the lateral NQS dominates, and the corresponding parameter extraction becomes reliable (ref. Fig. 12(b)). For example, for input **fcrbi** parameter values of 0.2 and 0.4, we extract 0.28 and 0.48, respectively; thus, confirming that only the widest (i.e., $0.42 \times 5\mu\text{m}^2$) transistor allows the extraction of this parameter reliably. A solution to this problem is to increase the bias voltage, which will increase the C_{RBi} without decreasing R_{Bi} too much, resulting in a reduced lateral NQS cut-off frequency.

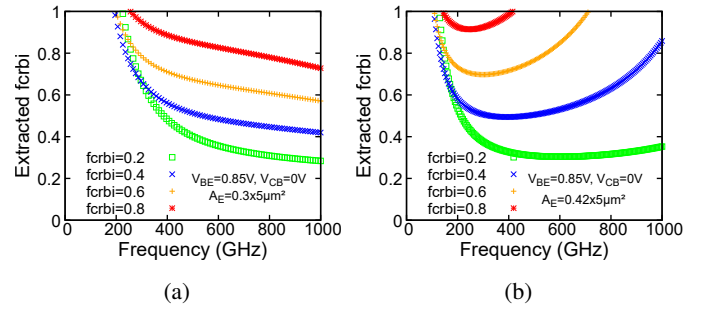


Fig. 12: Testing the **fcrbi** extraction for (a) $A_E = 0.3 \times 5\mu\text{m}^2$, (b) for $A_E = 0.42 \times 5\mu\text{m}^2$ at $V_{BE}=0.85\text{V}$, $V_{CB}=0\text{V}$.

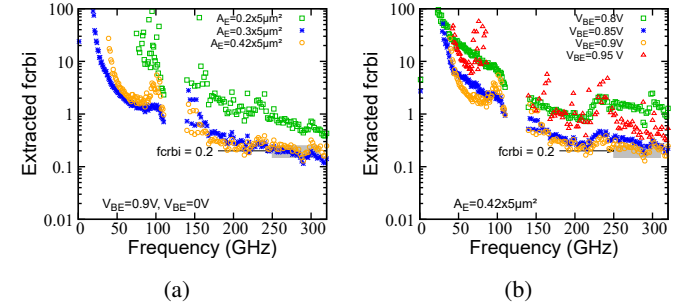


Fig. 13: Extraction of the **fcrbi** extraction from the measurement of (a) (left) three device geometries at $V_{BE}=0.9\text{V}$, $V_{CB}=0\text{V}$, (b) (right) for the widest device $A_E = 0.42 \times 5\mu\text{m}^2$ at different bias.

In Fig. 13(a), the parameter **fcrbi** is extracted for three devices measured at $V_{BE}=0.9\text{V}$ and $V_{BC}=0\text{V}$. It can be observed that for the two widest geometries ($0.3 \times 5\mu\text{m}^2$, $0.42 \times 5\mu\text{m}^2$), it results in a consistent value of **fcrbi**=0.2 which matches exactly the theoretical expectations [30] [42]. It also concludes that the narrowest device ($0.2 \times 5\mu\text{m}^2$) does not allow to extract **fcrbi** correctly, even in the high injection regime (at $V_{BE}=0.9\text{V}$).

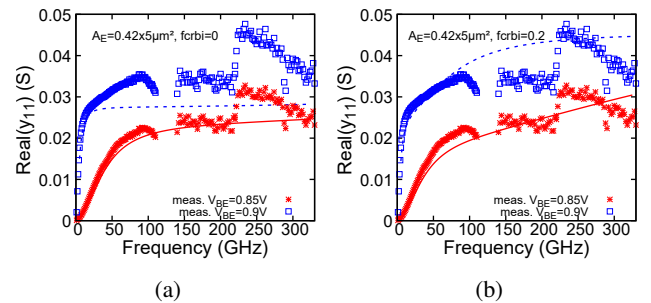


Fig. 14: $\Re\{y_{11}\}$ as a function of frequency for four different bias (V_{BE}) for the device with geometry $A_E = 0.42 \times 5\mu\text{m}^2$ (a) at **fcrbi** = 0, and (b) the new updated **fcrbi** = 0.2.

2) *Extraction Through Optimization of Measurement Data:* A second way to estimate the **fcrbi** parameter is by following the optimization procedure on $\Re\{y_{11}\}$. Fig. 14(a) shows both the measured and simulated $\Re\{y_{11}\}$ data for the widest device ($0.42 \times 10\mu\text{m}^2$) with **fcrbi**=0 at different biases. Here, we can observe that the model does not fit well at **fcrbi**=0. Now,

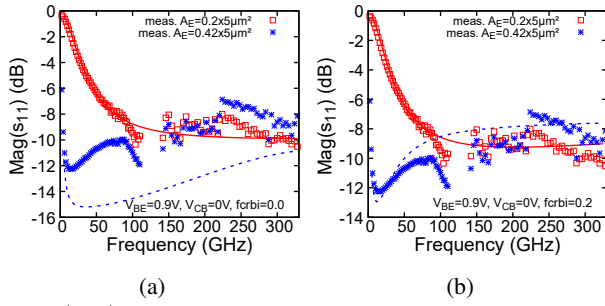


Fig. 15: $|s_{11}|$ characteristics for different geometries both from measurement and HICUM at $V_{BE}=0.9V$, $V_{CB}=0V$ when (a) $\mathbf{fcrbi}=0$ and (b) $\mathbf{fcrbi}=0.2$.

changing its value to 0.2 (shown in Fig. 14(b)) improves the model fitting and confirms the accuracy of the theoretical value derived in the last section. A similar test has been carried out for two different device geometries at different biases considering $|s_{11}|$, which is handy for circuit designers. It can be observed from Fig. 15 that the optimization suggests a global \mathbf{fcrbi} value of 0.2 for all the geometries discussed in this work.

B. Vertical NQS Parameter Optimization

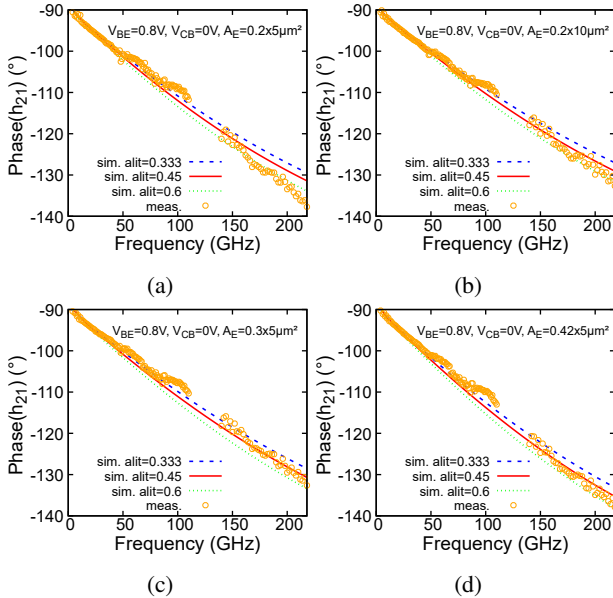


Fig. 16: $\angle h_{21}$ vs. frequency characteristics at $V_{BE}=0.8V$ and $V_{CB}=0V$ for four different devices (a) $0.2 \times 5\mu m^2$, (b) $0.2 \times 10\mu m^2$, (c) $0.3 \times 5\mu m^2$, (d) $0.42 \times 5\mu m^2$. The simulation corresponds to \mathbf{alit} values of 0.333, 0.45, and 0.6. Please note that the other parameters studied in this work are updated during this optimization, and hence the used values are $\mathbf{fbepar}=0.93$, $\mathbf{fbcpar}=0.95$, $\mathbf{fcrbi}=0.2$.

From classical transistor theory, it is well known that at high frequency, the minority charge and the transfer current give a delayed response with respect to the applied bias. This effect is coined as vertical NQS effect, and it has been introduced in HICUM with the help of \mathbf{alit} and \mathbf{alqf} parameters. The

study on \mathbf{alqf} determination in [38] is satisfactory; hence not included in this work. Concerning \mathbf{alit} extraction, there are two possible options: (i) using the TCAD method or (ii) using an optimization procedure on the $\angle h_{21}$ parameter. In [38], it is extracted using TCAD following transient simulation. However, this method has some shortcomings related to the need for an extremely high level of calibrated TCAD simulation deck; hence, the results can be misleading, and also, the collector current as a function of time does not allow for isolating the delay related to the input RC circuits (R_{Bx} , R_{Bi} , C_{Jci} , C_{Jei} , C_{DE} , and C_{DC}) and lateral NQS effects from the vertical NQS delay. Hence, there is a need for 1-D device simulation to ensure an exclusion the influence of other delays; however, it is a cumbersome task to rebuild the 1-D compact model of the transistor. Hence, it is wise to choose an optimization procedure on the measurement data. Therefore, for the \mathbf{alit} parameter, optimization of $\angle h_{21}$ is the preferred method.

In Fig. 16, the measured $\angle h_{21}$ data is compared with HICUM simulated $\angle h_{21}$ at $V_{BE}=0.8V$ and $V_{CB}=0V$ for the chosen four different geometries at three different \mathbf{alit} values 0.333, 0.45, and 0.6. From the observation, 0.45 is the most accurate parameter over the frequency range of interest. It is important to note that during the comparison, two uncertainties must be considered: (i) the quasi-static model must be precisely calibrated to ensure a focused study at the high-frequency, and (ii) the accuracy of the measurement is uncertain in the range of 70-110 GHz range due to coupling related to the probes. Moreover, beyond 0.85V, the resistive effect starts influencing V_{BE} ; thus, the analysis is limited up to $V_{BE}=0.85V$. Regarding the interplay with the effects described by \mathbf{fcrbi} and \mathbf{fbcpar} we recommend to optimize \mathbf{alit} at low injection levels on the narrowest geometries (close to 1D structure). For example, in the present case, the bias for optimization of \mathbf{alit} should be chosen at $V_{BE}=0.8V$.

VI. DISCUSSIONS AND CONCLUSION

In this paper, an in-depth investigation of the high-frequency model of the devices fabricated with STMicroelectronics's 55 nm SiGe HBT technology up to 330 GHz has been carried out. The works reported in [14] [15] up to such high frequency were either limited to some parameters that pose less difficulty to characterize, like s_{21} , h_{21} , $|U|$, or limited to a single frequency band. The work in [38] has some limitations, which are discussed in this work and resolved. Notably, this work is focused on the extraction of parameters devoted to modeling non-quasi-static (\mathbf{fcrbi} , \mathbf{alit}) and the parasitic capacitance partitioning factors (\mathbf{fbepar} , \mathbf{fbcpar}) that play a critical role above 100 GHz. For the first time, using both high-frequency calibrated TCAD structure, calibrated HICUM, and other small-signal SPICE models, the analysis is done, parameters are extracted, and the sensitivity of the parameters on concerned device characteristics is tested up to very high-frequency.

The parasitic capacitance partitioning factors (\mathbf{fbepar} , \mathbf{fbcpar}) describing complex distributed capacitance behavior is extracted using customized TCAD and are optimized by applying a novel numerical solution method on highly sensitive measurement data for $\Re\{y_{11}\}$ and $\Re\{y_{12}\}$. The \mathbf{fcrbi}

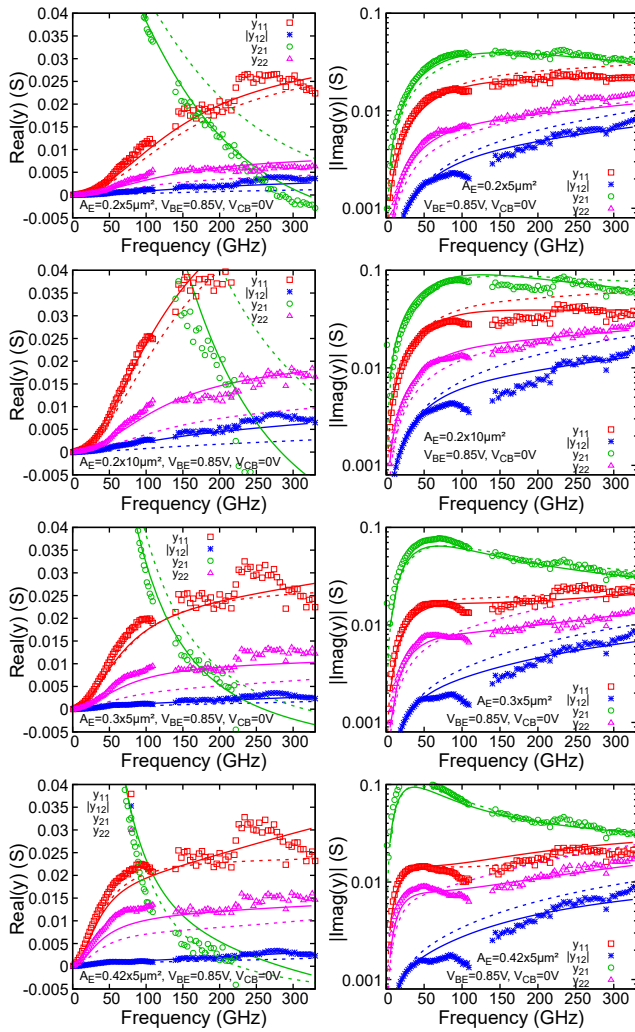


Fig. 17: Comparison of y -parameters as a function of frequency at $V_{BE}=0.85V$, $V_{CB}=0V$ (near peak f_T) for four different transistor geometries. Symbols represent the measurement data, and corresponding dashed lines represent the HICUM simulation with the default calibrated parameter set ($fcrbi = 0$, $fbepar=0$, $fbcpar=0$, $alit= 0$), and solid lines represent the parameter set extracted in this study ($fcrbi = 0.2$, $fbepar=0.93$, $fbcpar=0.95$, $alit= 0.45$).

parameter is extracted using a modified small-signal equivalent circuit model given by [41]. The extracted theoretical value is 0.2, different from the initial guess value of 0. The sensitivity study on the measured data confirms the new $fcrbi$ value of 0.2. This extraction method works significantly well for the widest device with $A_E=0.42 \times 5\mu m^2$. But for the devices with $A_E=0.3 \times 5\mu m^2$, we need to extend the work above 500 GHz to extract the correct parameter value. The effect of the $fcrbi$ parameter is more visible on the s_{11} parameter, and it has notable importance for impedance matching during the design of a circuit, particularly on the widest transistors and/or at high injection. Similarly, for the extraction of the vertical NQS parameter, $alit$, an optimization method is followed with respect to $\angle h_{21}$. The study also suggests that for the extraction of $alit$, the device must be operating at not too high injection levels. Finally, Fig. 17 demonstrate the improvement

of the modeling in the high-frequency range with the updated parameter values studied in this work. In conclusion, the study gives a recipe for high-frequency parameter extraction for SiGe HBTs in the frequency range above 100 GHz.

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REFERENCES

- [1] S. Lee et al., "9.5 An 80Gb/s 300GHz-Band Single-Chip CMOS Transceiver," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 170-172.
- [2] H. Hamada et al., "Millimeter-wave InP Device Technologies for Ultra-high Speed Wireless Communications toward Beyond 5G," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 9.2.1-9.2.4.
- [3] M. Seo, A. S. H. Ahmed, U. Soyulu, A. Farid, Y. Na and M. Rodwell, "A 200 GHz InP HBT Direct-Conversion LO-Phase-Shifted Transmitter/Receiver with 15 dBm Output Power," 2021 IEEE MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 2021, pp. 378-381.
- [4] M. H. Eissa, N. Maletic, E. Grass, R. Kraemer, D. Kissinger and A. Malignaggi, "100 Gbps 0.8-m Wireless Link based on Fully Integrated 240 GHz IQ Transmitter and Receiver," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 627-630.
- [5] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications," IEEE Transactions on Microwave Theory and Techniques, vol. 46, no. 5, pp. 5725-5729, 1998.
- [6] U. R. Pfeiffer and E. Javorsky, "Terahertz imaging with CMOS/BiCMOS process technologies," in 2010 Proceedings of ESSCIRC, IEEE, 2010, pp. 5260.
- [7] T. S. Rappaport, Y. Xing, O. Kanhere, S. Ju, A. Madanayake, S. Mandal, A. Alkhatieb, and G. C. Trichopoulos, "Wireless communications and applications above 100 GHz: Opportunities and challenges for 6G and beyond," IEEE access, vol. 7, pp. 78 72978 757, 2019.
- [8] B. Heinemann, H. Rucker, R. Barth, F. Barwolf, J. Drews, G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel et al., "SiGe HBT with f_x/f_{max} of 505 GHz/720 GHz," in 2016 IEEE International Electron Devices Meeting (IEDM). IEEE, 2016, pp. 31.
- [9] P. Chevalier, G. Avenier, G. Ribes, A. Montagne, E. Canderle, D. Celi, N. Derrier, C. Deglise, C. Durand, T. Quemerais et al., "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz $f_T/370$ GHz f_{MAX} HBT and high-Q millimeter-wave passives," in 2014 IEEE international electron devices meeting. IEEE, 2014, pp.39.
- [10] M. Schroter, G. Wedel, B. Heinemann, C. Jungemann, J. Krause, P. Chevalier, and A. Chantre, "Physical and electrical performance limits of high-speed SiGe HBTs Part I: Vertical scaling," IEEE Transactions on Electron Devices, vol. 58, no. 11, pp. 3687-3696, 2011.
- [11] M. Schroter and A. Chakravorty, "A geometry scalable physics-based compact bipolar transistor model," IEICE Trans. Electronics, Special Issue on Analog Circuit and Device Technologies, vol. 88, no. 6, pp. 10981-1113, 2005.
- [12] R. Pritchard, "Two-dimensional current flow in junction transistors at high frequencies," Proceedings of the IRE, vol. 46, no. 6, pp. 1152-1160, 1958.
- [13] A. Chakravorty et al., "Compact hierarchical bipolar transistor modeling with HICUM," World Scientific, 2010.
- [14] S. P. Voinescu, E. Dacquay, V. Adinolfi, I. Sarkas, A. Balteanu, A. Tomkins, D. Celi, and P. Chevalier, "Characterization and modeling of an SiGe HBT technology for transceiver applications in the 100-300-GHz range," IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 12, pp. 4024-4034, 2012.

- [15] L. Galatro, A. Pawlak, M. Schroter, and M. Spirito, Capacitively loaded inverted CPWs for distributed TRL-based de-embedding at (sub) mm-waves, *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 49144924, 2017.
- [16] S. Yadav, A. Chakravorty, and M. Schroter, Modeling of the lateral emitter-current crowding effect in SiGe HBTs, *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 41604166, 2016.
- [17] B. Saha, S. Fregonese, S. R. Panda, A. Chakravorty, D. Celi, and T. Zimmer, Collector-substrate modeling of SiGe HBTs up to THz range, in 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS). IEEE, 2019, pp. 14.
- [18] S. Fregonese, M. Deng, M. Cabbia, C. Yadav, M. De Matos, and T. Zimmer, THz characterization and modeling of SiGe HBTs: review, *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 13631372, 2020.
- [19] S. Fregonese, M. Deng, M. De Matos, C. Yadav, S. Joly, B. Plano, C. Raya, B. Ardouin, and T. Zimmer, Comparison of on-wafer TRL calibration to ISS SOLT calibration with open-short de-embedding up to 500 GHz, *IEEE Transactions on Terahertz Science and Technology*, vol. 9, no. 1, pp. 8997, 2018.
- [20] S. R. Panda, M. Cabbia, M. Deng, S. Fregonese, C. Yadav, A. Chakravorty, and T. Zimmer, SiGe HBT Device Characterization up-to 500 GHz: Procedure and Layout Improvement of Calibration Standards, in 2020 5th IEEE International Conference on Emerging Electronics (ICEE). IEEE, 2020, pp. 14.
- [21] S. Fregonese, M. Cabbia, C. Yadav, M. Deng, S. R. Panda, M. De Matos, D. Celi, A. Chakravorty, and T. Zimmer, Analysis of high-frequency measurement of transistors along with electromagnetic and SPICE cosimulation, *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 47704776, 2020.
- [22] M. Cabbia, M. Deng, S. Fregonese, M. De Matos, D. Celi, and T. Zimmer, In-situ calibration and de-embedding test structure design for SiGe HBT on-wafer characterization up to 500 GHz, in 2020 94th ARFTG Microwave Measurement Symposium (ARFTG). IEEE, 2020, pp. 14.
- [23] C. Yadav, S. Fregonese, M. Cabbia, M. Deng, M. De Matos, and T. Zimmer, S-Parameter Measurement and EM Simulation of Electronic Devices towards THz frequency range, in 2022 IEEE 34th International Conference on Microelectronic Test Structures (ICMTS). IEEE, 2022, pp. 14.
- [24] J. Korn, H. Rucker, and B. Heinemann, Experimental verification of TCAD simulation for high-performance SiGe HBTs, in 2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF). IEEE, 2017, pp. 9496.
- [25] T. Van Vu, D. Celi, T. Zimmer, S. Fregonese, and P. Chevalier, Advanced Si/SiGe HBT architecture for 28-nm FD-SOI BiCMOS, in Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2016 IEEE, 2016.
- [26] S. R. Panda, S. Fregonese, A. Chakravorty, and T. Zimmer, TCAD simulation and assessment of anomalous deflection in measured Sparameters of SiGe HBTs in THz range, in 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS). IEEE, 2019, pp. 14.
- [27] G. Sasso, Transport models and advanced numerical simulation of silicon-germanium heterojunction bipolar transistors, *Universita degli Studi di Napoli Federico II*, 2010.
- [28] S. R. Panda, S. Fregonese, P. Chevalier, A. Chakravorty, and T. Zimmer, A TCAD-Based Analysis of Substrate Bias Effect on Asymmetric Lateral SiGe HBT for THz Applications, *IEEE Transactions on Electron Devices*, 2023.
- [29] S. R. Panda, S. Fregonese, M. Deng, A. Chakravorty, and T. Zimmer, TCAD and EM co-simulation method to verify SiGe HBT measurements up to 500 GHz, *Solid-State Electronics*, vol. 174, p. 107915, 2020.
- [30] M. Schroter, A. Pawlak, and A. Mukherjee, HICUM/L2 a geometry scalable physics-based compact bipolar transistor model, *Documentation*, 2017.
- [31] A. Koldehoff, M. Schroter, and H.-M. Rein, A compact bipolar transistor model for very-high-frequency applications with special regard to narrow emitter stripes and high current densities, *Solid-State Electronics*, vol. 36, no. 7, pp. 10351048, 1993.
- [32] M. Schroter, Private communication about HICUM-productization and support update, 2023.
- [33] M. Schroter and M. Krattenmacher, Modeling distributed dynamic lateral large-signal switching effects in bipolar transistors, in 2019 IEEE 19th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF). IEEE, 2019, pp. 14.
- [34] S. Ghosh, S. Yadav, and A. Chakravorty, Modeling Dynamic Lateral Current Crowding in SiGe HBTs, 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), pp. 224227, 2022, IEEE.
- [35] S. Fregonese, D. Celi, T. Zimmer, C. Maneux, and PY. Sulima, A scalable substrate network for compact modeling of deep trench insulated HBT, *Solid-state electronics*, vol. 49, no. 10, pp. 1623–1631, 2005, Elsevier.
- [36] B. Ardouin, T. Zimmer, H. Mnif, and P. Fouillat, Direct method for bipolar base-emitter and base-collector capacitance splitting using high frequency measurements, in Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No. 01CH37212). IEEE, 2001, pp. 114117.
- [37] S. Fregonese, S. Lehmann, T. Zimmer, M. Schroter, D. Celi, B. Ardouin, H. Beckrich, P. Brenner, and W. Kraus, A computationally efficient physics-based compact bipolar transistor model for circuit Design-part II: parameter extraction and experimental results, *IEEE transactions on electron devices*, vol. 53, no. 2, pp. 287295, 2006.
- [38] B. Saha, S. Fregonese, A. Chakravorty, S. R. Panda, and T. Zimmer, Sub-THz and THz SiGe HBT Electrical Compact Modeling, *Electronics*, vol. 10, no. 12, p. 1397, 2021.
- [39] M. Schroter and A. Pawlak, Analysis of the transistor tetrode-based determination of the base resistance components of bipolar transistors a review, *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 820828, 2018.
- [40] M. Versleijen, Distributed high frequency effects in bipolar transistors, in Proceedings of the 1991 Bipolar Circuits and Technology Meeting. IEEE, 1991, pp. 8588.
- [41] W. Kloosterman, J. Paasschens, and D. Klaassen, Improved extraction of base and emitter resistance from small signal high frequency admittance measurements, in Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No. 99CH37024). IEEE, 1999, pp. 9396.
- [42] M. Schroter, A. Pawlak, A. Mukherjee, D. Celi and M. Krattenmacher, HICUM/L2: Extensions over the last decade, in 2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). IEEE, 2020.