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Maskless patterned plasma fabrication of interdigitated back contact silicon heterojunction solar cells: Characterization and optimization

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A B S T R A C T

We demonstrate a novel method to fabricate passivated interdigitated back contact (IBC) crystalline silicon solar cells incorporating a maskless, patterned plasma etching step. After deposition in a plasma-enhanced chemical vapor deposition (PECVD) chamber, the intrinsic and doped hydrogenated amorphous silicon and microcrystalline silicon layers (necessary for the passivated interdigitated contacts in such heterojunction technology (HJT) devices) are patterned via a single, maskless etching step, also performed in a PECVD chamber. The patterning step relies on selectively lighting an etching plasma within slits in the patterned powered electrode when it is placed very close to the substrate. The process flow is characterized and optimized at each step using spectroscopic ellipsometry, photoluminescence, and surface photovoltage mapping. It is shown that a critical step is the removal of a damaged layer formed on the surface after the patterned etching. Without this step, the IBC-HJT solar cells systematically exhibit S-shaped curves in their current-voltage (I - V) characteristics (giving fill factors below 25%). Once this critical step is included, the solar cells display I - V curves with fill factors above 65%, demonstrating the advantage of the maskless plasma patterning process.

1. Introduction

A promising architecture to bring laboratory record efficiencies for crystalline silicon (c-Si) solar cells to commercial modules combines two technologies that are each, individually, already commercially available for many years. The first is the interdigitated back contact (IBC) diffused-junction structure, as developed in the 1970s [1]. It has been commercialized predominantly by SunPower since 1985 (setting many efficiency records along the way [2,3]), and is currently sold by two major module manufacturers [4–6], whilst others have also demonstrated manufacturability on a pilot line scale [7].

The second technology is the use of hydrogenated amorphous silicon (a-Si:H) deposited using plasma enhanced chemical vapor deposition (PECVD) as the passivation and doping layers (variously called heterojunction technology (HJT) or heterojunction with intrinsic thin layer (HIT) structures). This technology was brought to the forefront by Sanyo/Panasonic [8], and is currently commercialized by multiple

companies [9,10].

When IBC and HJT concepts are used together [11], as first proposed in 2007 [12], the benefits of each technology complement each other. As demonstrated by Kaneka [13,14], they can operate with an efficiency (26.7%) that was, for a time, the pinnacle of single junction c-Si technology. However, this combination of IBC + HJT technologies has very little presence on the market [10] due to the combined cost of PECVD processes, and the patterning required for IBC cells.

Laboratory and industrial research activities around the world are attempting to increase this combined architecture's market share. These activities include simplifying the fabrication process by introducing a single patterned etching step using a hard mask [15], or otherwise avoiding lithography altogether by patterning the IBC using laser-ablation or -annealing [16–18], or shadow masking during deposition [19–22].

In recent work, we have demonstrated a promising technique to avoid having to do lithography or use a shadow mask when patterning

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semiconductor layers on a substrate. Said technique employs a custom radiofrequency (RF) powered electrode containing slits to selectively light a plasma only in the areas where the desired process should occur. In this way, a large area plasma process can directly be used for patterned deposition or etching in a PECVD chamber [23,24] without ever contacting the surface. In this work, we demonstrate the use of this patterned plasma processing technique to fabricate IBC-HJT solar cells.

2. Experimental details

2.1. Process description

Device Architecture - The architecture and the necessary process steps to fabricate the IBC-HJT solar cells studied in this work are depicted in Fig. 1. The specific technical details of each process step is then further discussed below.

As shown in Fig. 1(a), step (1) is a blanket deposition of an intrinsic (i) a-Si:H passivation layer on both sides of a n-type (n) c-Si wafer, followed by a stack of three layers: an (n) a-Si:H layer (which will eventually form the N-contact), an n-type microcrystalline silicon ((n) μ c-Si:H) layer, and finally a p-type (p) μ c-Si:H layer. The (n) a-Si:H layer is necessary to maintain good passivation while being an effective electron-selective contact. The last two (p) μ c-Si:H and (n) μ c-Si:H layers will form a recombination junction that allows current flow, specifically electron flow out of the N-contact.

In step (2), these layers are locally etched away in selected areas down to the (i) a-Si:H layer. Finally, a blanket p-type (p) a-Si:H layer is deposited, and aluminum contacts are deposited by evaporation (step (3)). The metallic contact in the etched area is the P-contact, as the first doped material the (n) c-Si sees in this area is (p) a-Si:H. The metallic contact in the non-etched area is therefore the N-contact, as the first doped layer the (n) c-Si sees is (n) a-Si:H.

If one considers the path of the dashed line shown for step (3), one can draw the energy band diagram of Fig. 1(b), which represents the barriers seen by electrons and holes created in (n) c-Si. Electron-hole pairs generated in the (n) c-Si are selectively removed, as the holes can flow to the (p) a-Si:H, and the electrons flow to the (n) a-Si:H. The electrons are then transferred through the (n)/(p) μ c-Si:H recombination junction by recombining with a hole coming from the surface (p) a-Si:H layer, completing the circuit. This architecture is conceptually similar to that presented in Ref. [20], in which they produce a similar structure using a shadow mask within the capacitively-coupled PECVD chamber during deposition.

The next sections describe the details of each of these processing steps in practice.

Blanket deposition - The blanket processes are done in two semi-industrial capacitively-coupled PECVD tools (INDEOtec OCTOPUS and NEXTRAL), both with RF excitation at 13.56 MHz. The wafers used are 4-inch double side polished float-zone wafers from TOPSIL (<100>

thickness 280 μ m, resistivity 1–5 Ohm-cm, with bulk minority carrier lifetimes greater than 2 ms).

After dipping the wafer in HF for 30 s to remove the native oxide, the layers depicted in step (1) of Fig. 1(a) are deposited at 180 $^{\circ}$ C in the OCTOPUS tool. The thicknesses of all the layers in this stack are as follows: (i) a-Si:H (20 nm) front and back, (n) a-Si:H (11 nm), (n) μ c-Si:H (15 nm), and (p) μ c-Si:H (40 nm). After these layers were deposited (after step (1)), the minority carrier lifetime was measured and was found to be of the order of 1 ms.

After the patterned etching (described in the next section), a 30 nm thick (p) a-Si:H is deposited at 250 $^{\circ}$ C in the NEXTRAL tool.

Patterned Etching - The most novel and critical process step in this architecture is the contactless and maskless patterned etching. This process is achieved through the use of a custom RF powered electrode in a capacitively-coupled PECVD reactor [23,24]. The particularity of this electrode is that it contains five slits of 1 mm wide and 60 mm long (and 10 mm apart), positioned in the location desired for etching, as shown in Fig. 2(a). The electrode is placed in proximity to the substrate (0.3 mm), as depicted in Fig. 2(b). At this distance, a plasma cannot light in any area other than the position of the slits. Therefore, the plasma is localized within the slits, and so the plasma processing step (in this case, an etching step) is localized to the area underneath the slits.

In this work, the patterned etching process is carried out in a lab scale single chamber PECVD tool. It contains a cylindrical plasma confinement vessel (grounded), and the patterned RF (13.56 MHz) powered electrode is positioned parallel with the grounded electrode, at an inter-electrode distance of 300 μ m. The etching is performed at ambient temperature using a gas mixture of Ar and NF₃, and the process pressure used is 10 Torr.

Due to the hollow cathode effect [25,26], the plasma which ignites within the slits under these conditions is very intense, and the resulting process can be very fast (etch rate up to 250 $\text{\AA}/\text{s}$). While this is very appealing from a throughput point of view, it can also result into reproducibility issues at lab scale. Indeed, if one aims to stop etching at the 20 nm thick (i) a-Si:H (as shown in step (2) of Fig. 1), this gives an etch stop window of 0.8 s. To slow the process down to allow for a manageable etch stop point, a pulsed operation was instead used. As an example, the effect of pulsing was examined by etching the (n) c-Si wafers with a 100 W RF (13.56 MHz) power pulsed at 1 kHz with duty cycle varying from 0.5% to 10%. As one can see in Fig. 3, the etch rate shows almost a linear increase as a function of the duty cycle. Using duty cycles below 3–4% allows one to slow the etch rate down to below 10 $\text{\AA}/\text{s}$, giving an etch stop window of 10 s, which is a reasonable window for a human operator in a lab environment.

Metallization and patterning - For this work, test cell metallization contacts are placed as depicted in Fig. 4. The contact layers are 400 nm thick aluminum evaporated through a shadow mask. A single contact with a width of 0.5 mm is placed in the etched trench (P-contact) and two, 2 mm wide contacts are placed on either side of it (N-contacts). No

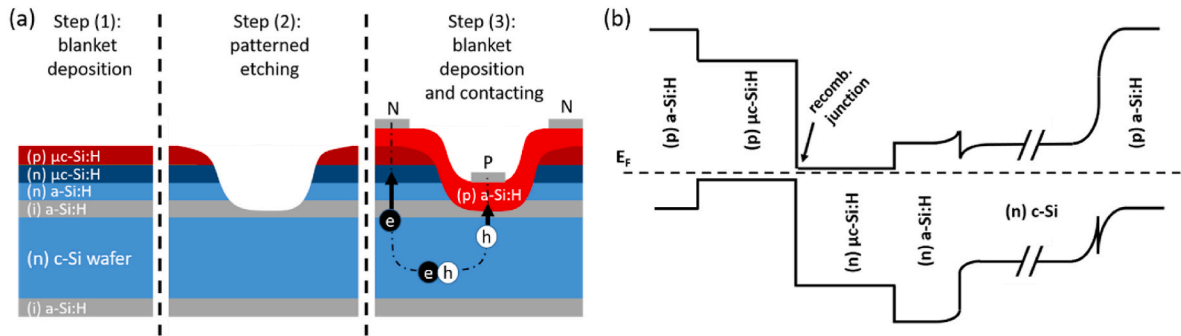


Fig. 1. (a) Device architecture and fabrication steps: (1) uniform deposition of front passivation layer, rear passivation stack, and recombination junction, (2) localized etching down to passivation layer, and (3) uniform deposition of (p) a-Si:H layer. (b) Energy band diagram of the structure following the path of the dashed line in step (3) ((i) a-Si:H layer not included).

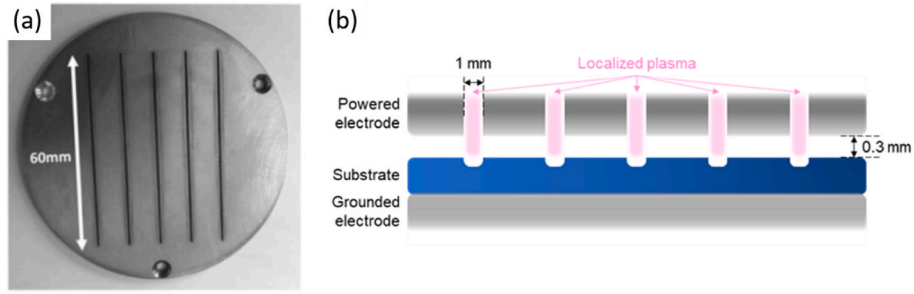


Fig. 2. (a) Photograph of patterned RF powered electrode, and (b) schematic showing localization of plasma within slits, limiting the extent of plasma processing area.

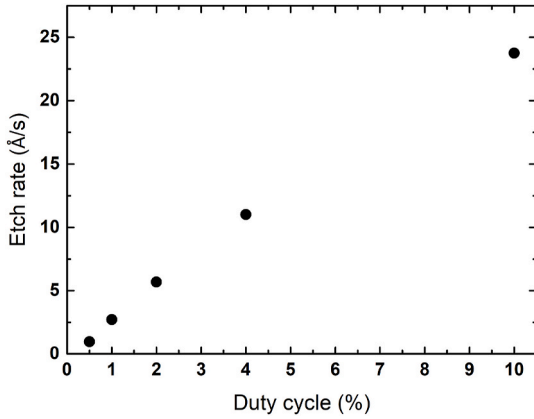


Fig. 3. Etch rate of (n) c-Si wafer as a function of duty cycle at a pulsing frequency of 1 kHz.

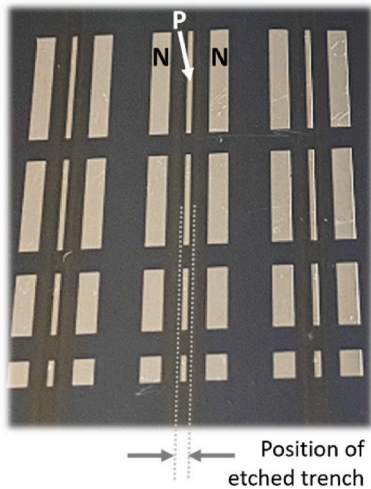


Fig. 4. Pattern of metallization for test cells in this work.

particular effort was made to optimize these contact widths (as is commonly done for IBC structures) except to make sure that the 0.5 mm contact lies fully within the etched trench. The contacts have lengths of 2, 5, 8 and 10 mm. With such contact placement and no careful masking of the illuminated area, it was difficult to precisely define the cell area, so all measurements are presented in values of current; the absolute value of efficiency claimed should be considered to have significant uncertainty.

2.2. Characterizations

A number of characterization techniques have been used throughout the course of this experimental work. To determine the shape of the etched trenches, profilometry was performed using a Bruker, Dektak XT. To determine the layer thickness and roughness, *ex-situ* spectroscopic ellipsometry was performed using a Horiba Jobin-Yvon UVISSEL. Quasi-steady-state photoconductance decay calibrated photoluminescence and the resulting minority carrier lifetime measurements were performed using a BT Imaging, LIS R2. Kelvin probe/Surface photovoltage scans were performed using a KPTechnology, ASKP200250, to acquire a surface photovoltage map. The current-voltage measurements were performed using a home-made setup with illumination (from the patterned side) with a spectrally adjusted halogen source, or in the dark. To determine the atomic composition of the layers, secondary ion mass spectrometry was performed by a private characterization company (Probian). Two different ion sources (O_2^+ for positive ion detection and Cs^+ for negative ion detection) were used for ablation.

3. Results and discussion

3.1. Before metallization (after etching)

Profilometry - The samples have been characterized at multiple steps throughout the process, and the first measurement is of the surface profile directly after the patterned etching step. In Fig. 5, the profile obtained after etching a (n) c-Si sample using a single slit is presented (with 60 W RF power pulsed at 1 kHz and with a duty cycle of 1%, giving an etch rate of ~ 1 Å/s). For comparison, also shown on this figure is the

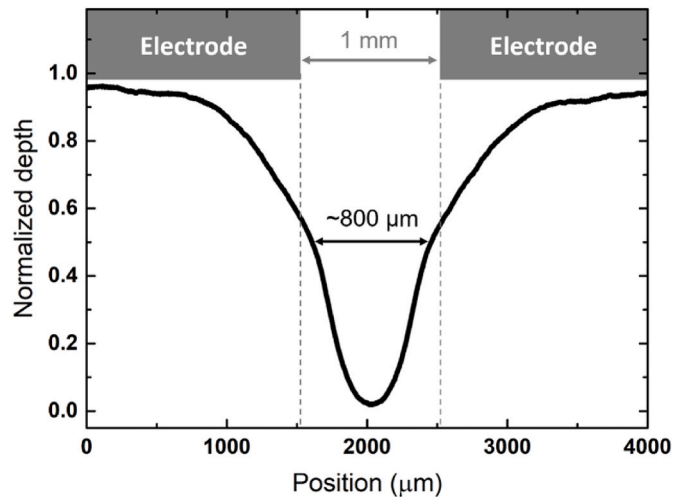


Fig. 5. Profilometry scan across a patterned etched trench. Patterned electrode (gray bars) and width of slit (dash lines) are shown for comparison.

width of the slit in the electrode. For this etching process, the full-width at half maximum is about 800 μm , which is less than the width of the slit (1 mm). However, the trench width at the surface is slightly wider than the slit. In previous work studying deposition using the same patterned electrode concept [23], the width of the deposition profile was actually narrower than the slit width. In subsequent work, a slight variation in deposition conditions showed a more complex profile, where the central deposited peak was superimposed on a weaker but broader trench profile [24]. In this work, the use of a fluorinated etching gas appears to broaden the trench profile. Whether this is a general trend for trench profiles when using the patterned plasma processing technique remains to be seen.

Spectroscopic Ellipsometry (SE) - SE spectra were also obtained for a stack sample before and after the patterned etching step (in the etched trench, but before the final (p) a-Si:H blanket deposition step), and are presented in Fig. 6. The initial “pristine” stack terminates with a (p) $\mu\text{c-Si:H}$ layer, and the characteristic shoulders of $\mu\text{c-Si:H}$ at 3.4 and 4.2 eV are observable on the blue curve of this figure. After performing the patterned etching step (with a 60 W RF power pulsed at 100 Hz with a duty cycle of 0.5%) and removing ~ 75 nm of material, only the (i) a-Si:H layer remains. A two-layer model with a bulk layer and a roughness layer has been used to fit the experimental data (as shown by the inset), where the amorphous material is described by a single Tauc-Lorentz dispersion formula. When fitting an optical model to the SE spectra obtained at this location, one observes the expected 9.9 nm layer of (i) a-Si:H, and a 2.2 nm roughness layer. Thus, we can precisely control the remaining thickness of the (i) a-Si:H layer, required to provide a low surface recombination in the P-contact region.

Photoluminescence (PL) - The profilometry and SE measurements above can provide morphological information concerning the trench profile and the surface roughness, but they will not be good predictors of photovoltaic behavior. A more effective predictor of photovoltaic behavior would be a mapping of the minority carrier lifetime, performed after the final, blanket (p) a-Si:H layer deposition, but before metallization. This is particularly important for the process being investigated in this work, as the patterned etching process must be precisely controlled, as depicted in Fig. 7. If etching is stopped at the (n) a-Si:H layer, this will prevent the formation of a P-N heterojunction with the (n) c-Si wafer when the final (p) a-Si:H is deposited. If too little (i) a-Si:H remains (and especially if etching continues after reaching the (n) c-Si surface) passivation will be poor and the open circuit voltage (V_{OC}) of devices will be low. The goal is therefore to optimize the process and

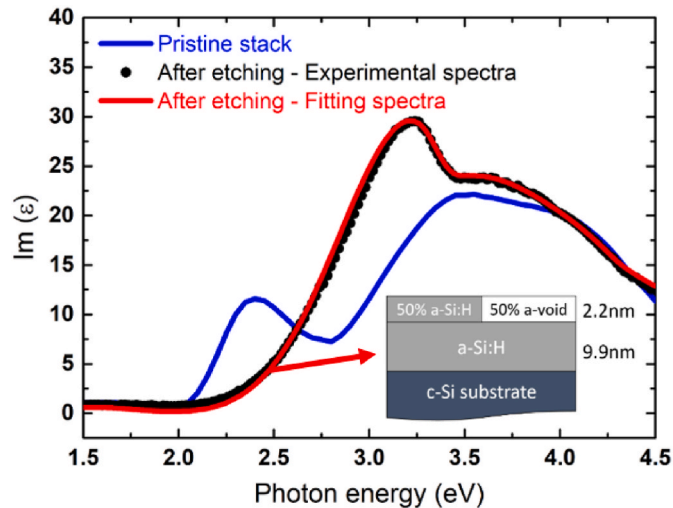


Fig. 6. Ellipsometry spectra for film stack taken before patterned plasma etching (blue line) and within etched trench (black dots) after etching. The fitting spectra after etching is also depicted (red line), along with the optical model shown in the inset.

completely remove the three-layer stack ((p) $\mu\text{c-Si:H}/(\text{n}) \mu\text{c-Si:H}/(\text{n})$ a-Si:H), while leaving a few nm of (i) a-Si:H to maintain a sufficient level of passivation.

With these limits in mind, the results of Fig. 8 are presented; these three subfigures are minority carrier lifetime mapping images (obtained through calibrated PL for minority carrier densities of 10^{15} cm^{-3}) for samples corresponding to the three different patterned etching scenarios in Fig. 7 (with (p) a-Si:H deposited). One can see that for the etching process leaving a significant amount of (n) a-Si:H, lifetimes greater than 10 ms are observed throughout the center of the wafer (Fig. 8(a)). No evidence of the etching process can be observed. For the etching process leaving only (i) a-Si:H (Fig. 8(b)), one can now recognize the slits pattern of the RF electrode (Fig. 2(a)), clearly showing where etching occurred. Although some degradation is seen, for most areas, the lifetime remains above 4 ms. The variation in lifetime is due to some inhomogeneity in the etching process. For the case where etching has reached the surface (Fig. 8(c)), we see that passivation has been destroyed in the etched areas. This result underlines the precision needed in the etching process, but is encouraging in that when etching down to the intrinsic layer, a sufficient level of passivation can be maintained.

Surface photovoltage (SPV) - The PL mapping results presented in Fig. 8 give a clear upper limit on the etching time, but will not indicate on their own if scenario (a) of Fig. 7 has occurred. If this does occur, the (n) a-Si:H will not be fully removed, and the blanket (p) a-Si:H layer will not contact the (i) a-Si:H to achieve a good P-N heterojunction. To verify that a junction was present before performing metallization, SPV measurements were carried out using a contactless Kelvin probe setup. This technique has been previously used to measure SPV in IBC cells as an optimization tool [27]. A typical SPV result for a device in this work is presented in Fig. 9. In this figure, one can see indeed that a photovoltage is present in the etched zones. A difference between the P and N regions of about 200 mV are observed. Although this value is much lower than the V_{OC} that would be expected from a c-Si solar cell, at this point, one can attribute this difference to either the very low illumination level used in the setup ($\sim 5 \text{ mW/cm}^2$), but also to the surface traps which decrease the observed photovoltage, even for high performance IBC structures [27].

3.2. After metallization

Current-voltage (I - V) measurements - The definitive characterization step for a solar cell is metallization and measurement of its I - V characteristic. These steps were performed, and a representative I - V curve for a cell where the (i) a-Si:H was completely removed is shown in Fig. 10. Although the I - V curves in the dark appear to indicate normal diodes, under illumination, S-shaped curves are apparent. Such shapes are typical of the presence of an undesired non-Ohmic junction somewhere in the solar cell stack, often at a metallic contact [28,29].

It should be noted that such curves could be obtained even when the PL image shows perfect passivation, reminding one that the challenges of passivation and transport are not easily solved simultaneously, and are often in contradiction. Such S-shaped curves were observed for a wide variety of remaining thickness of (i) a-Si:H, process conditions, annealing steps, and metallic contact designs. (This particular cell is selected so that all the subsequent data comes from a single pair of comparable cells, both with no remaining (i) a-Si:H). After exhaustive elimination of all other possible sources for these S-shaped curves, it was hypothesized that some residual surface layer on the etched area originating from the patterned etching step was at their origin. To remove this layer, a low-power, blanket etching step was added (performed in the OCTOPUS tool) before the final (p) a-Si:H deposition. For this “gentle” etching step, an $\text{NF}_3/\text{N}_2/\text{Ar}$ gas mixture was used, with an etch rate of 1 nm/s, which is slow enough to still allow for a manageable etch stop. One can note that this etch rate is in the same range as that of the patterned etching, but without any pulsing of the plasma.

In order to obtain the same final structure while incorporating this

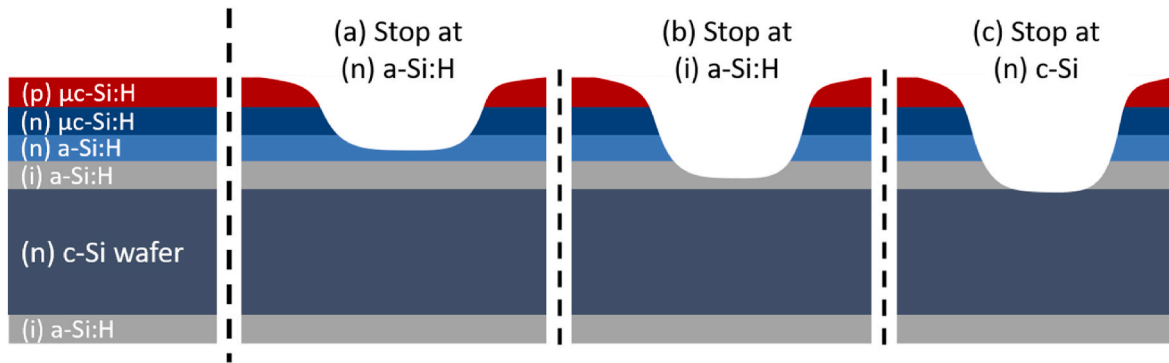


Fig. 7. Three different patterned etching scenarios (step (2) of Fig. 1(a): (a) the etching is stopped at the (n) a-Si:H, (b) the etching is stopped at the (i) a-Si:H, and (c) the etching is stopped at the (n) c-Si surface.

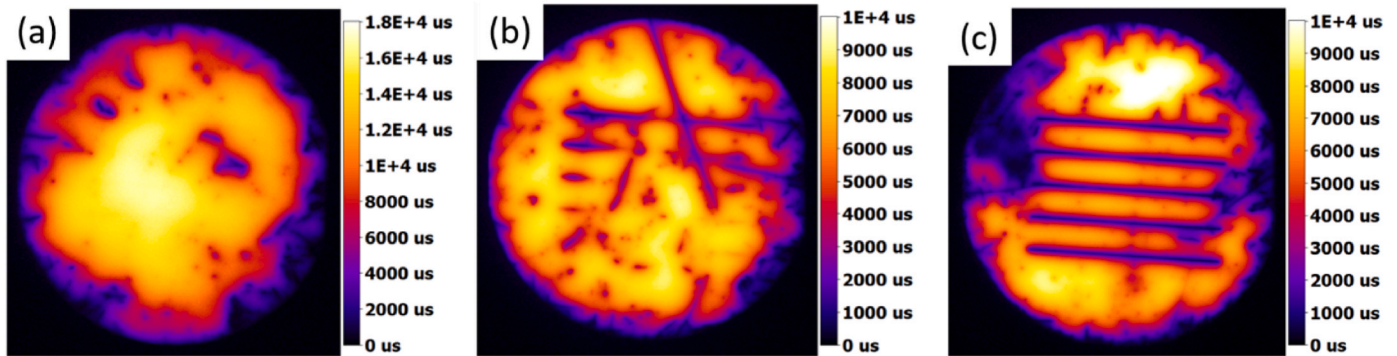


Fig. 8. Quasi-steady-state photoconductance decay calibrated photoluminescence lifetime mappings after final (p) a-Si:H deposition. Three different etching times are shown, resulting in the following: (a) some (n) a-Si:H remains after etching, (b) only (i) a-Si:H remains after etching, and (c) etching continues even after the (n) c-Si surface is exposed.

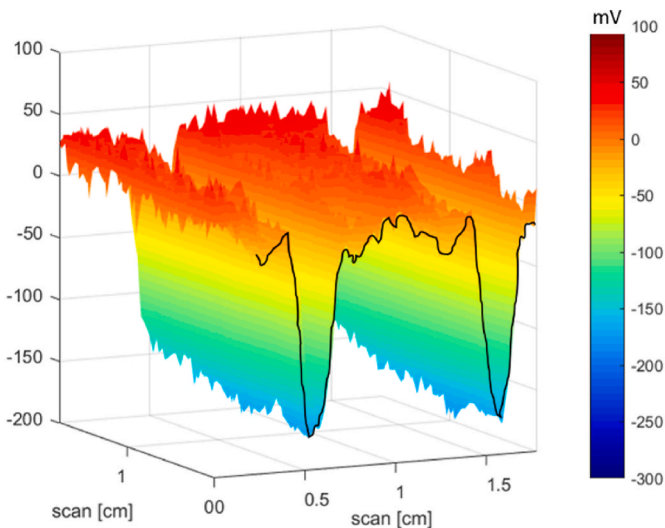


Fig. 9. 3D mapping of surface photovoltage for sample processed by patterned etching.

blanket etching step, two modifications were made to the process, as shown in Fig. 11. First, a thicker (p) $\mu\text{c-Si:H}$ was deposited in the blanket layer deposition step so that the recombination junction would still be present in the final device. Second, the patterned etching was stopped at the (n) a-Si:H layer. The blanket etching step then uniformly transfers the profile down, with the center of the trench reaching the (n) c-Si surface.

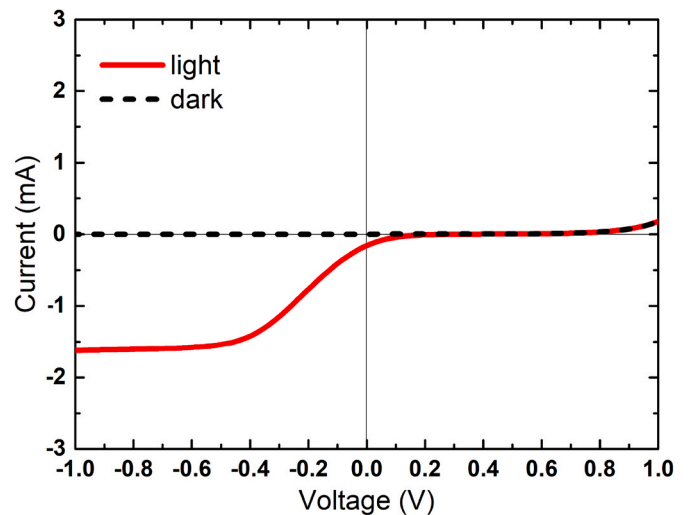


Fig. 10. Dark and light I - V characteristics for solar cell processed only by patterned etching.

Solar cells were fabricated using an identical process to the one that generated the I - V characteristics shown in Fig. 10, but including the additional “gentle” etching step, which completely removed the (i)a-Si:H within the trench. With the inclusion of this critical “gentle” etching step, the surface layer left after the patterned etching step was removed and an I - V characteristic without an S-shaped curve was achieved (as presented in Fig. 12). One can also note on the I - V curve of Fig. 12 that the V_{OC} of ~ 0.59 V is below the expected value for a HJT solar cell,

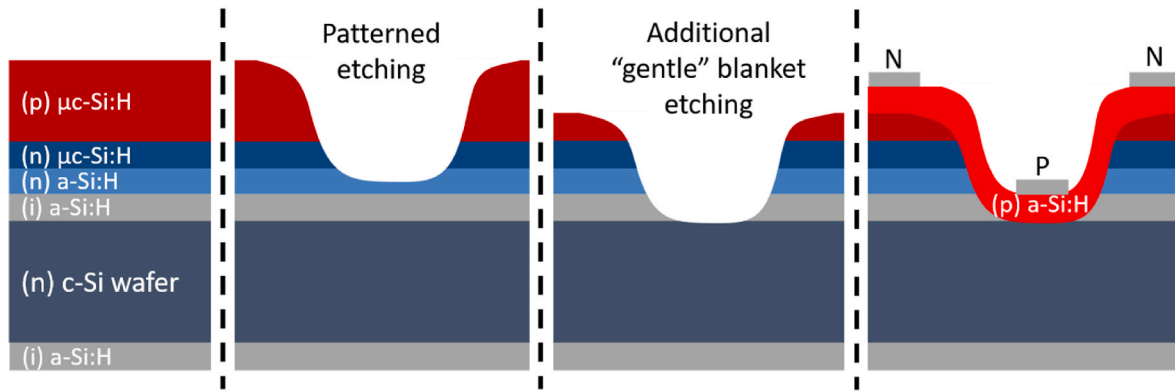


Fig. 11. Device fabrication process incorporating “gentle”, blanket etching step to remove surface layer after patterned etching.

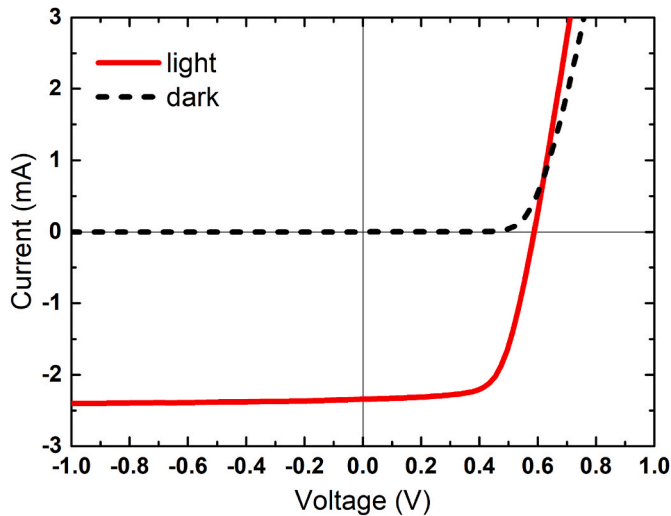


Fig. 12. Dark and light I - V characteristics for solar cell processed by “gentle”, blanket etching after the patterned etching.

which is logical as the entire (i) a-Si:H layer has been etched away, thus reducing the effectiveness of the passivation [30]. Keeping in mind that the wafer is not textured and does not have an anti-reflection coating, we estimate the active area to be 0.15 cm^2 , which gives a short circuit current density of approximately 15.6 mA/cm^2 . A fill factor of 65.8% for this cell is obtained, and this gives an estimated efficiency of 9.1%.

Secondary ion mass spectrometry (SIMS). Although from an engineering perspective, the problem can be considered solved, the question remained concerning the nature of this residual layer, and how the “gentle” etching mitigated it.

The most direct measurement thus far showing the impact of the “gentle” etching were SIMS measurements, the results of which are presented in Fig. 13. These measurements were performed on two samples, one having undergone the “gentle” etching step after the patterned etching, and another having only undergone the patterned etching. In both cases there was no (i) a-Si:H layer left, and both samples had been completed by depositing the blanket (p) a-Si:H layer on top. Fig. 13(a) shows elemental traces using positive ion detection (measured using O_2^+ ions for the ablation), whereas Fig. 13(b) shows the results for negative ion detection (obtained using Cs^+ ions for ablation).

The results of Fig. 13(a) show two important features: (1) although some C contamination can be observed, it is present in equal amounts for both samples (decreasing only very slightly with the “gentle” etching), and so is not at the origin of the S-shaped curve. (2) A more significant decrease caused by the “gentle” etching step is in the F concentration, which is somewhat counterintuitive, as this step itself uses a fluorinated

process gas.

More information can be gleaned from the results of Fig. 13(b), showing the traces for negative ions. In this graph, the decrease in F is again observed, as well as a decrease in O by about the same amount. Much more impressive is the decrease in N. The presence of N can be attributed both to its presence in NF_3 (and so the N could be incorporated in the subsurface during etching as NF_x fragments), or from the exposure of these samples to atmosphere between process steps. The SIMS results do not allow us to determine the more likely origin.

These results lead one to the following conclusion: the patterned etching process leaves behind a surface layer that is strongly impacted by the aggressive etching step, and contains traces of process gas contamination (N and F) but also atmospheric contamination from the air break (N_2 , O_2 , and H_2O). This layer is present in the device directly at the location of the P-N heterojunction, and can impact the device behavior, causing an S-shaped curve. Removal of this aggressive-etch impacted layer restores the surface, allows the formation of a proper P-N heterojunction, and suppresses the S-shaped curve.

Finally, the impact of the removal of said layer through the “gentle” blanket etch step is also observable in SPV measurements, and the result is presented in Fig. 14. One can note that, compared to the sample which has only undergone the patterned etching of Fig. 9, the SPV difference is augmented from about 200 mV to almost 350 mV by including this step in the process flow.

The results shown in Fig. 14 demonstrate the power of SPV mapping in optimizing IBC devices as they are very sensitive to the underlying issues with the solar cell. This emphasizes the effectiveness of SPV in optimizing process conditions, even before metallization.

4. Conclusions

We have demonstrated, for the first time, a maskless and contactless method to fabricate IBC-HJT solar cells. The novel element is an etching step that uses a patterned RF powered electrode in a capacitively-coupled PECVD chamber rather than a mask to create the P and N regions. Slowing this process down by using pulsed plasma excitation enables a reasonable etch rate and should allow to stop the etch at the correct, passivating (i) a-Si:H layer. The process has been demonstrated on flat wafers, and the impact of using textured wafers has not been considered, although it is known that such wafers can influence the optimization of devices, even for amorphous growth [31]. As well, the current etching step process gives a broad peak shape that will limit how closely contacts can be placed. Future efforts should focus on making this profile into a square shape. After this patterned etching process, a necessary step for good solar cell behavior is the removal of the top-most surface layer, which appears to be damaged by the patterned etching process, through a “gentle” blanket etching process. Once this “gentle” etching step is included, the solar cells no longer exhibit S-shaped curves in their I - V characteristics. The development of the patterned etching

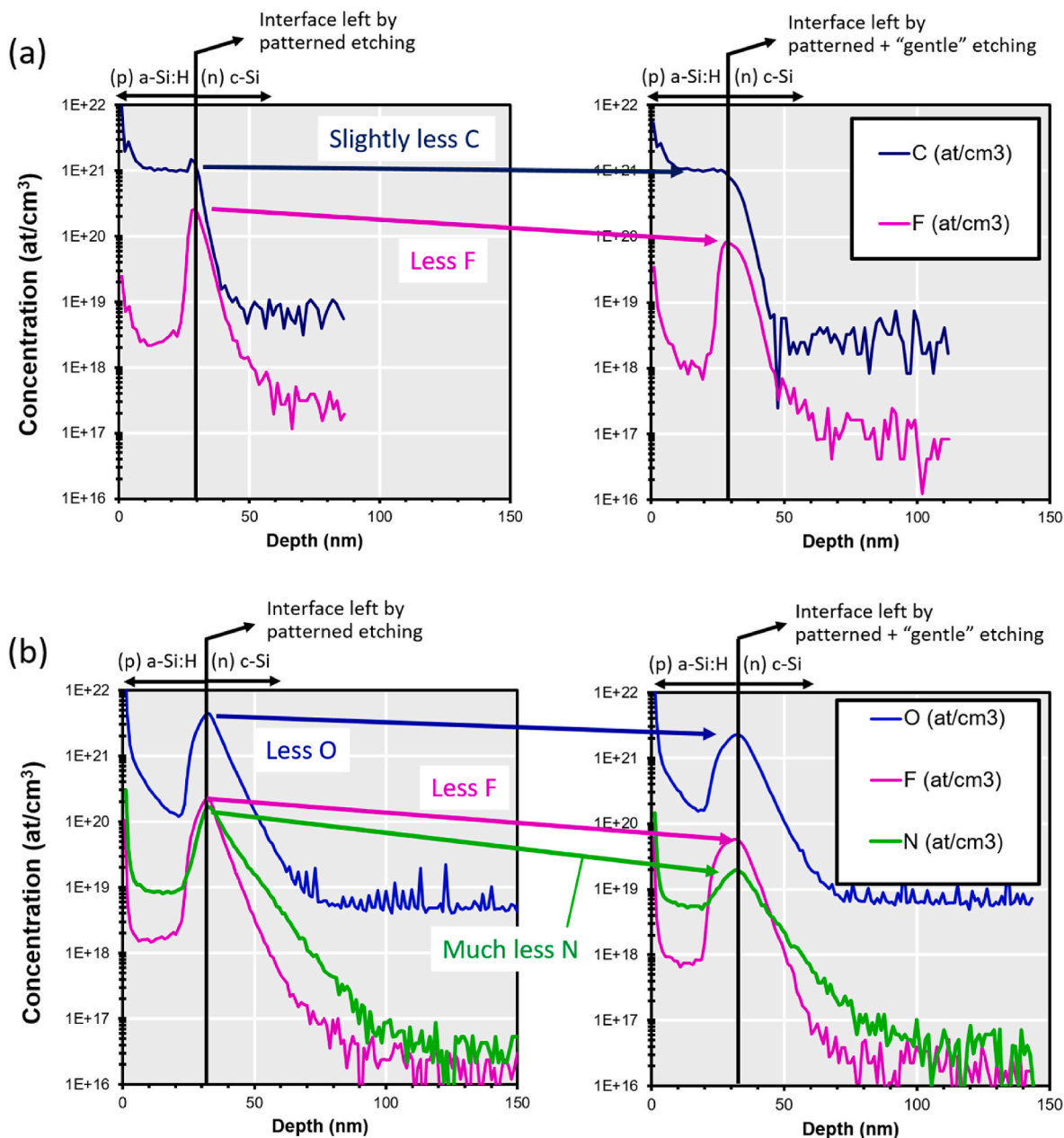


Fig. 13. Secondary ion mass spectrometry measurements. (a) Detection of positive ions using O_2^+ beam, (b) detection of negative ions using Cs^+ beam. The figures on the left correspond to the measurements after patterned etching while these on the right correspond to the profiles after patterned etching and “gentle” etching.

process is guided through the use of contactless measurements throughout, including spectroscopic ellipsometry, photoluminescence, and surface photovoltage measurements. This maskless process may hold advantages over the analogous use of a shadow mask within the deposition chamber, as no mask needs to be added or removed from vacuum between steps (the inter-electrode distance can be modified instead). Furthermore, as the electrode can be made much thicker than a shadow-mask (and therefore more robust), it is more compatible with producing a narrow spacing between the P and N contacts, particularly for full-size cells. However, producing an optimized etching profile to enable said very close finger spacing remains an open challenge.

CRedit authorship contribution statement

Junkang Wang: Writing – review & editing, Writing – original draft, Visualization, Validation, Resources, Methodology, Investigation,

Formal analysis. **Monalisa Ghosh:** Writing – review & editing, Resources, Investigation. **Karim Ouaras:** Writing – review & editing, Resources. **Dmitri Daineka:** Writing – review & editing, Resources. **Pavel Bulkin:** Writing – review & editing, Resources. **Pere Roca i Cabarrocas:** Writing – review & editing, Resources. **Sergej Filonovich:** Writing – review & editing, Resources, Conceptualization. **José Alvarez:** Writing – review & editing, Resources, Methodology, Investigation. **Erik V. Johnson:** Writing – review & editing, Writing – original draft, Supervision, Project administration, Methodology, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Erik Johnson reports financial support was provided by French National

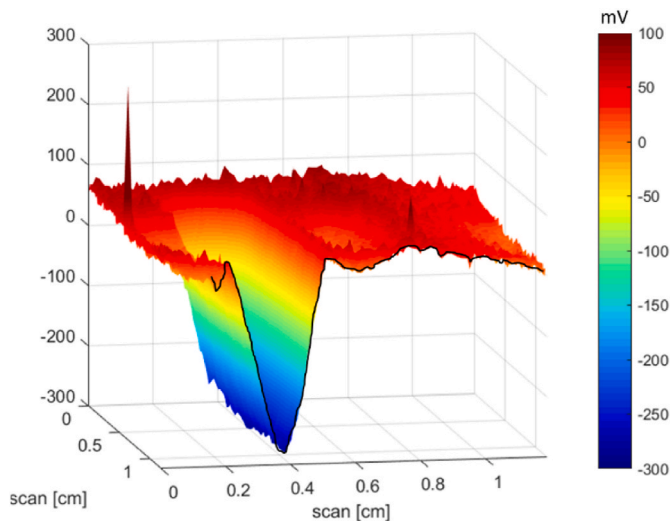


Fig. 14. 3D mapping of surface photovoltage for samples processed by patterned + blanket etching.

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