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Using HARV-SoC for Reliable Sensing Applications in Radiation Harsh Environments

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Abstract

Sensing systems are present in most application domains, including those in harsh environments. These systems are often designed around processing units sensitive to these environmental conditions. Still, the systems must withstand extreme operational conditions in these environments and maintain consistent measurements. In this work, we present the challenges imposed by radiation effects in sensing applications and discuss the utilization of a fault-tolerant RISC-V System-on-Chip, the HARV-SoC, to mitigate their impact. The HARV-SoC comprises peripherals and the fault-tolerant HARV core, which relies on hardening strategies, such as physical and information redundancy, to meet the requirements of critical applications targeting harsh environments and reduce the propagation of errors. Hence, we guide how to employ the proposed system in sensing applications and empower the community with a new tool for reliability-oriented projects.

Index Terms

RISC-V, System-on-Chip, Sensors, Reliability, Radiation Effects

I. INTRODUCTION

Sensing research and development has experienced significant growth in recent years, instigated by their broad utilization in several application domains (e.g., radiation facilities, avionics, aerospace, and industry). Some of these applications are exposed to harsh environments, which may affect the operation of the electronic system due to harsh conditions such as extreme temperatures, pressure, corrosion, and radiation [1]. Thus, these systems must monitor the environmental conditions with proper sensors to ensure safe and acceptable operation. Besides that, the elements connected to the sensor, such as controllers, interfaces, and peripherals, must also be designed to deal with the characteristics of the harsh environment.

For example, in nuclear power plants [2], [3] and particle accelerators [4], [5], the electronic components and systems may be exposed to a mixed radiation field. This exposure can lead to different types of radiation damage as displacement damage, Single Event Effects (SEEs), and Total Ionizing Dose (TID). The operation of the systems can be affected by transient, permanent, or intermittent faults caused by the condition of harsh environments [6]. For instance, single and multiple-bit upsets in sensitive elements and structures of a system may lead to catastrophic failures in critical systems.

The effects caused by radiation can be mitigated by using radiation-hardened components. Although, these components are expensive due to the tailored manufacturing process and the niche market. Moreover, many of these components are based on proven, and older technologies and may lack in performance, e.g., power consumption and processing speed [7].

One possible approach is to use Commercial Off-The-Shelf (COTS) devices, mainly designed for terrestrial commercial purposes. However, most documentation of COTS components does not have the necessary radiation data to estimate their degradation in different environments [8]. Another possibility is to combine COTS components with radiation-hardening techniques. The developers can employ redundancy methods by exploiting temporal, spatial, and informational characteristics of a system to improve reliability [9].

In this context, in [10], we presented HARV-SoC, an open-source fault-tolerant RISC-V System-on-Chip (SoC), aimed at hardening the processor against SEEs and enduring the TID of most applications. The RISC-V is an open-source emerging Instruction Set Architecture (ISA) that is becoming an industry standard [11]. It is based on the design of the

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MIPS processor and has an optimized architecture aimed at simplifying implementation. Despite the several soft-core RISC-V implementations [12]–[14], there are few readily available fault-tolerant RISC-V processors. The focus of the HARV-SoC soft-core implementation is to achieve the highest reliability with the least possible resource usage. The SoC was hardened in its internal architectural structures and has been proven robust for different environments, withstanding harsh radiation conditions. In this work, we discuss the use of the HARV-SoC in several sensing applications in radiation harsh environments.

The remainder of this paper is organized as follows. Section II presents relevant related works. Section III describes the HARV-SoC implementation and its fault tolerance features. Section IV presents possible applications using the HARV-SoC. Finally, Section V gives the final conclusion and proposes future works.

II. RELATED WORK

The following subsections present works that explore the RISC-V ISA for sensing applications and apply fault tolerance techniques to improve the systems' reliability.

A. RISC-V in Sensing Applications

In [15], the authors used the Microchip PolarFire SoC with a RISC-V processor to evaluate the performance and power consumption of the RISC-V architecture for onboard sensor data processing applications. For this, they compared the metrics with platforms containing the ARM Cortex-A9, ARM Cortex-A53, and Power e5500 architectures. The results show that the RISC-V architecture provides a competitive balance between performance and power consumption when compared against well-established ARM Cortex and Power architectures.

The authors from [16] proposed a lightweight pipeline integrated deep learning architecture compatible with RISC-V instructions. Their main goal was to improve the computational performance as much as possible under the limit of low power consumption to accelerate the processing of data captured by the sensors. Thus, they explored instruction- and data-level parallelism to obtain a satisfactory energy efficiency ratio and meet the balanced performance metrics, including low power consumption, low latency, and flexible configuration.

B. RISC-V for Harsh Environments

The Scale4Edge project [17] focused on the development of an ecosystem based on a platform concept to supply efficient and cost-effective application-specific edge devices and services for different market segments. The platform is customizable by optional instructions for individual applications, such as High Reliability (HiRel). The Scale4Edge HiRel platform employs a multiprocessor architecture of RISC-V cores that can be configured in hardware lock-step modes, enabling core-level error detection and correction to increase reliability.

The DuckCore, a fault-tolerant processor core architecture based on RISC-V, is proposed in [18]. This architecture uses improved SECCED (Single Error Correction, Double Error Detection) code between pipelines, detects processor operating errors in real-time through the supervision unit, and takes instruction rollbacks for different error types.

C. This Work

Currently, there is a lack of readily available fault-tolerant RISC-V systems that aim at sensing applications. The HARV-SoC is a fault-tolerant processing system, based on readily available COTS components. Thus, in this work, we discuss and present how this SoC can be useful for certain sensing applications and the possible benefits of its usage.

III. FAULT-TOLERANT RISC-V SoC

The HARV-SoC is a RISC-V-based SoC that focuses on reliability for harsh applications [10]. In order to provide these features, this SoC uses the HARV (Hardened RISC-V) processor core [19], which applies fault tolerance techniques to aid in detecting and correcting errors. The following subsections present the HARV processor core and SoC, followed by its radiation characterization.

A. HARV Core

HARV is a multi-cycle RISC-V-based processor core that supports the integer instruction set (RV32I), Control and Status Registers (CSRs), interrupts, and exceptions. Its multi-cycle architecture comprises five stages: instruction fetch, execution, memory access, write back and handle trap. This separation of stages enables faster instruction execution for non-memory access instructions, which will take at least one less cycle when compared to memory access instructions. Furthermore, utilizing a stage for handling traps simplifies the logic for handling synchronous traps. This core is implemented as a soft-core described in VHDL (Very-High Speed Integrated-Circuit Hardware Description Language), improving its portability to most FPGA (Field-Programmable Gate Array) vendors.

Concerning the hardening against faults, HARV applies techniques such as ECC (Error-Correcting Code) and TMR (Triple-Modular Redundancy) for the detection and correction of errors in its internal components. The registers of the register file, the program counter, and the instruction register are hardened using SECCED (Single-Error Correction and Double-Error Detection). The control, ALU (Arithmetic-Logic Unit), and critical CSRs use TMR for hardening. An overview of the HARV core architecture and hardening techniques is presented in Fig. 1.

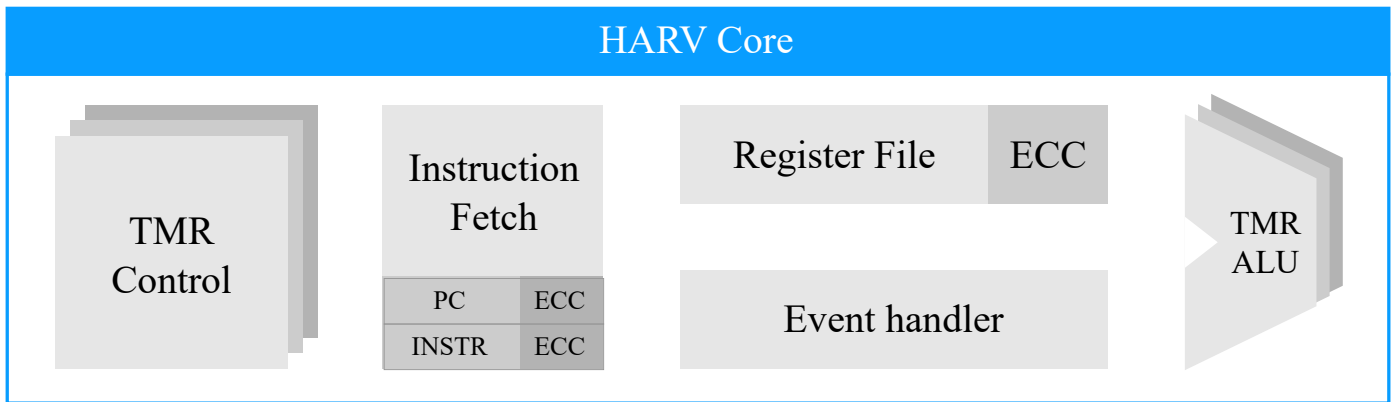


Fig. 1. HARV core overview.

In addition to the hardening, the HARV processor also provides error reporting capabilities, enabling further application reliability. The error reporting is provided through exceptions, which synchronously interrupt the application flow and report detailed information on the detected error, such as the fault type, application context, and corrupted data. These details enable further investigation by the application to decide, for example, the action taken in case of a double-bit upset in the Program Counter (PC), which is not correctable by the processor architecture.

B. Hardened RISC-V System-on-Chip

The HARV-SoC is a reliable SoC that comprises the peripherals and their integration with the processor while having a low area overhead for its fault tolerance techniques [20]. It has standard features of modern microcontrollers, including support for FreeRTOS and peripherals such as I2C (Inter-Integrated Circuit), GPIO (General Purpose Input/Output), SPI (Serial Peripheral Interface), CAN (Controller Area Network), and UART (Universal Asynchronous Receiver/Transmitter). Also, the SoC includes controllers that enable access to external memories, such as Flash and SDRAM (Synchronous Dynamic Random Access Memory).

Fig. 2 presents an overview of the SoC architecture, including the HARV processor, its interconnection with peripherals, and the fault monitor module, which comprises error correction, detection, and reporting.

The reliability of the HARV-SoC is provided by hardening its critical components, i.e., data memory ECC, bus access timeout, reset controller, watchdog timer reset, and application checksum. For the data memory, the SoC has a configurable parameter that separates the memory into two parts: the data and the ECC. For access to peripherals, the master bus controller provides a timeout flag that triggers an exception when a peripheral takes too long to respond. With the bus timeout, the application receives information about the faulty peripheral. The application may use this faulty peripheral information to perform actions to restore the functionality of a peripheral. For that, the SoC provides a reset controller, which enables resetting specific peripherals. Besides the timeout from the bus, the system also provides a watchdog timer that resets the SoC when a timeout is reached, preventing hang processor failures.

In addition to the hardening embedded in the SoC, application checksum verification is provided. The application startup routines check the entire application using the CRC-32 (Cyclic Redundancy Check-32) checksum. This verification enables the detection of errors while loading the program from the Flash memory.

Furthermore, the fault monitor's error reporting capabilities enable the application to perform actions according to the detected error. If the error is not correctable, the application uses the available information to decide, for example, to ignore the error and continue the execution or even force a system reset to avoid faulty system behavior.

C. Radiation Characterization

The HARV-SoC has been tested in radiation experiments in particle accelerator facilities with different types of particles, such as neutrons, protons, and mixed-field. The latest work [10] presents the results from a test campaign with neutron irradiation in the Chiplr beamline at the Rutherford Appleton Laboratory (RAL), United Kingdom, which reported 97.73% of correct benchmark executions, correcting 98.89% of the detected errors in the fully hardened version of the SoC. The work also presented a detailed analysis of the faulty executions.

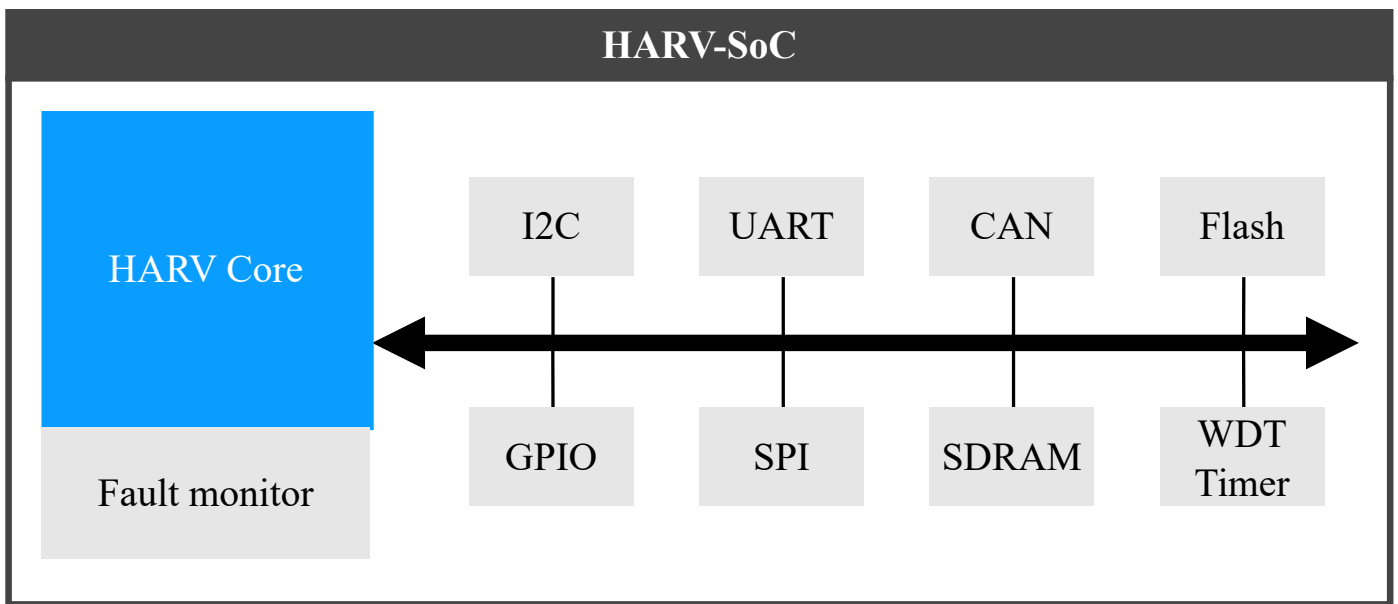


Fig. 2. HARV-SoC – fault-tolerant RISC-V SoC architecture.

IV. APPLICATIONS

In this section, we present some sensing application use cases in which HARV-SoC can be used to improve the system's reliability. Despite that, it is important to mention that HARV-SoC is not limited to the given examples since it was primarily developed for harsh environments (e.g., space applications), enabling robust systems to be deployed in these challenging scenarios. Then, our intent in this work is to guide the use of the SoC in a subset of these applications (e.g., sensing, test setups) and empower interested readers with a new tool for projects as well as radiation experiments.

A. Long-Term Exposure

Robust and hardened devices are required for electronics with long-term radiation exposure. When the irradiation is severe, more drastic countermeasures are applied, using expensive hardened devices in complex redundant topologies. However, electronics are not always employed in severe environments for long periods. They often have mild exposure with more moderate requirements, and, in some cases, they need to endure sporadic harsher events.

Nuclear power plants [2], [3] and particle accelerators [4], [5] are examples of facilities where many complex systems and networks are installed, enduring harsh and mild environments with various levels of reliability requirements. As mentioned, applying radiation-hardened devices is expensive, and deploying COTS-only systems is risky and requires high maintenance. Thus, developers combine both approaches to find the most optimized solutions. The HARV-SoC has many desirable characteristics to provide more flexibility for developing these systems, such as enhanced reliability, resourceful fault awareness, design simplicity, and low cost.

For instance, as suggested in [21], the controller unit is an important component to be analyzed under radiation for these applications. As stated in the article, the challenges arise not only from arranging the building blocks for the system but also from the radiation assurance perspective due to the lack of observability in the device and the limited capabilities to recreate realistic irradiation conditions. Hence, HARV-SoC is again a compelling candidate since it provides a lot of built-in internal and flexible external observability. These features allow proper SEE characterization of the full platform since, besides system-level testing, it is possible to have a much deeper analysis of the controller unit without major tailored and complex test fixtures.

Fig. 3 presents the mentioned sensing solution. Each subsystem is subject to different types of validation and concerns: recoverability and robustness of the controller unit, with system-level testing; transceiver device resilience, in which device characterization is envisioned; power system continuity of service, with failure rates and mean time to failure type of tests. It is worth mentioning that such a platform can be used to detect leakages in nuclear power plants, remote sensing units distributed in complex particle accelerators, or to retrofit and upgrade older systems without requiring major infrastructure modifications.

In [23], the authors present key aspects of mobile robots in emergency response to nuclear accidents. The robots need to withstand the radiation encountered in these environments, where different levels of exposure are experienced.



Fig. 3. Battery-powered radiation Monitoring (BatMon) system, a radiation tolerant wireless Internet of Things (IoT) platform for on-field sensor data acquisition [22].

In this case, each robot includes several sensors and actuators, depending on the specific mission. They were designed to operate in normal conditions, and efforts were made to understand their reliability in situ. This application would greatly benefit from using HARV-SoC in the robot's design due to the SoC characteristics: reliability, fault awareness, low cost, low power, and portability. Similarly, the authors in [24] analyze technologies for robotic platforms supporting nuclear decommissioning. They emphasize the reliability requirements for the processing subsystem and provide guidelines for the qualification of such platforms.

B. Atmospheric and Space Applications

Another interesting application for HARV-SoC is payloads embedding sensors and measurement units, targeting in-orbit operation or validating these systems: a processing unit for a camera module in a satellite; a radiation sensor module [25]; or an in-orbit measurement unit [26]. In the first case, the main objective is to provide the most reliable controller to allow continuous and predictable sensor operation. Similarly, in the other use cases, the controller handles important functions associated with the operation of the sensor or experiment and suffers from the same damaging effects that it aims to measure, hence the controller should be more robust and tolerant facing radiation. Despite that, these applications can still compromise the reliability or continuity of operation within their scope (e.g., atmospheric probes, Low Earth Orbit (LEO) satellites). Therefore, developers aim to find solutions that meet the reliability requirements with the lowest effort and cost.

In this context, HARV-SoC is again a competing candidate. The community behind the RISC-V architecture has always-evolving software support with libraries in several domains. Thus, HARV-SoC, as a compatible RISC-V SoC, allows easy porting of these frameworks and provides a standard interface for future extensions. Also, deploying these enhanced COTS-based systems is cheaper than traditional solutions based on radiation-hardened devices.

Fig. 4 shows the payload board that was part of two satellite projects, aiming to perform in-orbit measurements using various memory devices as radiation sensors [26]. This system comprises a main controller that handles and reports the results from algorithms executed in several memory devices target of the study. In this case, an FPGA was used to implement the required memory buses, execute the algorithms, manage experimental data, and forward the data

to the satellite modules. This custom solution was selected to exploit the chosen FPGA device robustness and further hardening enhancements in the implemented controlling logic, characteristics not found in COTS microcontrollers and SoCs at the time. Despite being robust, this solution required considerable development effort and many project iterations to achieve a flight-ready version. This could be reduced if a reliable processor-based approach was readily available and properly validated. Nowadays, this is the case for HARV-SoC, which hybrid architecture with a processor, built-in peripherals, and available programmable array enables the implementation of very flexible and agile solutions, keeping the targeted reliability. It is possible due to the SoC architecture, which allows custom configurations, and the possibility to port existing software and libraries in well-established and high-level programming languages for embedded systems, supporting faster development.

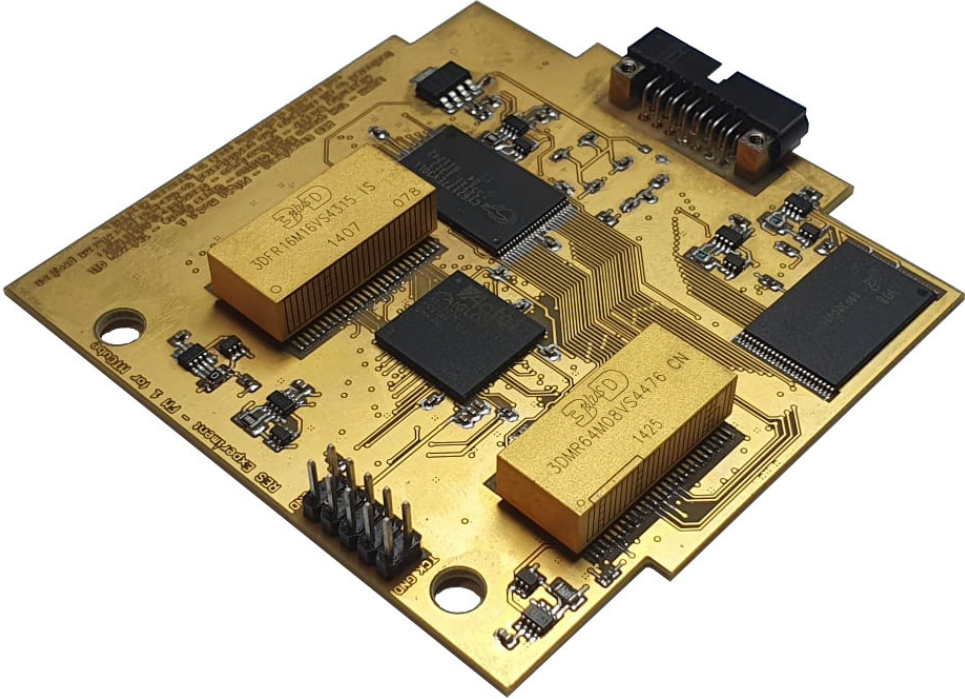


Fig. 4. Radiation Effects Study (RES) experiment board [26].

C. Challenging Radiation Experiments

A compelling use case for HARV-SoC is with radiation testing when not only the device under test is irradiated but the entire system. This is not the case for most experiments, where users have reasonable control over the irradiation area or the full system is exposed to minor effects due to secondaries. However, the irradiation area in some facilities is not configurable or roughly defined, or the source generates harmful secondaries. This is the case for CHARM [27], a mixed-field irradiation facility located at European Council for Nuclear Research (CERN), Switzerland, and ChipIrr [28], which generates atmospheric-like neutrons and is located at Rutherford Appleton Laboratory (RAL), United Kingdom.

Fig. 5 presents a board used in experiments of this nature in both mentioned facilities [29]. The system was designed to be testable in these facilities and also to endure a satellite mission for additional testing and validation. The main target of the experiment is to compare three different generations of an SDRAM memory to investigate the various changing technological elements and their impact on radiation performance. It hosts the controller close to the target memory devices to improve their operation and to fit in nanosatellite missions easily.

For the CHARM experiment, these attributes are essential to provide proper results with statistical significance. To reach targeted event counts, the full system must reliably endure the full duration of the test. Notably, the facility accumulates significant TID and induces a lot of SEE in all controlling circuits. For testing complex devices (e.g., memories, transceivers) or even system-level testing (e.g., complete boards, a full nanosatellite [30]), a test controller is often required to apply the test stimuli and report the acquired data. Thus, a reliable microcontroller combined with a flexible FPGA architecture offers an adequate environment for applying that. In this case, the use of HARV-SoC allows safely performing test algorithms in the memories, collecting the results, and reporting reliable experimental data, since the acquired data are not corrupted or erroneously generated in the controller itself.



Fig. 5. Harsh Environment CubeSat Payload (HARSH) board [29].

D. Processor-based Radiation Experiments

A particular application for the HARV-SoC is validating a sensing platform with built-in processing capabilities using complex software design or demanding algorithms. For instance, it can be a robust machine-learning algorithm designed to identify and classify structures or perform dynamic compression algorithms. Two main scenarios are envisioned: the test targets evaluating and comparing only the algorithm with different implementations, or HARV-SoC can be deployed in the actual application, and the test aims to evaluate the system's reliability. In both cases, the observability gained with HARV-SoC greatly supports the analysis. For example, it allows checking for corrupted data in registers and system memory, tracking execution flow just before an error, and critical failures not correctable, allowing proper selection of data in post-analysis.

More specifically, for the first presented scenario, the usage of HARV-SoC has very useful characteristics and features that significantly enhance the test. As mentioned, besides providing internal information to be correlated to the algorithm, it has different hardening configurations, allowing to enable or disable specific corrections. This can isolate or expose a specific element or characteristic of the algorithm and provide better data for analysis. More than that, the disabled corrections keep the error reporting, allowing more comparisons and information about error propagation.

In [31], the authors investigated the impact of radiation-induced errors in approximate computing. In this case, they used a neural network as a case study in an experimental approach to acquire realistic characterization data rather than an artificial injection. The study focused on the impact of memory errors in the application with different levels of approximation, thus the main processing unit was not irradiated. This is another example of the opportunity to improve the test using HARV-SoC. The researchers could have used the aforementioned features to extend their analysis and maintain a proper understanding of the irradiation impact on the overall system, despite the more complex setup.

V. CONCLUSION

In this work, we presented demanding sensing applications and how developers would benefit from utilizing fault-tolerant processing systems based on readily available COTS components. The main aspects and challenges were discussed in each use case, providing notions on employing these low-cost hardened solutions. In particular, systems designed with HARV-SoC present many desired characteristics that provide the required tools for developing and validating the mentioned applications due to the many fault tolerance techniques and error reporting strategies applied in the SoC architecture.

It is important to mention that hardened processing systems are available based on other architectures designed and validated in the industry and academia. However, using RISC-V-based solutions poses a bright future perspective

to novel developments due to the open-source nature of the architecture and the community behind it. With an always-evolving framework, RISC-V systems can inherit existing standard and robust software solutions from other application fields, enabling faster and more secure development. Also, it allows a rich and free ecosystem of development tools, reducing vendor dependency. We embrace this philosophy, making HARV readily available to the community, as shown in our prior works [32].

In future work, we envision improving the SoC capabilities by adding more performance with architectural changes and augmenting the platform with more flexible and diverse peripherals. Also, extending the radiation characterizations is a step forward to meet the requirements of more demanding applications and ensure reliability in a broader set of harsh environments.

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